DESCRIPTION

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The SDS14C15L08 component is designed to provide transient suppression on multiple data lines and I/O ports.

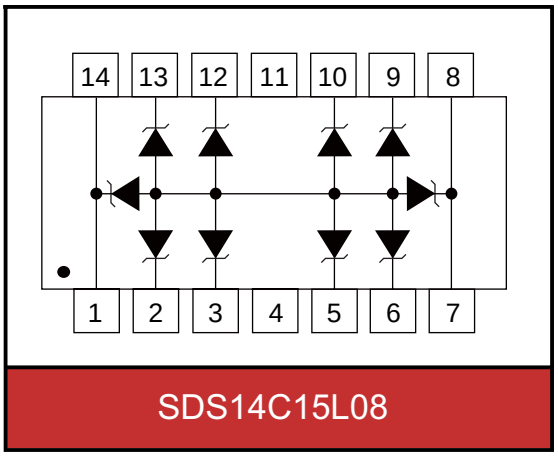
The low profile SOIC-14 design allows the user to protect up to eight data and I/O lines with one package.

This device will meet the surge requirements of IEC61000-4-2 (Formerly IEC 801-2), Level 4. "Human Body Model" for air and contact discharge.

HBM : ±8kV
Air Mode : ±15kV

SPECIFICATION FEATURES

- IEC61000-4-2 ESD 15KV Air,8KV contact compliance
- SOIC-14 surface mount package
- Protects eight I/O lines
- Peak power dissipation of 350W under 8/20μs waveform
- Working voltage : 15V
- Low leakage current
- Low clamping voltage
- Solid-state silicon avalanche technology
- Lead Free/RoHS compliant
- Solder reflow temperature:Pure Tin-Sn,260-270℃
- Flammability rating UL 94V-0



APPLICATIONS

- RS-232 and RS-422 data line protection
- Microprocessor based equipment
- LAN/WAN equipment
- Set Top Box (STB)
- Series and parallel ports
- Instrumentation
- Notebooks,desktops,servers
- Peripherals
- I^2C serial port

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak pulse power (tp=8/20μs waveform)	Ppp	350	W
ESD voltage (HBM contact)	V_{ESD}	±8	KV
ESD voltage (AIR contact)		±15	
Storage & operating temperature range	T_{STG} ,T_J	-55~+150	℃

ELECTRICAL CHARACTERISTICS (T_J=25℃)

SDS14C15L08 (Marking: B SM15C-8)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse stand-off voltage	V_{RWM}				15	V
Reverse breakdown voltage	V_{BR}	I_{BR}=1mA	16.7			V
Reverse leakage current	I_R	V_R=15V each I/O pin			1	μA
Clamping voltage (tp=8/20μs)	V_C	I_{PP}=1A			24	V
Clamping voltage (tp=8/20μs)	V_C	I_{PP}=5A			30	V
Off state junction capacitance	C_J	0Vdc,f=1MHZ between I/O pins and GND			75	pF

APPLICATIONS INFORMATION

Pins 2, 3, 5, 6, 9, 10, 12 and 13 are connected to the lines that are to be protected. Pins 1, 7, 8 and 14 are connected to ground. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces. Pins 4 and 11 are not connected.

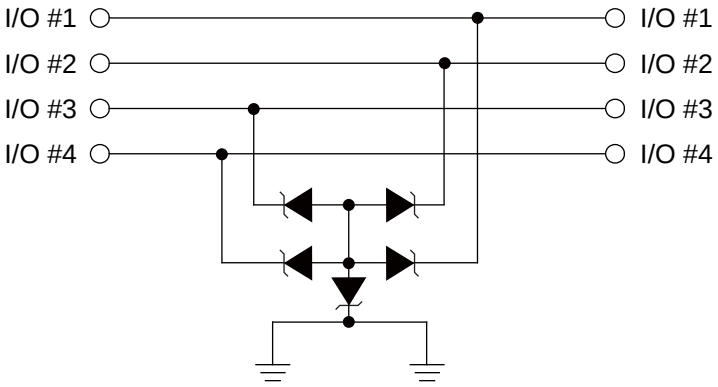
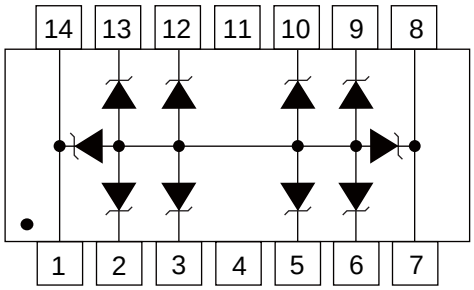


Figure 1. Bi-directional Protection



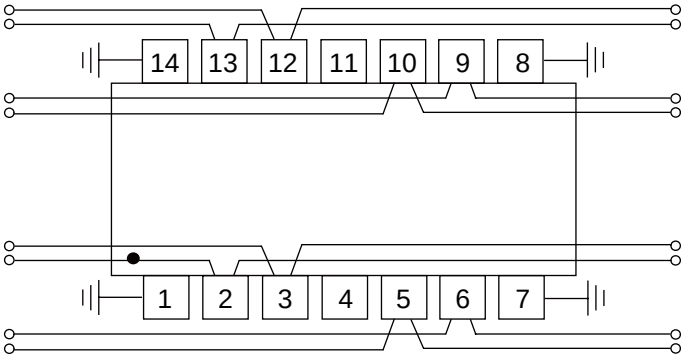


Figure 2. Short Path Length
(Reduce Parasitic Inductance)

TYPICAL CHARACTERISTICS CURVES

Figure 1. Power Derating Curve

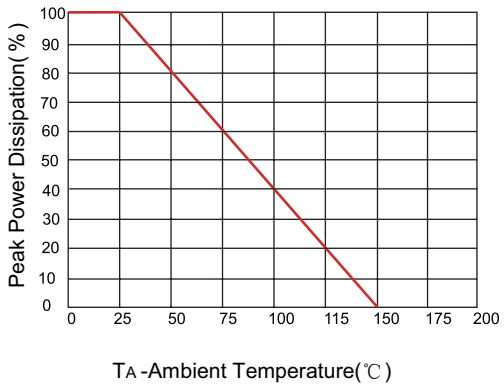


Figure 2. Pulse Waveforms

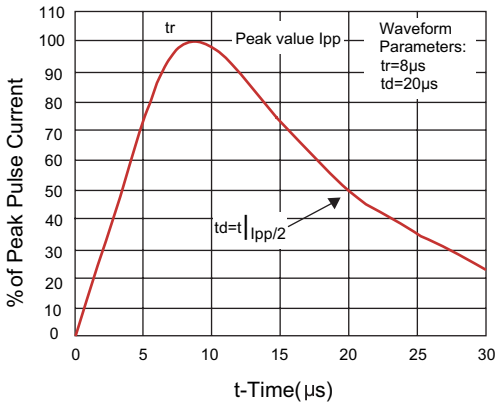
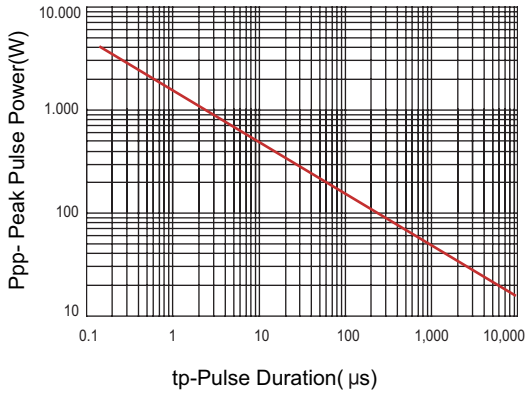
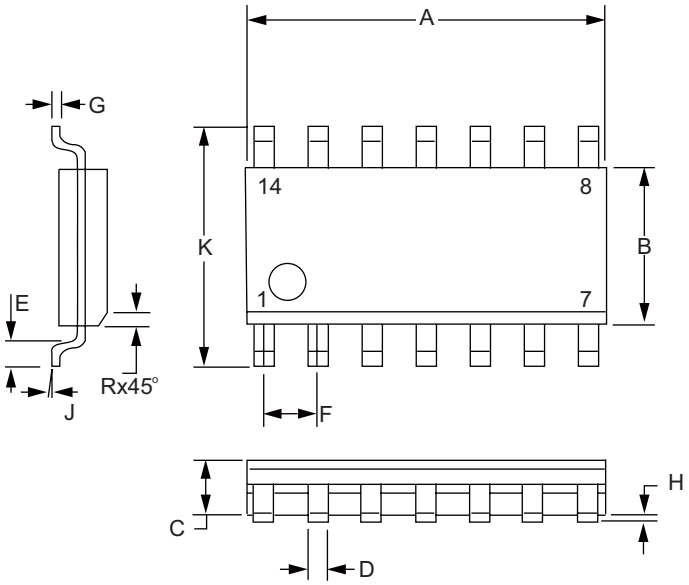


Figure 3. Non-Repetitive Peak Pulse vs Pulse Time



PACKAGE AND SUGGESTED PAD LAYOUT DIMENSION

SOIC-16(unit:mm)



DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.337	0.344	8.55	8.75
B	0.150	0.157	3.80	4.00
C	0.054	0.068	1.35	1.75
D	0.014	0.019	0.35	0.49
E	0.016	0.049	0.40	1.25
F	0.050 BSC		1.27 BSC	
G	0.008	0.009	0.19	0.25
H	0.004	0.009	0.10	0.25
J	0°	7°	0°	7°
K	0.228	0.244	5.80	6.20
R	0.010	0.019	0.25	0.50