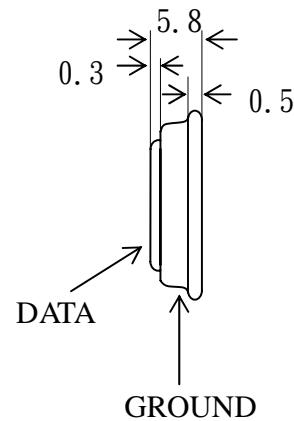
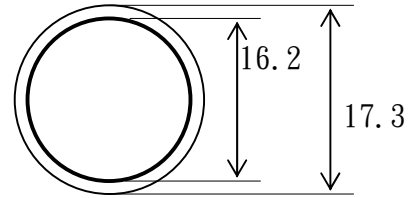


SMC1990A1

FEATURES

- The SMC1990 is compatible with the DS1990
 - Extended 2.8 to 5.25 voltage range
- Unique, 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester); guaranteed no two parts alike
- 8-bit family code specifies SMC1990 communications requirements to reader
- Presence Pulse acknowledges when the reader first applies voltage
- Reduces control, address, data, and power to a single pin
- Zero standby power required
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits/s
- Applications
 - PCB Identification
 - Network Node ID
 - Equipment Registration
- Operates over industrial temperature range of -40°C to +85°C





DESCRIPTION

The SMC1990 enhanced Silicon Serial Number is a low-cost, electronic registration number that Provides an absolutely unique identity which can be determined with a minimal electronic interface (typically, a single port pin of a microcontroller). The SMC1990 consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the Smart-Wire protocol that requires only a single data lead and a ground return. Power for reading and writing the device is derived from the data line itself with no need for an external power source.

OPERATION

The SMC1990's internal ROM is accessed via a single data line. The 48-bit serial number, 8-bit family code and 8-bit CRC are retrieved using the SMC Smart-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. All data is read and written least significant bit first.

Smart-Wire BUS SYSTEM

The Smart-Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the SMC1990 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and Smart-Wire signaling (signal type and timing).

Hardware Configuration

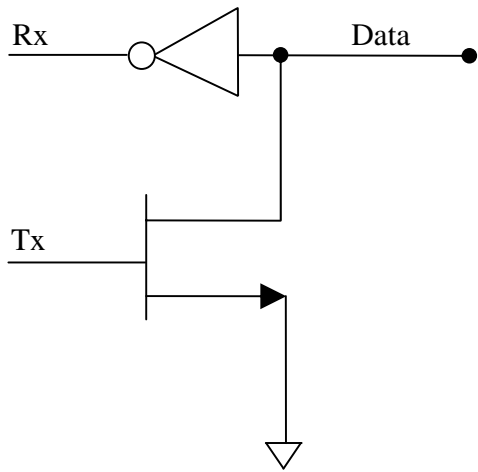
The Smart-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the Smart-Wire bus must have an open-drain connection or 3-state outputs. The SMC1990 is an open-drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pullup resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3.

The value of the pullup resistor should be approximately $5k\Omega$ for short line lengths. A multidrop bus consists of a Smart-Wire bus with multiple slaves attached. The Smart-Wire bus has a maximum data rate of 16.3kbits per second. The idle state for the Smart-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than $120\mu s$, one or more of the devices on the bus may be reset.

SMC1990 MEMORY MAP Figure 1

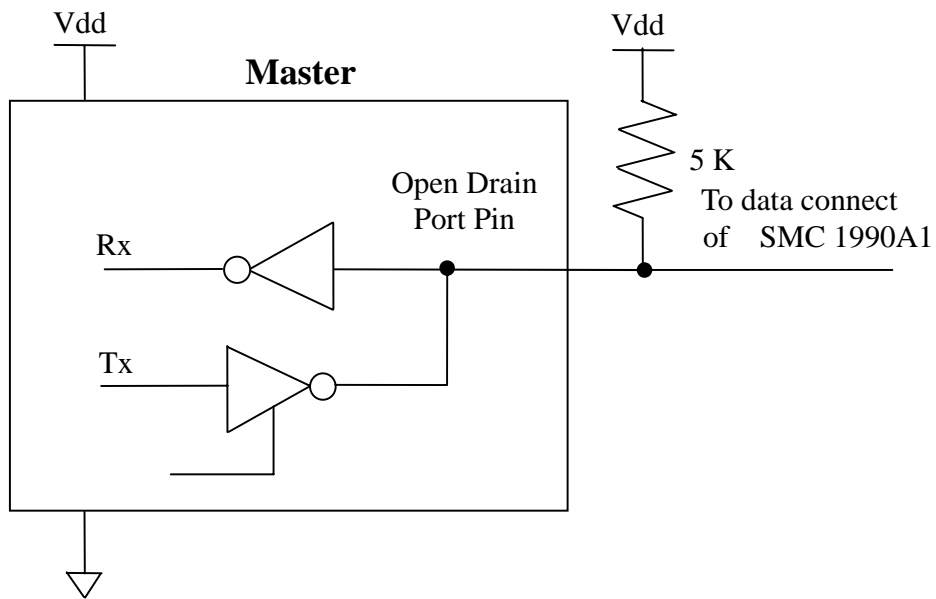
8-Bit CRC Code	48-Bit Serial Number	8-Bit Family Code (01h)
MSB	LSB MSB	LSB MSB
		LSB

SMC1990A1 EQUIVALENT CIRCUIT Figure 2

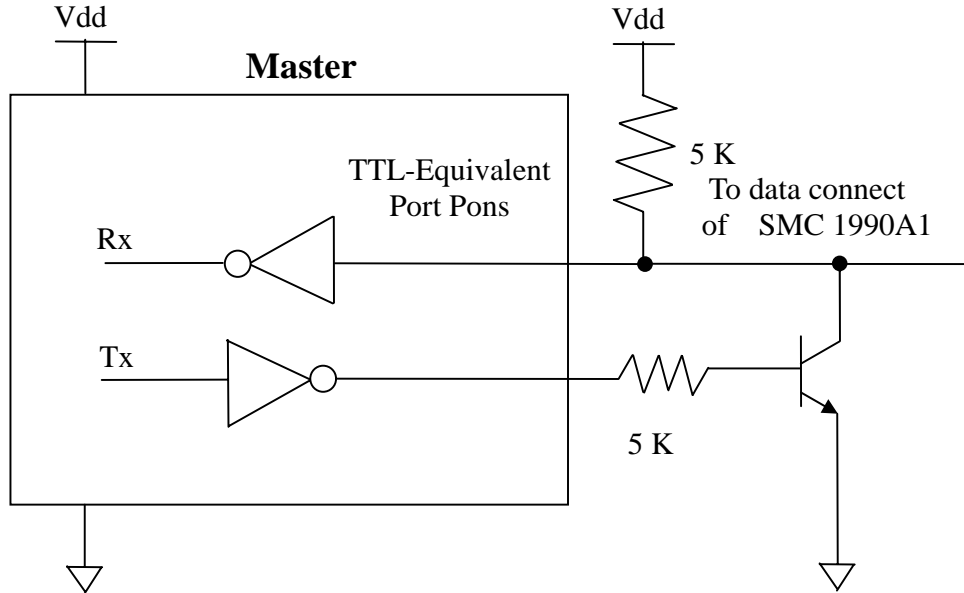


BUS MASTER CIRCUIT Figure 3

(A) Open Drain



(B) Standard TTL



TRANSACTION SEQUENCE

The sequence for accessing the SMC1990 via the Smart-Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the Smart-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a Presence Pulse(s) transmitted by the slave(s). The Presence Pulse lets the bus master know that the SMC1990 is on the bus and is ready to operate.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure4).

Read ROM [33h] or [0Fh]

This command allows the bus master to read the SMC1990's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single SMC1990 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The SMC1990 Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the Dallas Series.

Smart-Wire SIGNALING

The SMC1990 requires a strict protocol to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1, and read data. All these signals except Presence Pulse are initiated by the bus master.

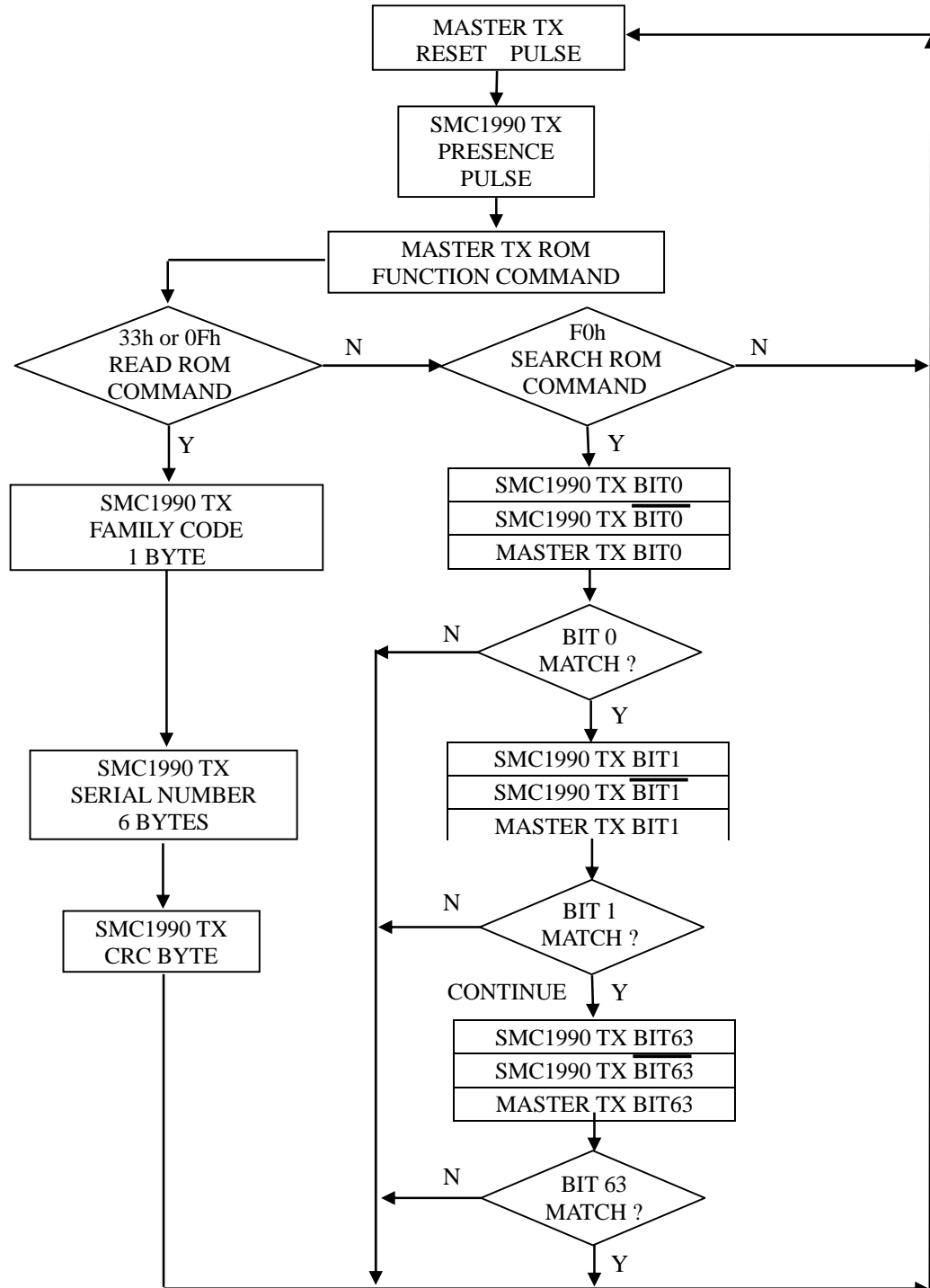
The initialization sequence required to begin any communication with the SMC1990 is shown in Figure 5. A reset pulse followed by a Presence Pulse indicates the SMC1990 is ready to send or receive data given the correct ROM command.

The bus master transmits (TX) a reset pulse (t_{RSTL} , minimum $480 \mu s$). The bus master then releases the line and goes into receive mode (RX). The Smart-Wire bus is pulled to a high state via the $5k\Omega$ pullup resistor. After detecting the rising edge on the data pin, the SMC1990 waits (t_{PDH} , $15-60 \mu s$) and then transmits the Presence Pulse (t_{PDL} , $60-240 \mu s$). The Smart-Wire bus requires a pullup resistor range of $1.5k\Omega$ to $5k\Omega$, depending on bus load characteristics.

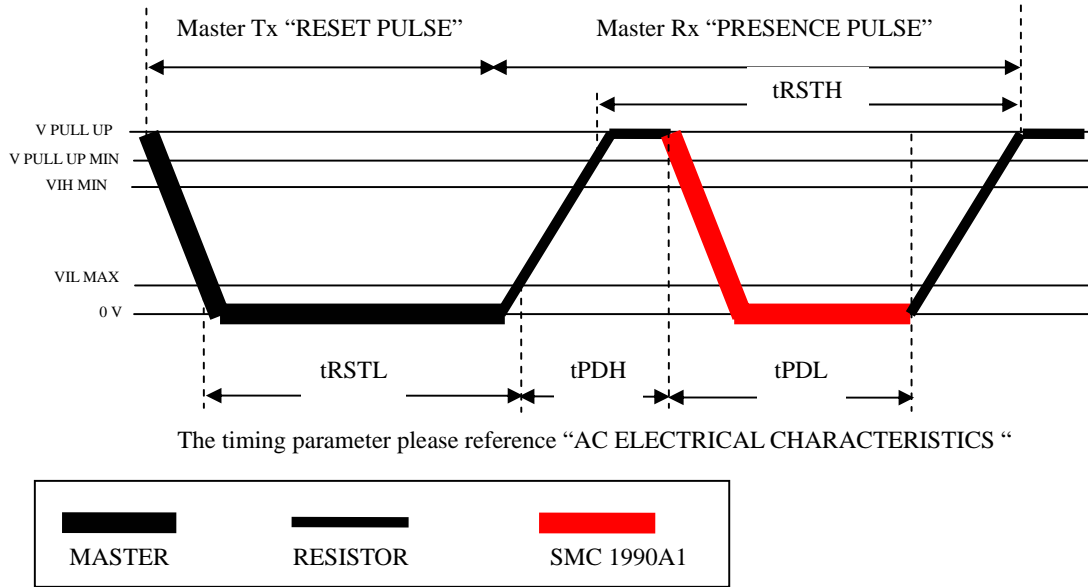
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the SMC1990 to the master by triggering a delay circuit in the SMC1990. During write time slots, the delay circuit determines when the SMC1990 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the SMC1990 will hold the data line low overriding the "1" generated by the master. If the data bit is a 1, the SMC1990 will leave the read data time slot unchanged.

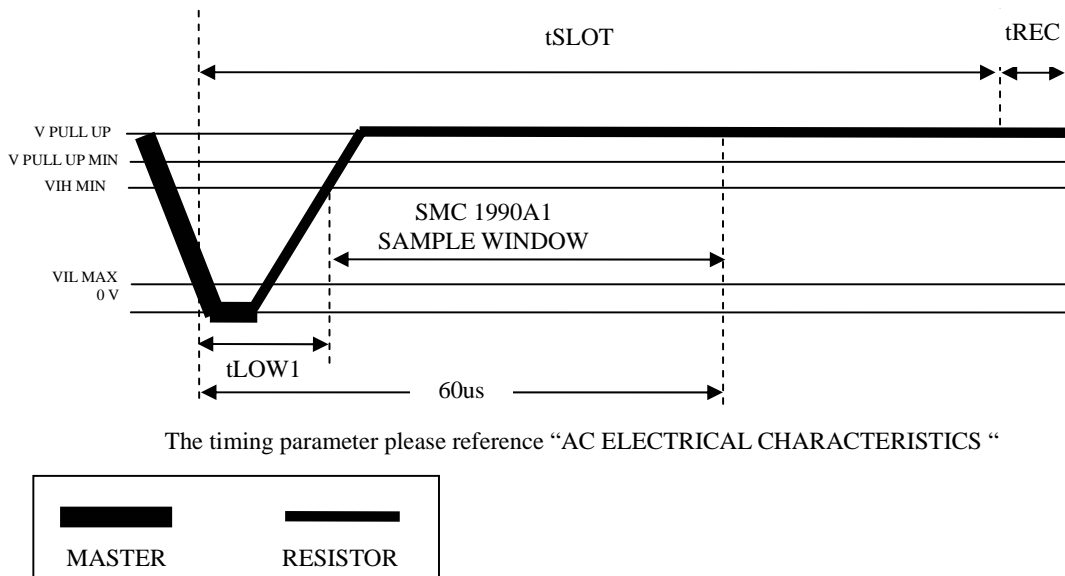
ROM FUNCTIONS FLOW CHART Figure 4



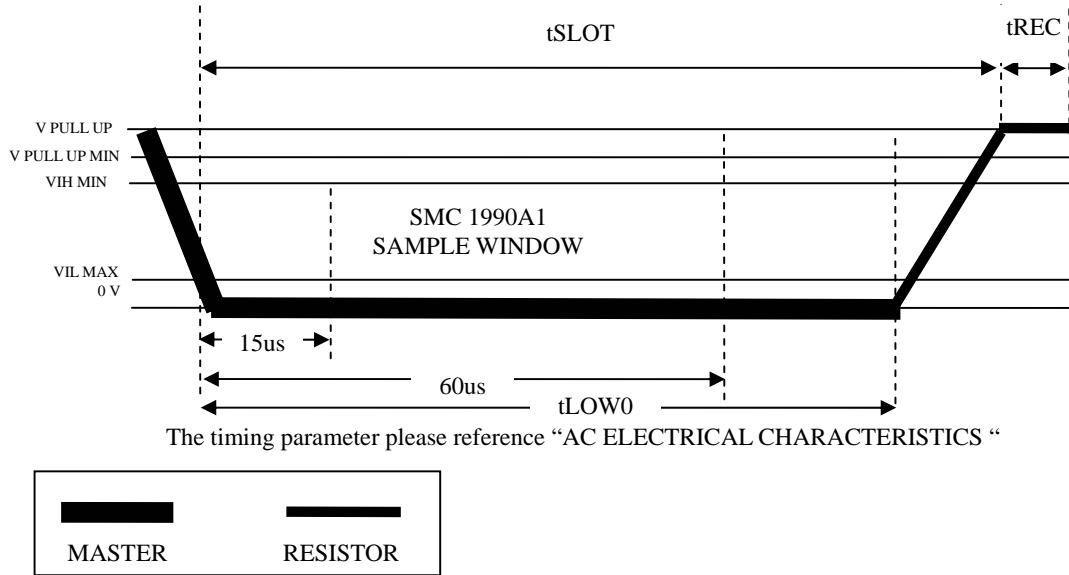
INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 5



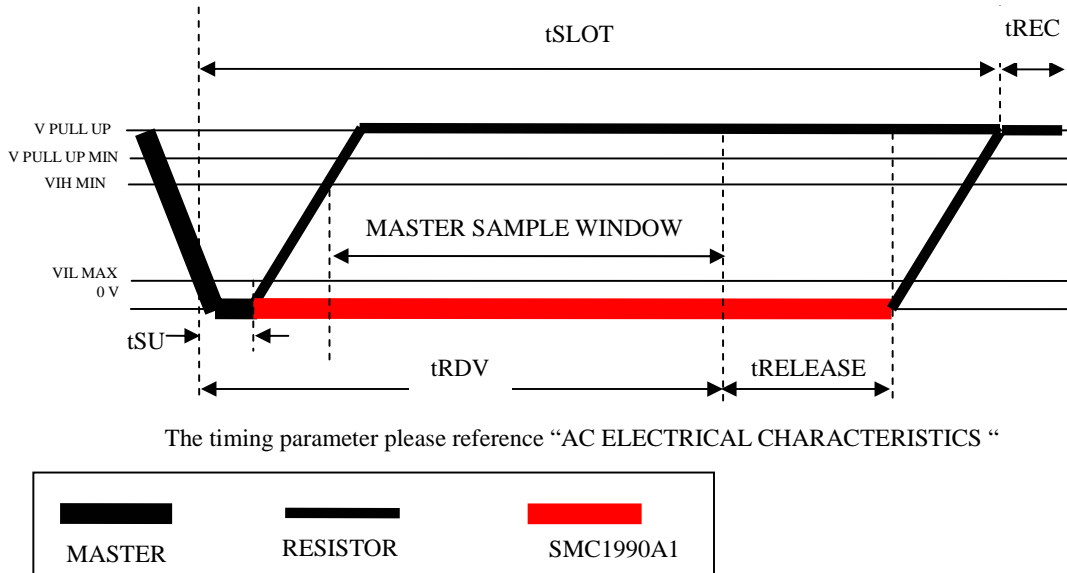
Write-One Time Slot Figure 6



Write-Zero Time Slot Figure 7



Read-data Time Slot Figure 8



CRC GENERATION

To validate the data transmitted from the SMC1990, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last 8 bits of the SMC1990. If the two CRC values match, the transmission is error-free.

The equivalent polynomial function of this CRC is: $CRC = x^8 + x^5 + x^4 + 1$.

CUSTOM SMC 1990A1

Customization of a portion of the unique 48-bit serial number by the customer is available. SMC Microelectronics Corp. will register and assign a specific customer ID in the 12 most significant bits of the 48-bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non-selectable and will be automatically incremented by one. Certain quantities and conditions apply for these custom parts. Contact your SMC Microelectronics Corp. sales representative for more information.

ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin relative to Ground	-0.5 V	to	+7.0 V
Operating Temperature	-40 C	to	+85 C
Storage Temperature	-55 C	to	+125 C

- This is a stress rating only and functional operation of the device at these or any any conditions above those indicated in the operation sections of this specification is not implied . Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (VPUP=3.3V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1	VIH	2.2		VCC +0.3	V
Logic 0	VIL	-0.3		+0.8	V
Output Logic Low	VOL			0.4	V
Output Logic High	VOH		VPUP	6.0	V

AC ELECTRICAL CHARACTERISTICS (VPUP=3.3V to 6.0V; -40°C to 85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Time Slot	tSLOT	60		120	μs
Write 1 Low Time	tLOW1	1		15	μs
Write 0 Low Time	tLOW0	60		120	μs
Read Data Valid	tRDV	15 (Exactly)			μs
Release Time	tRELEASE	0	15	45	μs
Read Data Setup	tSU			1	μs
Recovery Time	tREC	1			μs
Reset Time High	tRSTH	480			μs
Reset Time Low	tRSTL	480			μs
Presence Detect High	tPDH	15		60	μs
Presence Detect Low	tPDL	60		200	μs

— end —