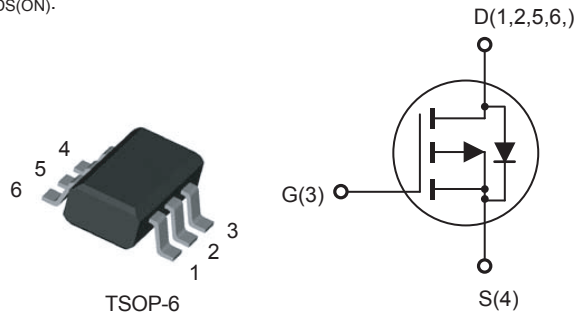


## P-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

### FEATURES

- -20V, -5.2A,  $R_{DS(ON)} = 48m\Omega$  @  $V_{GS} = -4.5V$ .
  - $R_{DS(ON)} = 60m\Omega$  @  $V_{GS} = -2.5V$ . □
  - $R_{DS(ON)} = 78m\Omega$  @  $V_{GS} = -1.8V$ . □
- High dense cell design for extremely low  $R_{DS(ON)}$ .
- Rugged and reliable.
- Lead free product is acquired.
- TSOP-6 package.



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	-5.2	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	-21	A
Maximum Power Dissipation	$P_D$	2.0	W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

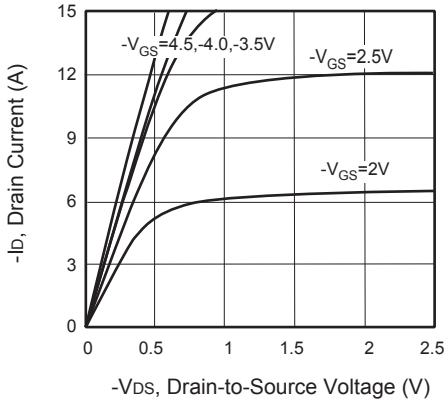
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$



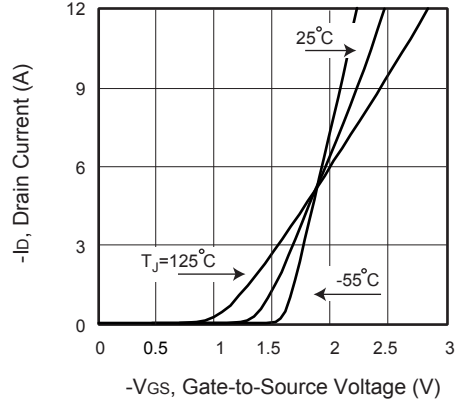
# CEH2331

## Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

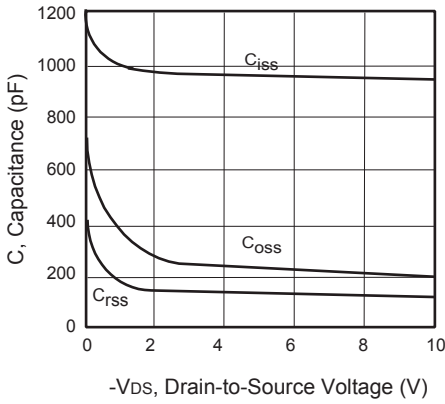
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 100$	nA
<b>On Characteristics</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	-0.4		-1	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -3.3A$		36	48	$m\Omega$
		$V_{GS} = -2.5V, I_D = -2.8A$		46	60	$m\Omega$
		$V_{GS} = -1.8V, I_D = -2A$		60	78	$m\Omega$
<b>Dynamic Characteristics <sup>d</sup></b>						
Forward Transconductance	$g_{FS}$	$V_{DS} = -5V, I_D = -4A$		13		S
Input Capacitance	$C_{iss}$	$V_{DS} = -10V, V_{GS} = 0V, f = 1.0\text{ MHz}$		965		pF
Output Capacitance	$C_{oss}$			200		pF
Reverse Transfer Capacitance	$C_{rss}$			155		pF
<b>Switching Characteristics <sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10V, I_D = -4A, \square$ $V_{GS} = -4.5V, R_{GEN} = 3\Omega$		15	30	ns
Turn-On Rise Time	$t_r$			10	20	ns
Turn-Off Delay Time	$t_{d(off)}$			40	80	ns
Turn-Off Fall Time	$t_f$			13	26	ns
Total Gate Charge	$Q_g$	$V_{DS} = -10V, I_D = -4A, V_{GS} = -4.5V$		13	17	nC
Gate-Source Charge	$Q_{gs}$			2.5		nC
Gate-Drain Charge	$Q_{gd}$			3		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				-5.2	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = -1A$			-1.2	V
<b>Notes :</b> $\square$ a. Repetitive Rating : Pulse width limited by maximum junction temperature. $\square$ b. Surface Mounted on FR4 Board, $t \leq 5\text{ sec.}$ $\square$ c. Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . $\square$ d. Guaranteed by design, not subject to production testing. $\square$ $\square$						



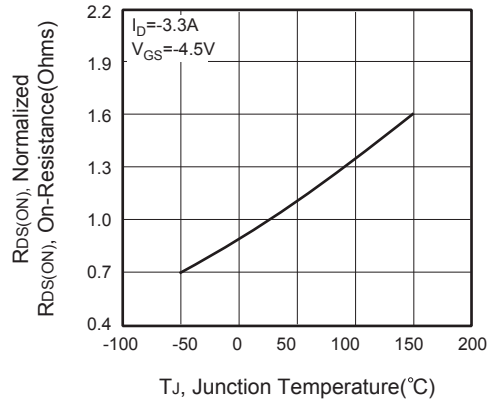
**Figure 1. Output Characteristics**



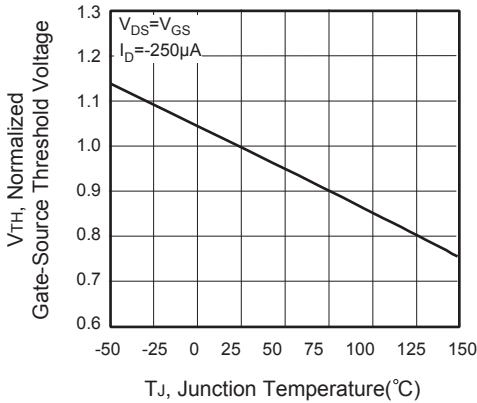
**Figure 2. Transfer Characteristics**



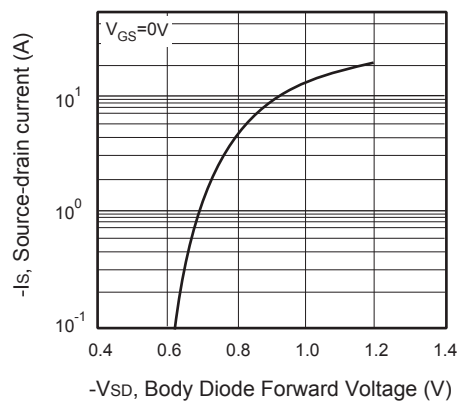
**Figure 3. Capacitance**



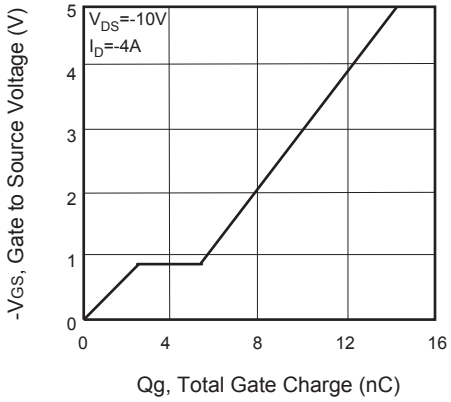
**Figure 4. On-Resistance Variation with Temperature**



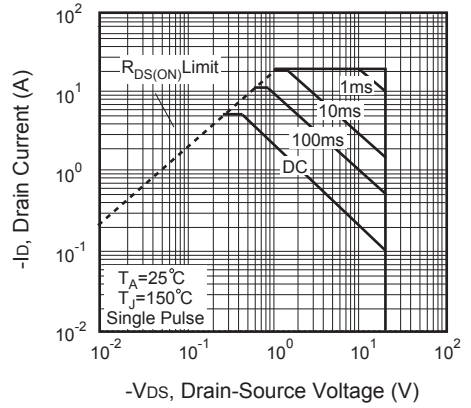
**Figure 5. Gate Threshold Variation with Temperature**



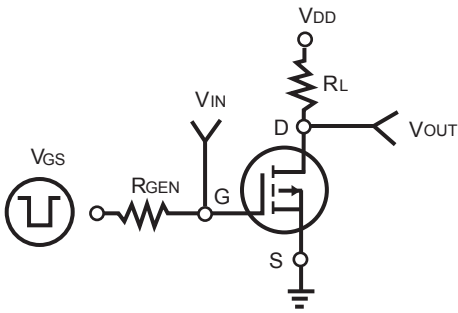
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



**Figure 7. Gate Charge**



**Figure 8. Maximum Safe Operating Area**



**Figure 9. Switching Test Circuit**



**Figure 10. Switching Waveforms**

