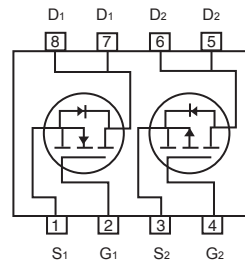
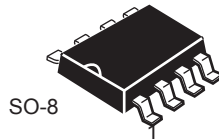


## Dual Enhancement Mode Field Effect Transistor (N and P Channel)

### FEATURES

- 40V, 6.1A,  $R_{DS(ON)} = 32m\Omega$  @ $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 46m\Omega$  @ $V_{GS} = 4.5V$ .
- -40V, -4.3A,  $R_{DS(ON)} = 66m\Omega$  @ $V_{GS} = -10V$ .  
 $R_{DS(ON)} = 105m\Omega$  @ $V_{GS} = -4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- Surface mount Package.



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### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	$V_{DS}$	40	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Drain Current-Continuous	$I_D$	6.1	-4.3	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	24	-17	A
Maximum Power Dissipation	$P_D$	2.0		W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$



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## N-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>c</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6.1A$		25	32	$m\Omega$
		$V_{GS} = 4.5V, I_D = 4.9A$		35	46	$m\Omega$
<b>Dynamic Characteristics<sup>d</sup></b>						
Forward Transconductance	$g_{FS}$	$V_{DS} = 5V, I_D = 6.1A$		3		S
Input Capacitance	$C_{iss}$	$V_{DS} = 20V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1050		pF
Output Capacitance	$C_{oss}$			155		pF
Reverse Transfer Capacitance	$C_{rss}$			95		pF
<b>Switching Characteristics<sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20V, I_D = 6.1A, V_{GS} = 10V, R_{GEN} = 3\Omega$		14	30	ns
Turn-On Rise Time	$t_r$			10	20	ns
Turn-Off Delay Time	$t_{d(off)}$			17	35	ns
Turn-Off Fall Time	$t_f$			18	35	ns
Total Gate Charge	$Q_g$	$V_{DS} = 20V, I_D = 6.1A, V_{GS} = 4.5V$		10.1	13	nC
Gate-Source Charge	$Q_{gs}$			3.5		nC
Gate-Drain Charge	$Q_{gd}$			4.0		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				6.1	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 1.0A$			1.0	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . d.Guaranteed by design, not subject to production testing.						



## P-Channel Electrical Characteristics $T_A = 25\text{ C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -40V, V_{GS} = 0V$			-1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics <sup>c</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -4.3A$		55	66	$m\Omega$
		$V_{GS} = -4.5V, I_D = -3.7A$		85	105	$m\Omega$
<b>Dynamic Characteristics <sup>d</sup></b>						
Forward Transconductance	$g_{FS}$	$V_{DS} = -5V, I_D = -4.3A$		7		S
Input Capacitance	$C_{iss}$	$V_{DS} = -20V, V_{GS} = 0V, f = 1.0\text{ MHz}$		705		pF
Output Capacitance	$C_{oss}$			125		pF
Reverse Transfer Capacitance	$C_{rss}$			75		pF
<b>Switching Characteristics <sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 6\Omega$		13	26	ns
Turn-On Rise Time	$t_r$			3	6	ns
Turn-Off Delay Time	$t_{d(off)}$			31	62	ns
Turn-Off Fall Time	$t_f$			5	10	ns
Total Gate Charge	$Q_g$	$V_{DS} = -20V, I_D = -4.3A, V_{GS} = -4.5V$		5.6	7.4	nC
Gate-Source Charge	$Q_{gs}$			2.1		nC
Gate-Drain Charge	$Q_{gd}$			2.3		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				-4.3	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = -1.3A$			-1.2	V
<b>Notes :</b> <input type="checkbox"/> a.Repetitive Rating : Pulse width limited by maximum junction temperature. <input type="checkbox"/> b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec.}$ <input type="checkbox"/> c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . <input type="checkbox"/> d.Guaranteed by design, not subject to production testing. <input type="checkbox"/> <input type="checkbox"/>						



## N-CHANNEL

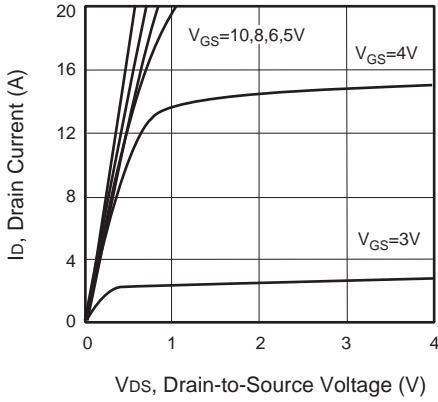


Figure 1. Output Characteristics

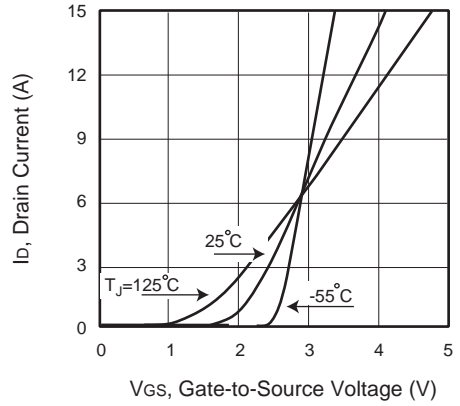


Figure 2. Transfer Characteristics

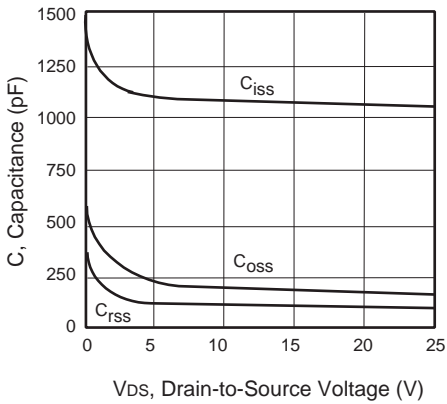


Figure 3. Capacitance

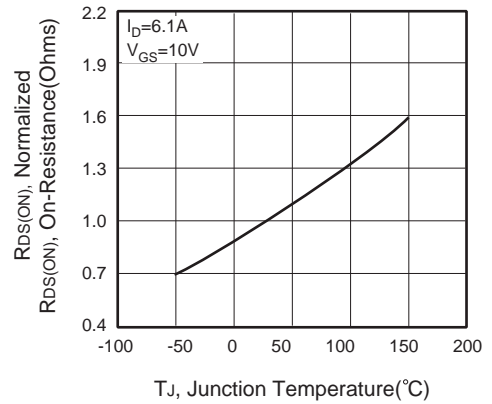


Figure 4. On-Resistance Variation with Temperature

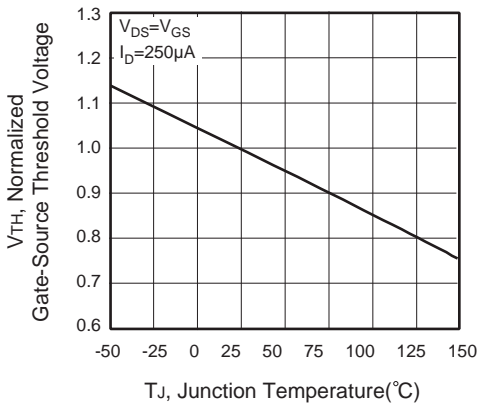


Figure 5. Gate Threshold Variation with Temperature

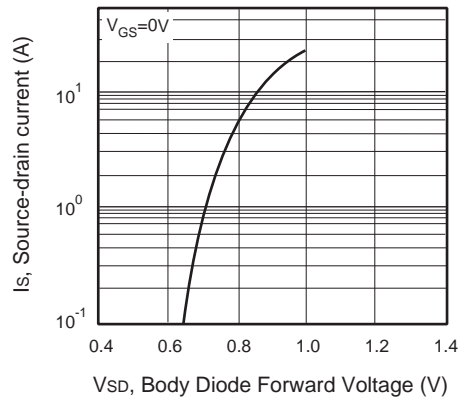


Figure 6. Body Diode Forward Voltage Variation with Source Current



# CEM4279

## P-CHANNEL

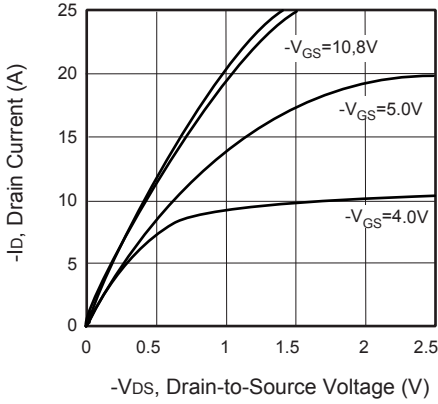


Figure 1. Output Characteristics

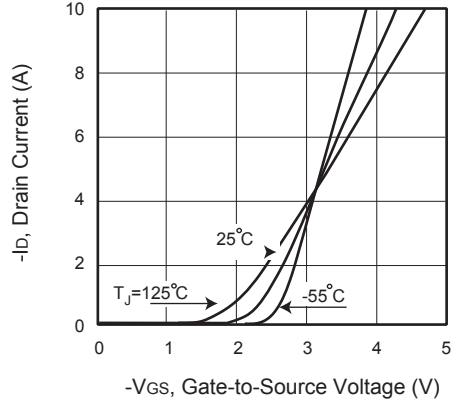


Figure 2. Transfer Characteristics

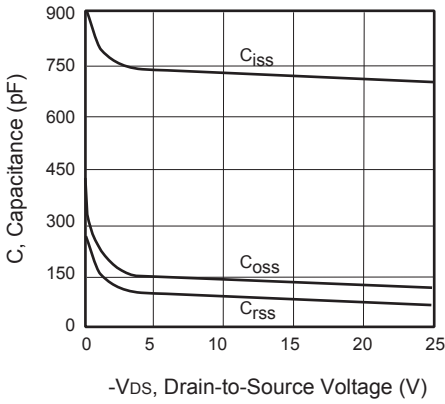


Figure 3. Capacitance

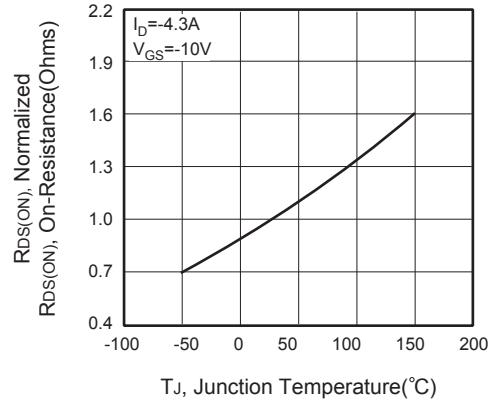


Figure 4. On-Resistance Variation with Temperature

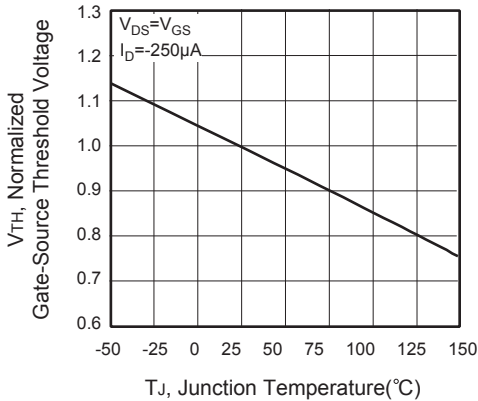


Figure 5. Gate Threshold Variation with Temperature

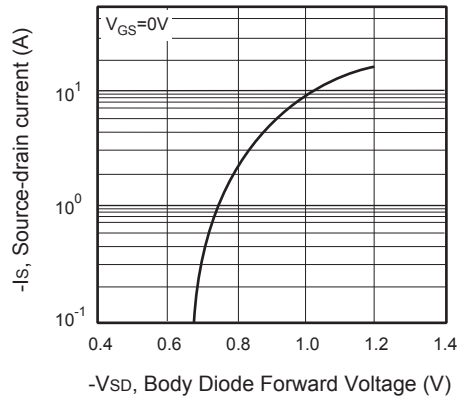


Figure 6. Body Diode Forward Voltage Variation with Source Current



## N-CHANNEL

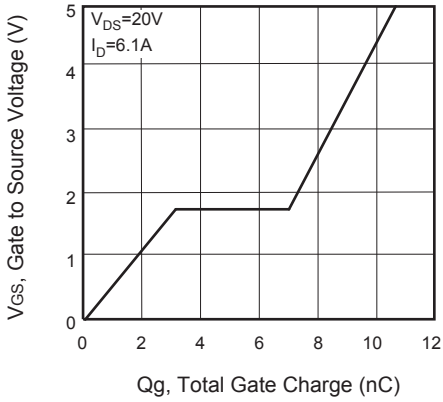


Figure 13. Gate Charge

## P-CHANNEL

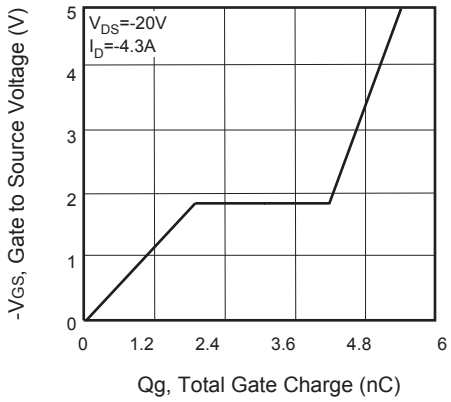


Figure 15. Gate Charge

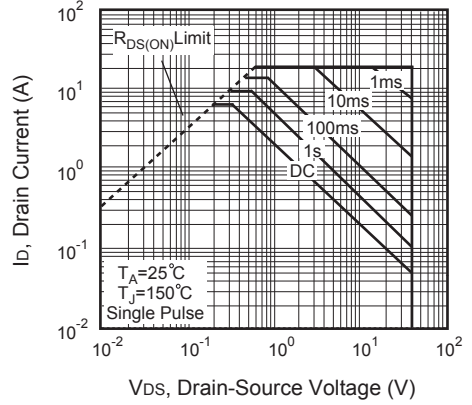


Figure 14. Maximum Safe Operating Area

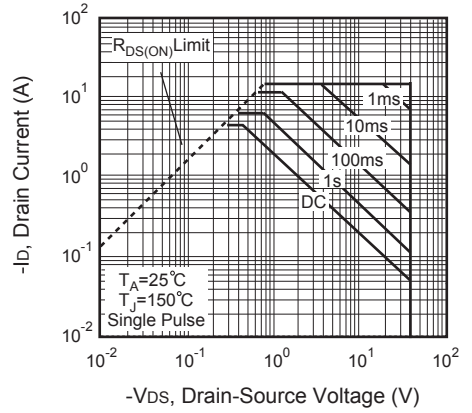


Figure 16. Maximum Safe Operating Area

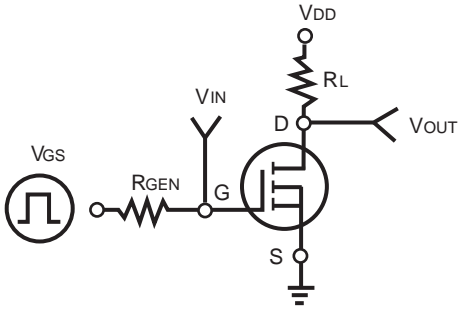


Figure 17. Switching Test Circuit

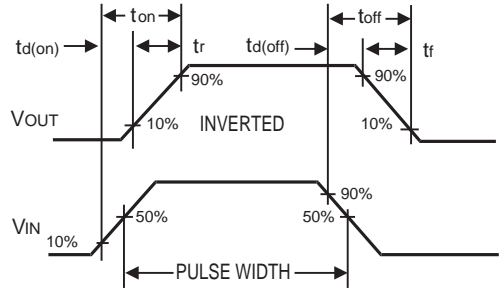


Figure 18. Switching Waveforms

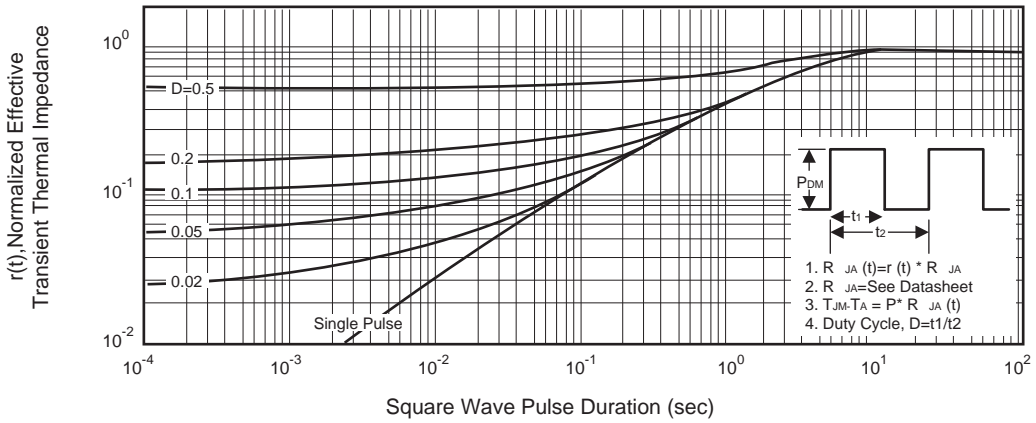


Figure 19. Normalized Thermal Transient Impedance Curve