SHANGHAI SIPROIN MICROELECTRONICS Co.,LTD.

PolyPhase Energy Metering

SSP1852 Specification

DATA：2021/09/10

VERSION：1.3

WEB：http://WWW.SIPROIN.COM

Catalogue

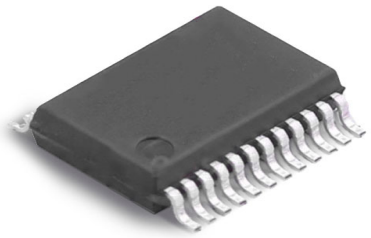
1.GENERAL DESCRIPTION

The SSP1852 is a high accuracy polyphase electrical energy measurement IC. The part specifications surpass the accuracy requirements as quoted in the IEC62053-2x standard. The only analog circuitry used in the SSP1852 is in the analog-to-digital converters (ADCs) and reference circuit. All other signal processing (such as multi-plication, filtering, and summation) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The SSP1852 supplies average real power information on the low frequency outputs, F1 and F2. These logic outputs may be used to directly drive an electromechanical counter or to interface with an MCU. The CF logic output gives instanta-neous real power information. This output is intended to be used for calibration purposes.

The SSP1852 includes a power supply monitoring circuit on the VDD pin. The SSP1852 remains inactive until the supply voltage on VDD reaches 4 V. If the supply falls below 4 V, no pulses are issued on F1, F2, and CF. Internal phase matching circuitry ensures that the voltage and current channels are phase matched. An internal no load threshold ensures the part does not exhibit any creep when there is no load.

The SSP1852 is available in a 24-lead SOIC package.



2.FEATURES

- High accuracy, supports 50 Hz/60 Hz IEC62053-2x
- Less than 0.1% error over a dynamic range of 500 to 1
- Compatible with 3-phase/3-wire delta and 3-phase/4-wire Wye configurations
- The SSP1852 supplies average real power on frequency outputs F1 and F2
- High frequency output CF is intended for calibration and supplies instantaneous real power
- Logic output REVP indicates a potential miswiring or negative power for each phase
- Direct drive for electromechanical counters and 2-phase stepper motors (F1 and F2)
- Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time
- On-chip power supply monitoring
- On-chip creep protection (no load threshold)
- On-chip reference 2.4 V ±8% (30 ppm/°C typical) with external overdrive capability
- Single 5 V supply, low power 33 mW typical
- Low cost CMOS process

3. Order information

product model	package	manner of packing	Minimum packing quantity
SSP1852-SOP24	SOP24	Tube	30PCS

4.PIN DESCRIPTION

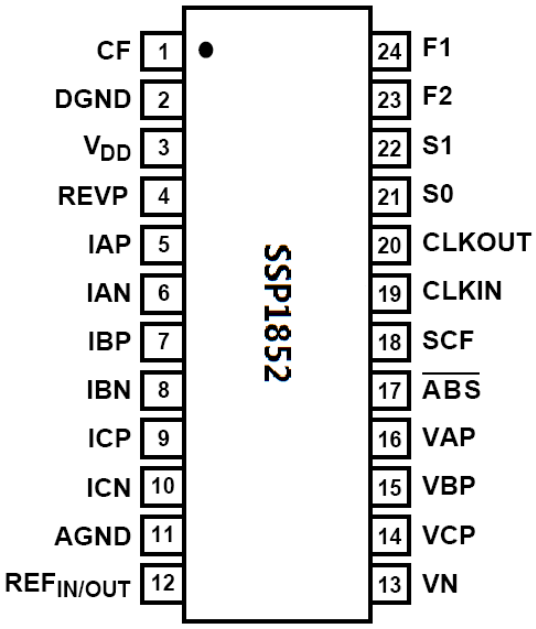


Figure 1. Pin Configuration

Pin No.	Mnemonic	Description
1	CF	Calibration Frequency Logic Output. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. See the SCF pin description.
2	DGND	This provides the ground reference for the digital circuitry: the multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the SSP1852 are small, it is acceptable to connect this pin to the analog ground plane of the whole system.
3	VDD	Power Supply. This pin provides the supply voltage for the digital circuitry in the SSP1852. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a 100 nF ceramic capacitor.
4	REVP	This logic output goes logic high when negative power is detected on any of the three phase inputs, that is, when the phase angle between the voltage and the current signals is greater than 90°. This output is not latched and is reset when positive power is once again detected. See the Negative Power Information section.
5,6 7,8 9,10	IAP,IAN IBP,IBN ICP,ICN	Analog Inputs for Current Channel. This channel is intended for use with the current transducer and is referenced in this document as the current channel. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V. Both inputs have internal ESD protection circuitry. In addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.

11	AGND	This pin provides the ground reference for the analog circuitry: the ADCs, temperature sensor, and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system.
12	REFIN/OUT	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.4 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor.
13-16	VN,VCP,VBP, VAP	Analog Inputs for the Voltage Channel. This channel is intended for use with the voltage transducer and is referenced in this document as the voltage channel. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation.
17	$\overline{ABS}$	This logic input is used to select the way the three active energies from the three phases are summed. This offers the designer the capability to do the arithmetical sum of the three energies ($\overline{ABS}$ logic high) or the sum of the absolute values ($\overline{ABS}$ logic low).
18	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table 1 shows how the calibration frequencies are selected.
19，20	CLKIN，CLKOUT	A crystal can be connected across CLKIN and CLKOUT to provide a clock source for the SSP1852. The clock frequency for specified operation is 10 MHz. Ceramic load capacitors between 22 pF and 33 pF should be used with the gate oscillator circuit.
21,22	S0,S1	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conver-sion. This offers the designer greater flexibility when designing the energy meter. See the Selecting a Frequency for an Energy Meter Application section.
23,24	F2，F1	Low Frequency Logic Outputs. F1 and F2 supply average real power information. The logic outputs can be used to drive electromechanical counters and two-phase stepper motors directly.

5.ABSOLUT MAXIMUM

Parameter	Rating
VDD to AGND	−0.3 V to +7 V
VDD to DGND	−0.3 V to +7 V
Analog Input Voltage to AGND (VAP, VBP, VCP, VN, IAP, IAN, IBP, IBN, ICP, and ICN)	−6 V to +6 V
Reference Input Voltage to AGND	−0.3 V to V + 0.3 V DD

Digital Input Voltage to DGND	−0.3 V to V + 0.3 V DD
Digital Output Voltage to DGND	−0.3 V to V + 0.3 V DD
Operating Temperature Range	−40°C to +85°C
Industrial	
Storage Temperature Range	−40°C to +85°C
Junction Temperature	150°C
24-Lead SOIC, Power Dissipation	450 mW
θJA Thermal Impedance	250°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

6.SPECIFICATIONS

（VDD = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz, TMIN to TMAX = –40°C to +85°C, unless otherwise noted.）

Parameter	Value	Unit	Conditions
ACCURACY			
Measurement Error on Current Channel	0.1	%Reading typ	Voltage channel with full-scale signal (±500 mV), 25°C, over a dynamic range of 500 to 1
Phase Error Between Channels			Line frequency 50~60Hz
PF = 0.8Capacitive	±0.1	Degrees	
PF = 0.5Inductive	±0.1	Degrees	
AC Power Supply Rejection			SCF=0,S1=S0=1，
Output Frequency Variation(CF)	0.2	%Reading typ	IA=IB=IC=100mVrms，50Hz VA=VB=VC=100mVrms，50Hz ripple on VDD of 175 mV rms，100Hz
DC Power Supply Rejection			S1=1，S0=SCF=0
Output Frequency Variation(CF)	±0.3	%Reading typ	IA=IB=IC=100mV rms，50Hz VA=VB=VC=100mVrms，50Hz VDD =5V±250mV
ANALOG INPUTS			
Maximum Signal Levels	±0.5	Vmax	VA,VB,VC,IA,IB,IC to GND
Input Impedance (DC)	390	kΩ min	CLKOSC=10MHz
Bandwidth(-3dB)	14	kHz typ	CLKOSC/256，CLKOSC=10MHz
ADC Offset Error	±16	mV max	
Gain Error	±9	%Ideal typ	External 2.5V reference IAP=IBP=ICP=500mV ， dc
ON-CHIP REFERENCE			Nominal 2.5V
Reference Error	±200	mV max	

Temperature Coefficient	30	ppm/°C typ	
CLKIN Input Clock Frequency	 12 8	 MHz max MHz min	All specifications for CLKIN of 10 MHz
LOGIC INPUTS SCF,S0,S1 and $\overline{ABS}$			
Input High Voltage,V_{INH}	2.4	V min	VDD=5V±5%
Input Low Voltage,V_{INL}	0.8	V max	VDD=5V±5%
Input Current,I_{IN}	±3	μA max	Typically 10nA,V_{IN}=0V to VDD
Input Capacitance,C_{IN}	10	pF max	
LOGIC OUTPUT F1 and F2			
Output High Voltage,V_{OH}	4.5	V min	I_{SOURCE}=10mA，VDD=5V
Output Low Voltage,V_{OL}	0.5	V max	I_{SINK}=10mA，VDD=5V
CF and REVP			
Output High Voltage,V_{OH}	4	V min	I_{SOURCE}=10mA，VDD=5V
Output Low Voltage,V_{OL}	0.5	V max	I_{SINK}=10mA，VDD=5V
POWER SUPPLY			For specified performance
VDD	4.75	V min	5V-5%
	5.25	V max	5V+5%
I_{DD}	8	mA max	
	5	mA min	Typically 6.5mA

7.TIMING CHARACTERISTICS

（VDD = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz, TMIN to T= –40°C to +85°C, unless otherwise noted.）

Parameter	Spec	Unit	Conditions
T_1	275	ms	F1 and F2 Pulse Width (Logic High).
T_2	See Table 1	s	Output Pulse Period. See the Transfer Function section.
T_3	1/2 T_2	s	Time between F1 Falling Edge and F2 Falling Edge.
T_4	96	ms	CF Pulse Width (Logic High).
T_5	See Table 1	s	CF Pulse Period. See the Transfer Function and the Frequency Outputs sections.
T_6	CLKOSC/4	s	Minimum Time Between the F1 and F2 Pulse.

注: (1) The pulse widths of F1, F2, and CF are not fixed for higher output frequencies. See the Frequency Outputs section.

(2) CF is not synchronous to F1 or F2 frequency outputs.

(3)The CF pulse is always 1 μs in the high frequency mode.

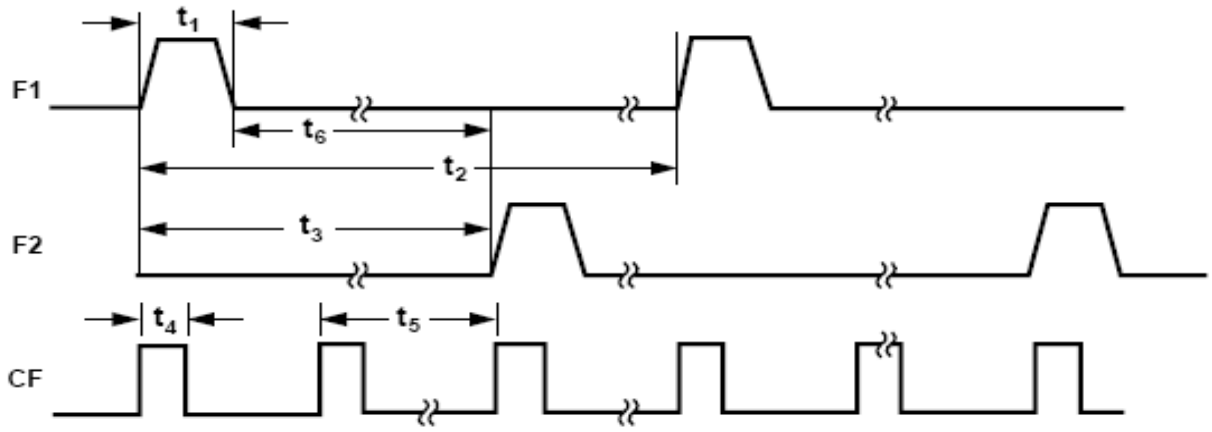


Figure 2. Timing Diagram for Frequency Outputs

8.OUTPUT PULSE SETTING

Table 1 Maximum Output Frequency on CF

SCF	S1	S0	$F_{1\sim7}$ (Hz)	CF Max for AC Signal(Hz)	Counter Rating (C=metering constant)
0	0	0	1.27	160×F1,F2=81.87	C/80
1	0	0	1.19	8×F1,F2=3.83	C/4
0	0	1	5.09	160×F1,F2=327.46	C/80
1	0	1	4.77	16×F1,F2=30.70	C/8
0	1	0	19.07	16×F1,F2=122.81	C/8
1	1	0	19.07	8×F1,F2=61.40	C/4
0	1	1	76.29	8×F1,F2=245.61	C/4
1	1	1	0.6	16×F1,F2=3.84	C/8

Table 2 Reference setting for SCF,S0 and S1

Max Current（A）	Rating of CTs	Sampling Resistor（Ω）	Metering constant	Rating Of Counter	SCF		S0		S1	
					0	1	0	1	0	1
					J1	J2	J3	J4	J5	J6
10 (for 1.5~6.0 2.5~10.0)	300:1	10	1600	200		●		●		●
		10		400		●	●		●	
		15*	3200	400		●		●		●
		15*		800		●	●		●	
50 (for 10~40 20~50)	1000:1	5.1	160	20		●		●		●
		5.1		40		●	●		●	
		6	320	40		●		●		●
		6		80		●	●		●	

		9.1	400	50		●		●		●
		9.1		100		●	●		●	
100 (for 15~60 20~80 20~100)	1000:1	3	160	20		●		●		●
		3		40		●	●		●	
		4.7	320	40		●		●		●
		4.7		80		●	●		●	
	2000:1	6.2	160	20		●		●		●
		6.2		40		●	●		●	
		9.1	320	40		●		●		●
		9.1		80		●	●		●	

*refer to maximum load resistor of CTs

9.OUTLINE DIMENSIONS

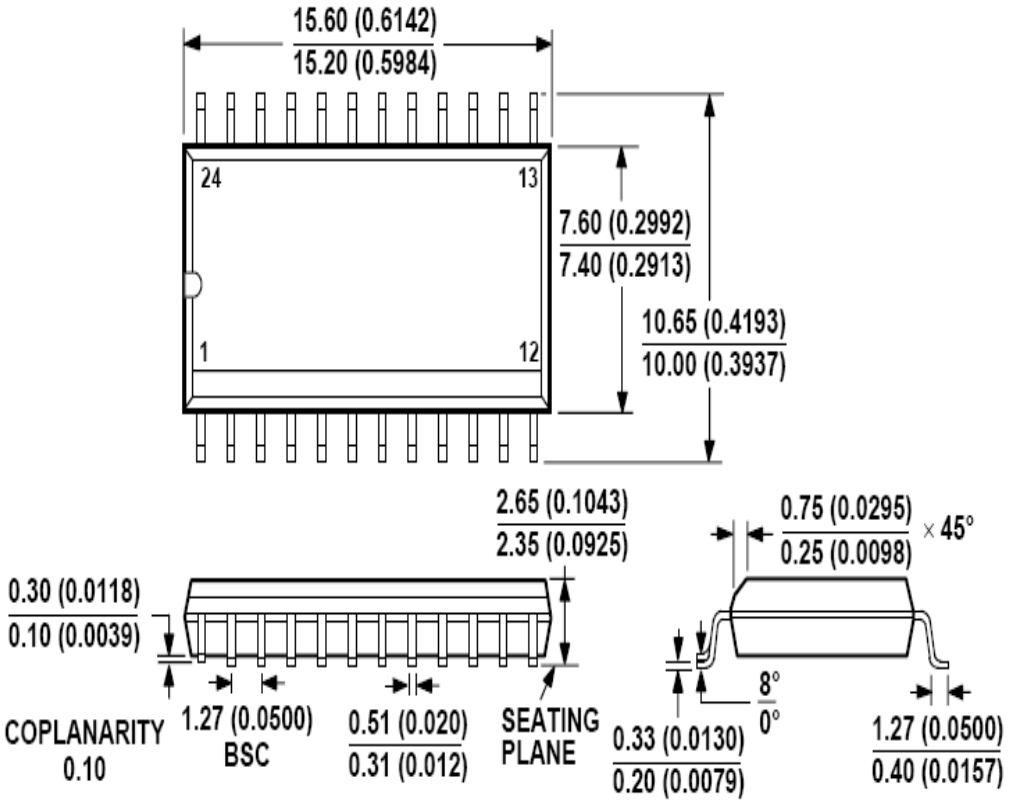


Figure 3. SOP-24 Wide Body

10.Typical Application

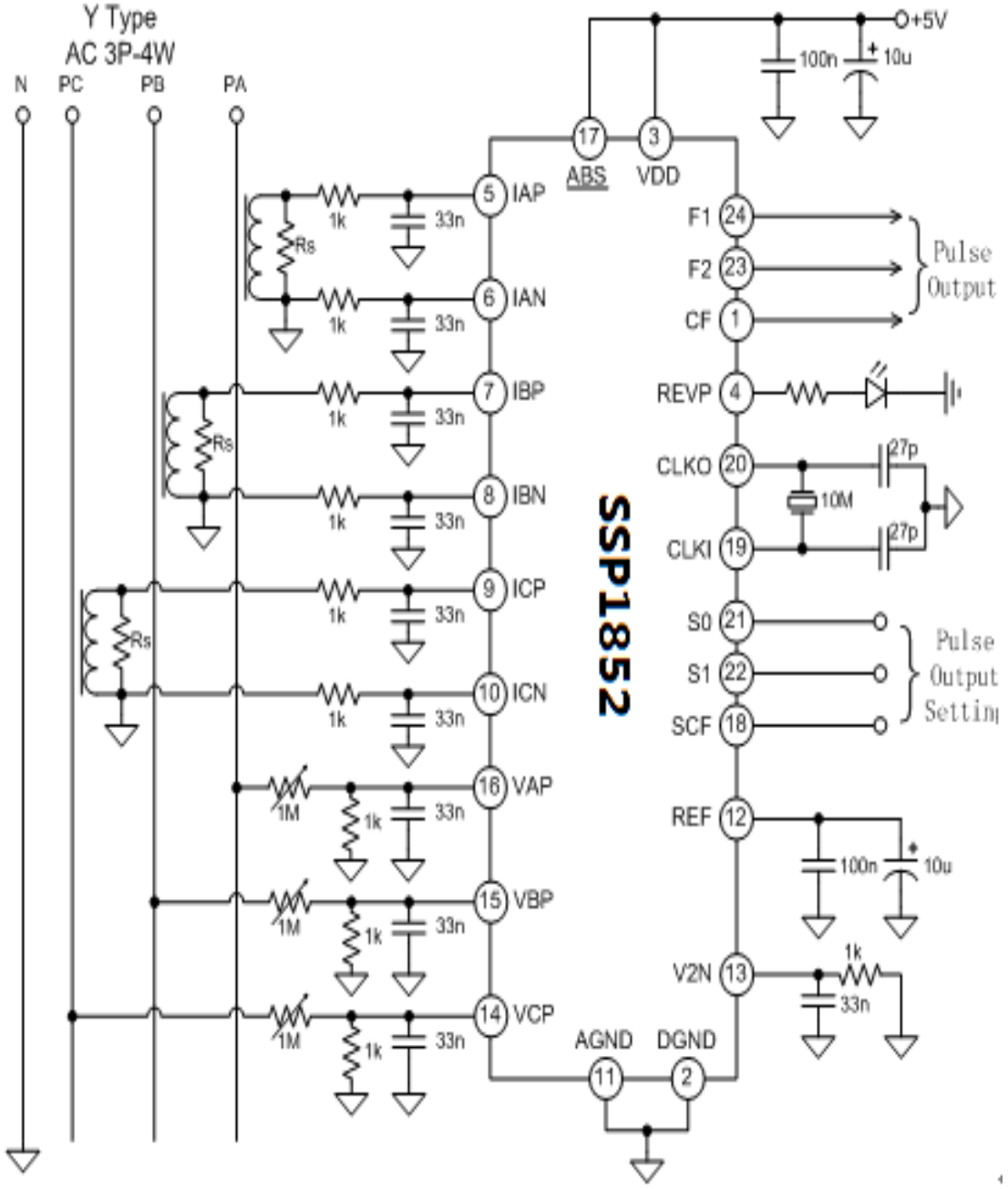


Figure 3. Typical Application Circuit

11.ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

SPECIAL EXPLANATION

The final interpretation right of this specification belongs to our company.

DESCRIPTION OF VERSION CHANGE

VERSION:V1.3 Author：Lifeng Liu Data：2021.9.15

Amendment record:

1. Re-layout the specifications and check some data.