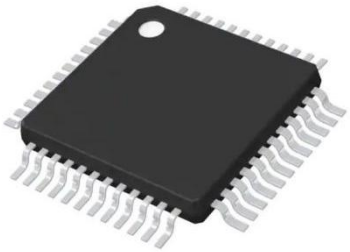
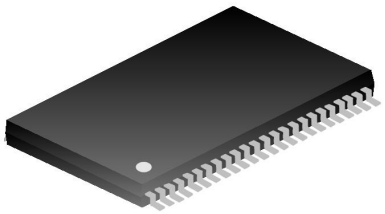
Standard LCD Segment Drivers

SSP55080

General Description

SSP55080 is a general LCD driver IC with 8COMx35SEG total output capacity of 280 bits, suitable for commonly used character/graphic LCD screens. SSP55080 support serial data interface(I^2C).





Features

- Integrated RAM 35*8=280Bit
- Integrated reset circuit
- Integrated Oscillation circuit
- Integrated Power supply circuit for LCD driving:
  1/4 Bias, 1/8 Duty
- Integrated Buffer AMP
- LCD drive output:
  8 Common output, 35 Segment output
- I^2C serial data interface
- Integrated Electrical volume register (EVR) function
- Low power consumption design
- Excellent EMC immunity
- Supply Voltage Range:2.5V~5.5V
- LCD drive power supply Range: 2.5V~5.5V
- Package：TSSOP48, LQFP48

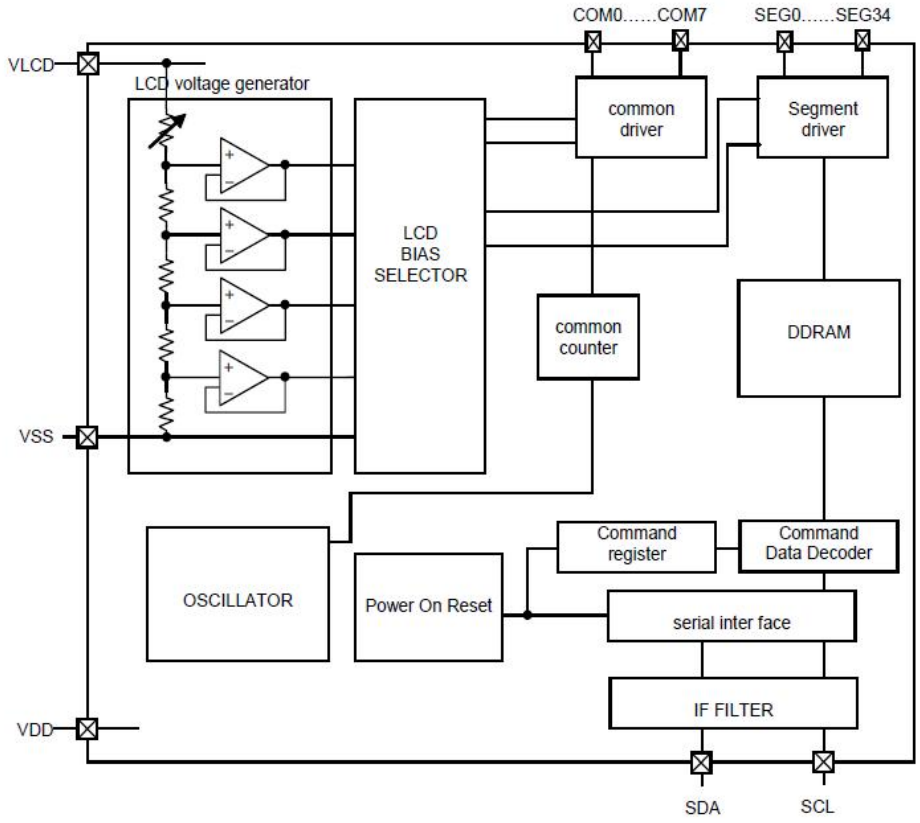
Applications

- Power Meter, Water meter, Gas Meter, phone
- FAX
- Home electrical appliance
- Toy
- Industrial instrument

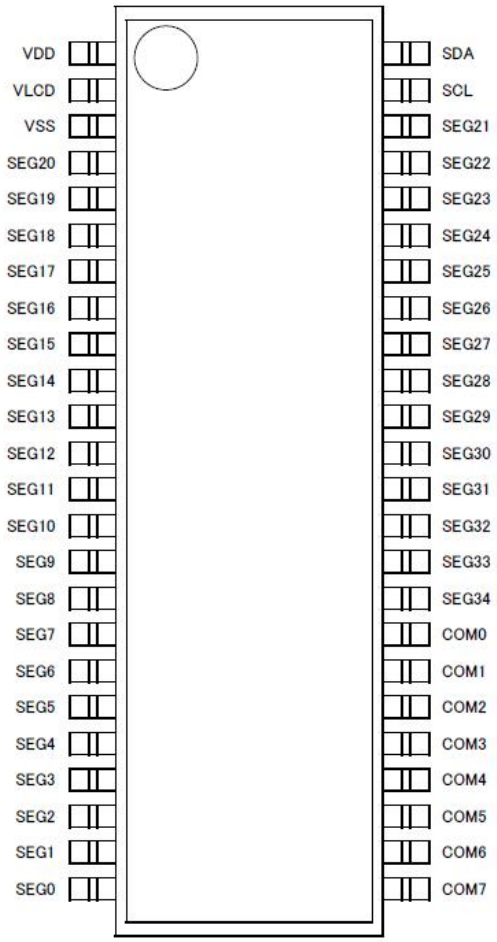
Order specification

Part No	Package	Manner of Packing	Devices per bag/reel
SSP55080AFV	TSSOP48	Reel	2500
SSP55080AKV	LQFP48	Tray	250

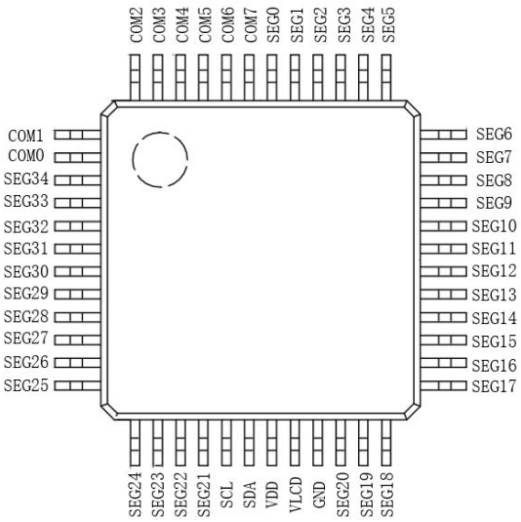
Block Diagram



Pin Arrangement Diagram



TSSOP48



LQFP48

Pin Assignment

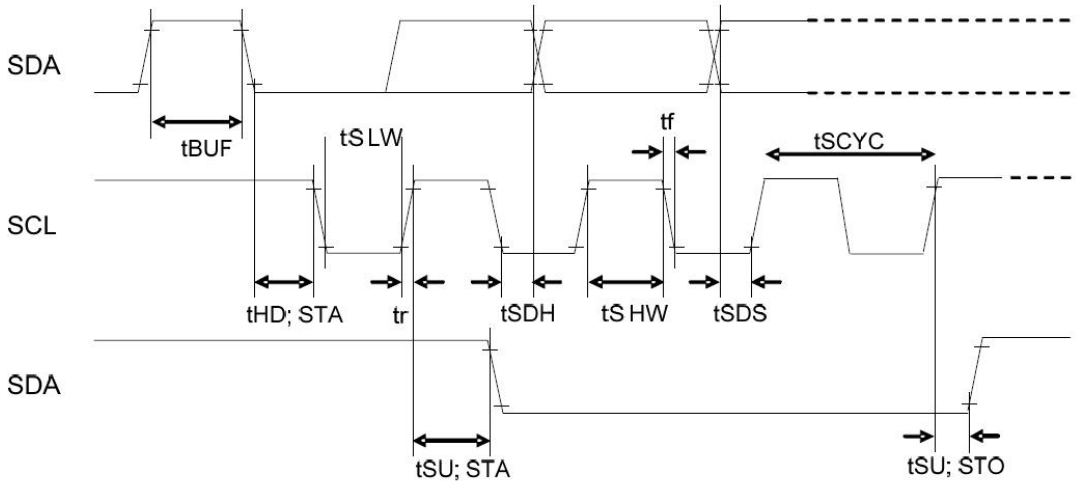
Terminal No.		Terminal	I/O	Function
TSSOP48	LQFP48			
4-24 33-46	3-16 22-42	SEG0~34	O	SEGMENT output for LCD drive
25-32	1-2 43-48	COM0~7	O	COMMON output for LCD drive
2	20	VLCD	I	Power supply for LCD drive
1	19	VDD	I	Power supply
3	21	VSS	I	GND
47	17	SCL	I	I^2C Serial data transfer clock
48	18	SDA	I/O	I^2C Serial data input

Electrical Characteristics

（VDD=3.3V, VLCD=5V, VSS=0, EVR=8, Ta=25℃）

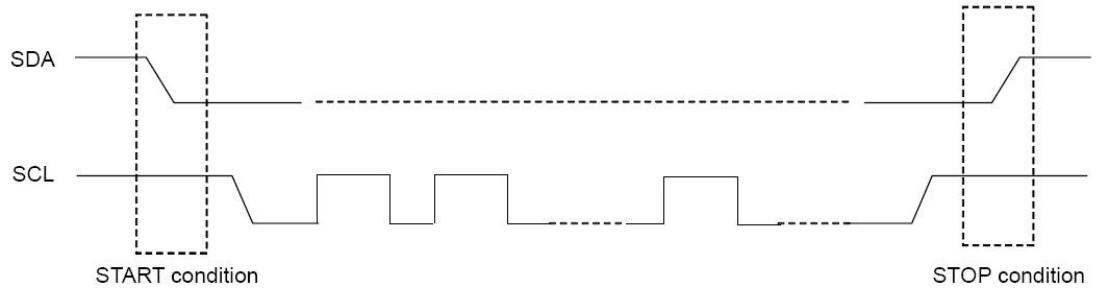
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply	VDD	---	2.5	---	5.5	V
Power Supply for LCD driving	VLCD	---	2.5	---	5.5	V
Standby current	I_{ST}	Display off Oscillation off	---	---	0.5	μA
Power consumption	I_{DD}	VDD=3.3V, VLCD=5V, FR=80HZ, T=25℃, 1/4bias, FRAME inversion	---	2	5	μA
LCD Power consumption	I_{LCD}	VDD=3.3V, VLCD=5V, FR=80HZ, T=25℃, 1/4bias, FRAME inversion	---	6	10	μA
Frame frequency	FCLK	VDD=3.3V, FR=80HZ	60	80	110	HZ
I^2C “H” level input voltage	V_{IH}	SDA, SCL	0.6VDD	---	VDD	V
I^2C “L” level input voltage	V_{IL}	SDA, SCL	VSS	---	0.3VDD	V
I^2C “H” level input current	I_{IH}	SDA, SCL	---	---	1	μA
I^2C “L” level input current	I_{IL}	SDA, SCL	-1	---	---	μA
LCD Driver on resistance	R_{ONSEG}	SEG I_{load} = ±10μA	---	3.5	---	kΩ
	R_{ONCOM}	COM I_{load} = ±10μA	---	3.5	---	kΩ
Input rise time	tr	---	---	---	0.3	μs
Input fall time	tf	---	---	---	0.3	μs
SCL cycle time	tSCYC	---	2.4	---	---	μs
“H” SCL pulse width	tSHW	---	0.6	---	---	μs
“L” SCL pulse width	tSLW	---	1.2	---	---	μs
SDA setup time	tSDS	---	100	---	---	ns
SDA hold time	tSDH	---	100	---	---	ns
Bus free time	tBUF	---	1.3	---	---	μs
START condition hold time	tHD;STA	---	0.6	---	---	μs
START condition setup time	tSU;STA	---	0.6	---	---	μs
STOP condition setup time	tSU;STO	---	0.6	---	---	μs

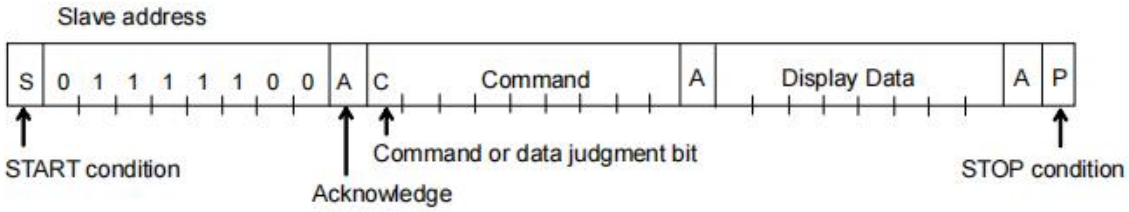
Sequence Diagram



Command /Data transfer method

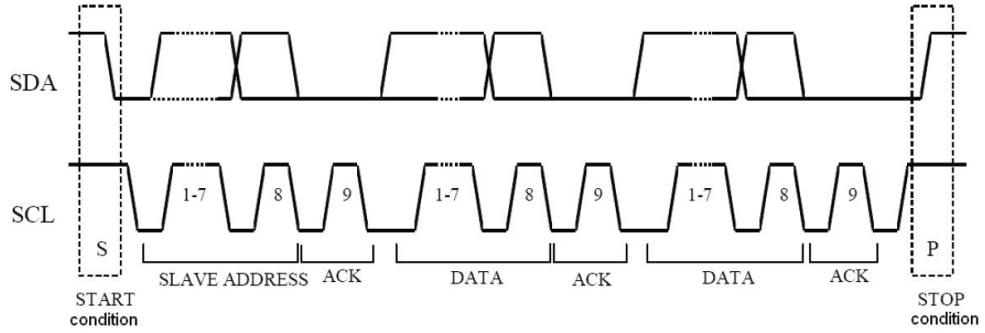
SSP55080 is controlled by 2wire serial signal. The basic steps are to generate “start condition”, then issue Slave address (01111100), transfer command,display data and generate “STOP condition”.





- **Acknowledge**

Data format is 8bits and return Acknowledge after transfer 8bits data.When SCL 8th =’L’ after transfer 8bit data (Slave Address, Command, Display Data), output open SDA line. When SCL 9th =’L’ , stop output function. If no need Acknowledge function, Please input ’L’ level from SCL 8th=’L’ to SCL 9th=’L’ .

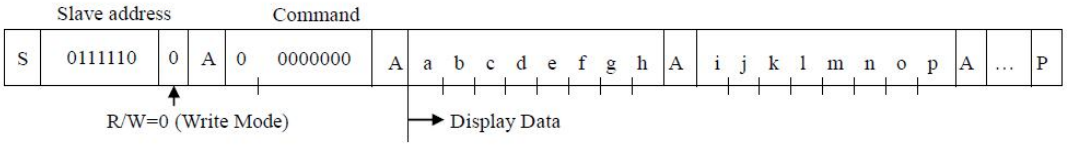


- **Command transfer method**

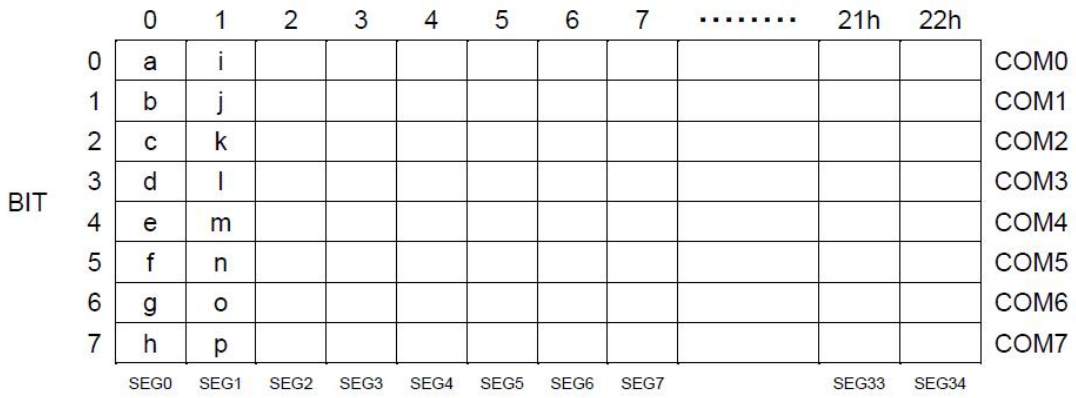
Command input follows after the Slave Address.When “Command or data judgement bit”=’1’, the next byte is a command. When “Command or data judegment bit”=’0’, the nexit byte is display data.Once it enters display data transfer condition, it cannot input any command.To input command again, please generate the “START condition” again.

- **Write display and transfer method**

SSP55080 has Display Data RAM(DDRAM) of 35 × 8=280bits. Write mode happens when R/W bit=’0’.The relationship between data input and display data, DDRAM data and address are as follows.



The 8-bit display data will be stored in the DDRAM. The address to be written is the address specified by Address Set command, and the address is automatically incremented after every 8-bits of data.Data can be continuously written in the DDRAM by transmitting data continuously.



Control Command

D7 is bit for command or data judgement.

C=0, indicates that the next byte (D7 to D0) is write data. C=1, indicates that the next byte is command.

The SSP55080 contains five control command bytes. Both command and data are sent as bytes to SSP55080. The five command bytes for SSP55080 are listed below.

	Command	Function
1	Address set(ADSET)	DDRAM address setting(00h~22h)
2	EVR set(EVRSET)	EVR setting(0~31)
3	Display Control(DISCTL)	Fram Frequency,Power save mode setting
4	IC operation set(ICSET)	LCD drive mode,software reset,display on/off
5	All pixe Control(APCTL)	All pixel control during display ON

- **Address Set**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Default Value	C	0	0	0	0	0	0	0

D5~D0: Address set addr[5:0]

Address range：000000~100010

- **EVR Set（Electrical volume register Set）**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Default Value	C	1	0	0	0	0	1	0

D4~D0: EVR setting.The relationships of electrical volume register setting and V0 voltage:

EVR	Calculation formula	VLCD=5.500	VLCD=5.000	VLCD=4.000	VLCD=3.500	VLCD=3.000	VLCD=2.500	[V]
0	VLCD	V0=5.500	V0=5.000	V0=4.000	V0=3.500	V0=3.000	V0=2.500	[V]
1	0.967*VLCD	V0=5.323	V0=4.839	V0=3.871	V0=3.387	V0=2.903	V0=2.419	[V]
2	0.937*VLCD	V0=5.156	V0=4.688	V0=3.750	V0=3.281	V0=2.813	V0=2.344	[V]
3	0.909*VLCD	V0=5.000	V0=4.545	V0=3.636	V0=3.182	V0=2.727	V0=2.273	[V]
4	0.882*VLCD	V0=4.853	V0=4.412	V0=3.529	V0=3.088	V0=2.647	V0=2.206	[V]
5	0.857*VLCD	V0=4.714	V0=4.286	V0=3429	V0=3.000	V0=2.571	V0=2.143	[V]
6	0.833*VLCD	V0=4.583	V0=4.167	V0=3.333	V0=2.917	V0=2.500	V0=2.083	[V]
7	0.810*VLCD	V0=4.459	V0=4.054	V0=3.243	V0=2.838	V0=2.432	V0=2.027	[V]
8	0.789*VLCD	V0=4.342	V0=3.947	V0=3.158	V0=2.763	V0=2.368	V0=1.974	[V]
9	0.769*VLCD	V0=4.231	V0=3.846	V0=3.077	V0=2.692	V0=2.308	V0=1.923	[V]
10	0.750*VLCD	V0=4.125	V0=3.750	V0=3.000	V0=2.625	V0=2.250	V0=1.875	[V]
11	0.731*VLCD	V0=4.024	V0=3.659	V0=2.927	V0=2.561	V0=2.195	V0=1829	[V]
12	0.714*VLCD	V0=3.929	V0=3.571	V0=2.857	V0=2.500	V0=2.143	V0=1.786	[V]
13	0.697*VLCD	V0=3.837	V0=3.488	V0=2.791	V0=2.442	V0=2.093	V0=1.744	[V]
14	0.681*VLCD	V0=3.750	V0=3.409	V0=2.727	V0=2.386	V0=2.045	V0=1.705	[V]
15	0.666*VLCD	V0=3.667	V0=3.333	V0=2.667	V0=2.333	V0=2.000	V0=1.667	[V]
16	0.652*VLCD	V0=3.587	V0=3.261	V0=2.609	V0=2.283	V0=1.957	V0=1.630	[V]
17	0.638*VLCD	V0=3.511	V0=3.191	V0=2.553	V0=2.234	V0=1.915	V0=1.596	[V]
18	0.625*VLCD	V0=3438	V0=3.125	V0=2.500	V0=2.188	V0=1.875	V0=1.563	[V]
19	0.612"VLCD	V0=3.367	V0=3.061	V0=2.449	V0=2.143	V0=1.837	V0=1.531	[V]
20	0.600*VLCD	V0=3.300	V0=3.000	V0=2.400	V0=2.100	V0=1.800	V0=1.500	[V]
21	0.588*VLCD	V0=3235	V0=2.941	V0=2.353	V0=2.059	V0=1.765	V0=1.471	[V]
22	0.576*VLCD	V0=3.173	V0=2.885	V0=2.308	V0=2.019	V0=1.731	V0=1.442	[V]
23	0.566*VLCD	V0=3.113	V0=2.830	V0=2.264	V0=1.981	V0=1.698	V0=1.415	[V]
24	0.555*VLCD	V0=3.056	V0=2.778	V0=2.222	V0=1.944	V0=1.667	V0=1.389	[V]
25	0.545*VLCD	V0=3.000	V0=2.727	V0=2.182	V0=1.909	V0=1.636	V0=1.364	[V]

26	0.535*VLCD	V0=2.946	V0=2.679	V0=2.143	V0=1.875	V0=1.607	V0=1.339	[V]
27	0.526*VLCD	V0=2.895	V0=2.632	V0=2.105	V0=1.842	V0=1.579	V0=1.316	[V]
28	0.517*VLCD	V0=2845	V0=2.586	V0=2.069	V0=1.810	V0=1.552	V0=1.293	[V]
29	0.508*VLCD	V0=2.797	V0=2.542	V0=2.034	V0=1.780	V0=1.525	V0=1.271	[V]
30	0.500*VLCD	V0=2.750	V0=2.500	V0=2.000	V0=1.750	V0=1.500	V0=1.250	[V]
31	0.491*VLCD	V0=2.705	V0=2.459	V0=1.967	V0=1.721	V0=1.475	V0=1.230	[V]

Note: 1. ▬ Prohibited setting ; 2.Incase EVR using, please satisfy VLCD-V0>0.6V; 3.Do not use V0 < 2.5V area.

- **Display Control**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Default Value	C	1	1	0	0	0	1	0

D3~D2: frame frequency control

00: 80HZ

01: 70HZ

10: 64HZ

11: 50HZ

D1~D0:10 (power save mode control)

- **Set IC Operation**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Default Value	C	1	1	1	0	1	0	0

D2: Set LCD drive waveform
0：LINE inversion mode
1: FRAME inversion mode

D1: Set Software Reset condition
0: No operation
1: Software reset

D0: Set Display ON and OFF
0: Display OFF
1: Display ON

- **All Pixel Control**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Default Value	C	1	1	1	1	0	0	0

D1: all pixel ON control
0: normal
1: all pixel on

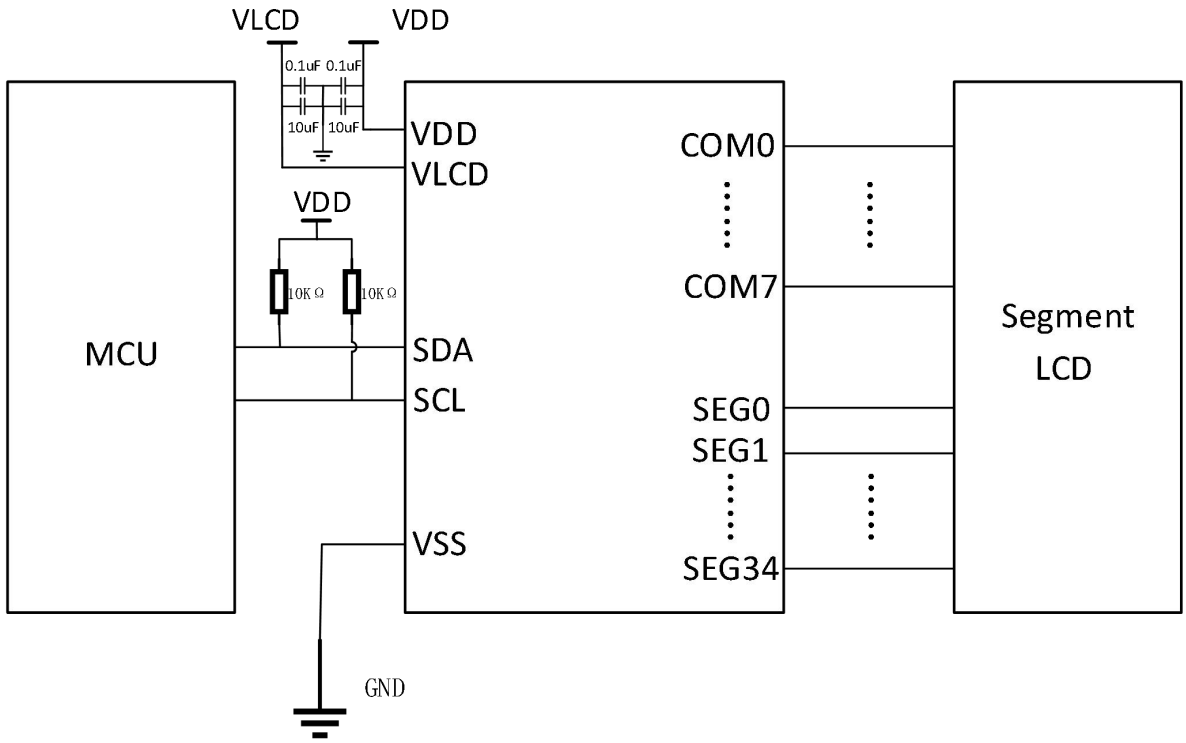
D0: all pixel OFF control
0: normal
1: all pixel off

Note：When D1 and D0=1, D0 is selected. D0 has higher priority than D1.

Start sequence example

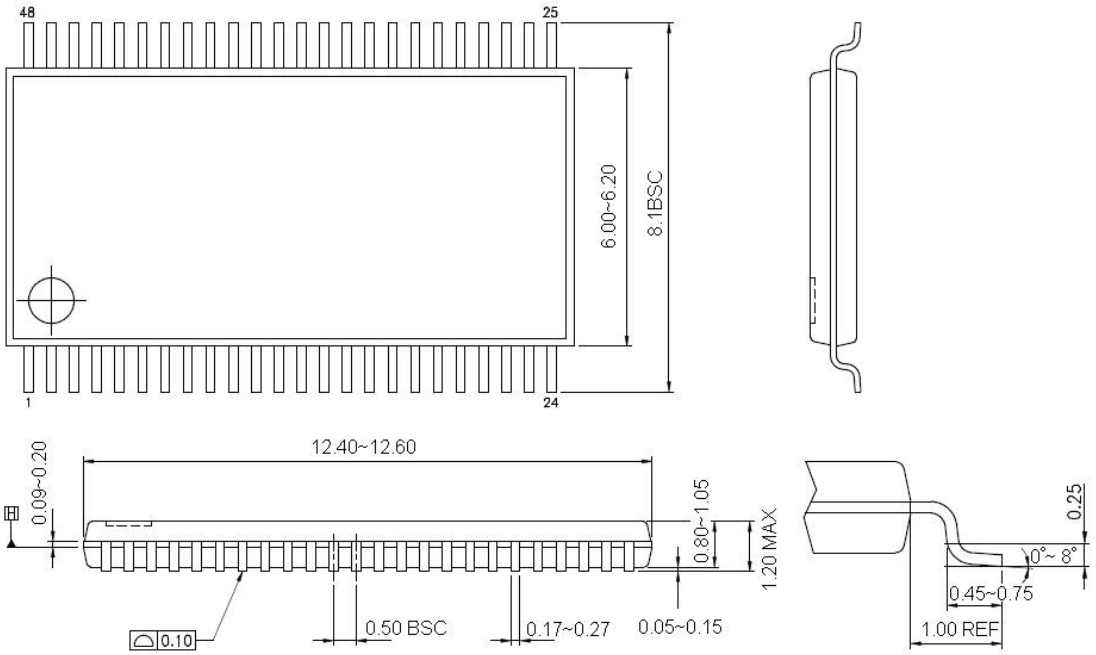
NO.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	Power on									VDD=0 to 5V(Tr=0.1ms)
	↓									
2	Wait 100us									Initialize IC
	↓									
3	Stop									Stop Condition
	↓									
4	Start									Start Condition
5	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
6	ICSET	1	1	1	1	0	*	1	*	Software Reset
	↓									
7	DISCTL	1	1	1	0	0	0	1	0	Unnecessary when initial value setup
	↓									(If you need to change the condition)
8	EVRSET	1	1	0	0	0	0	0	0	Unnecessary when initial value setup
	↓									(If you need to change the condition)
9	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	Address 00h
	...									...
	Display Data	*	*	*	*	*	*	*	*	Address 22h
	↓									
11	Stop									Start Condition
	↓									
12	Start									Start Condition
13	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
14	ICSET	1	1	1	1	0	*	0	1	Display ON

Application Circuits

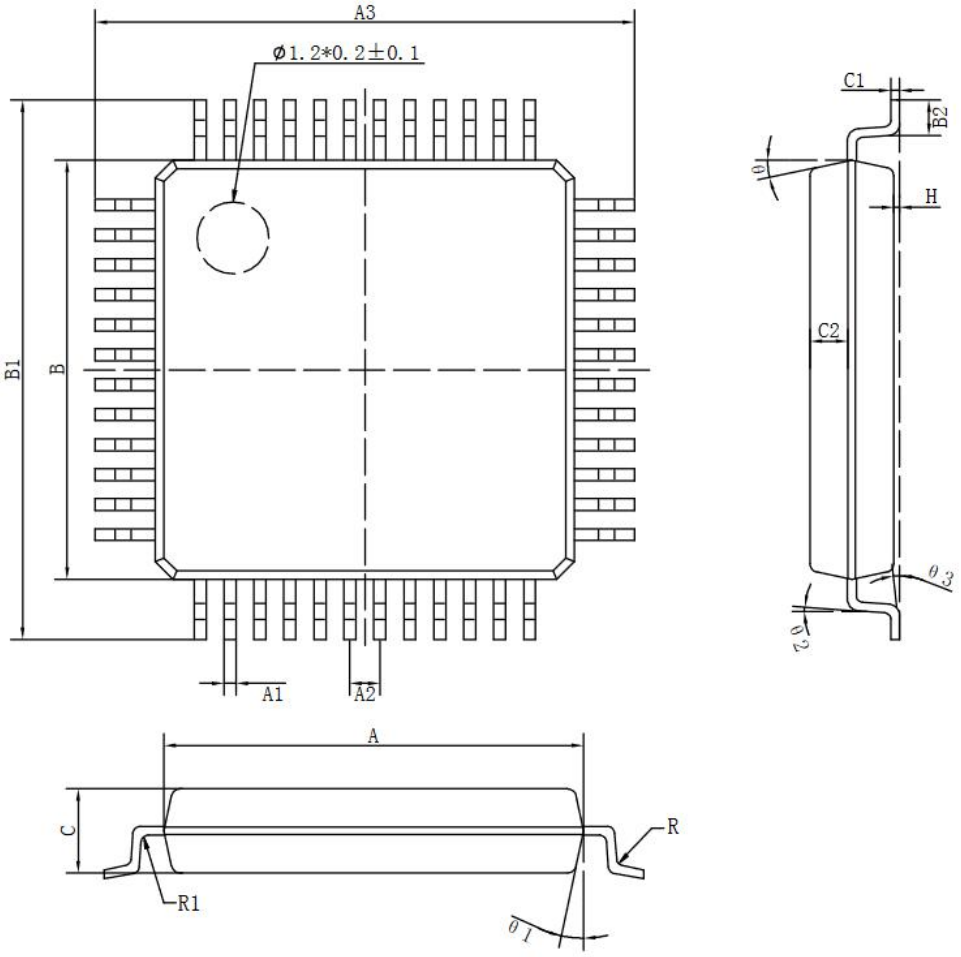


Package Information

TSSOP48



LQFP48



Symbol	Min.（mm）	Max.（mm）	Symbol	Min.（mm）	Max.（mm）
A	6.90	7.10	C2	0.636TYP	
A1	0.20TYP		H	0.05	0.15
A2	0.50TYP		θ	12° TYP	
A3	8.80	9.20	θ1	12° TYP	
B	6.90	7.10	θ2	4° TYP	
B1	8.80	9.20	θ3	0° ~ 5°	
B2	0.50	0.80	R	0.15TYP	
C	1.30	1.50	R1	0.12TYP	
C1	0.127	0.16			

Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version：V1.0 Author：XinCHun Li Time：2023.01.03

Modify the record：

1. Original Version

Statement

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