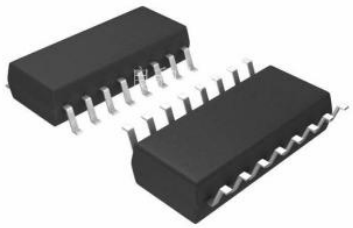
METER-BUS TRANSCEIVER

SSP721A

General Description

SSP721A is a single chip transceiver developed for Meter-Bus standard (EN1434-3、EN13757) applications.
The SSP721A interface circuit adjusts the different potentials between a slave system and the Meter- Bus master. The connection to the bus is polarity independent and supports full galvanic slave isolation with optocouplers. The circuit is supplied by the master via the bus. Therefore, this circuit offers no additional load for the slave battery. A power-fail function is integrated. The receiver has dynamic level recognition, and the transmitter has a programmable current sink. A 3.3V voltage regulator, with power reserve for a delayed switch off at bus fault, is integrated.

SOP-16



Features

- Meter-Bus Transceiver (for Slave) Meets Standard EN1434-3、EN13757
- Receiver Logic With Dynamic Level Recognition
- Adjustable Constant-Current Sink via Resistor
- Polarity Independent
- Power-Fail Function
- Module Supply Voltage Switch
- 3.3-V Constant Voltage Source
- Remote Powering
- Up to 9600 Baud in Half Duplex for UART Protocol
- Support multiple slave power supply modes
- Slave Power Support：

－Supply From Meter-Bus via Output VDD；
－Supply From Meter-Bus via Output VDD or From Backup Battery；
－Supply From Battery, Meter-Bus Active for Data Transmission Only；

- SOP-16 Package

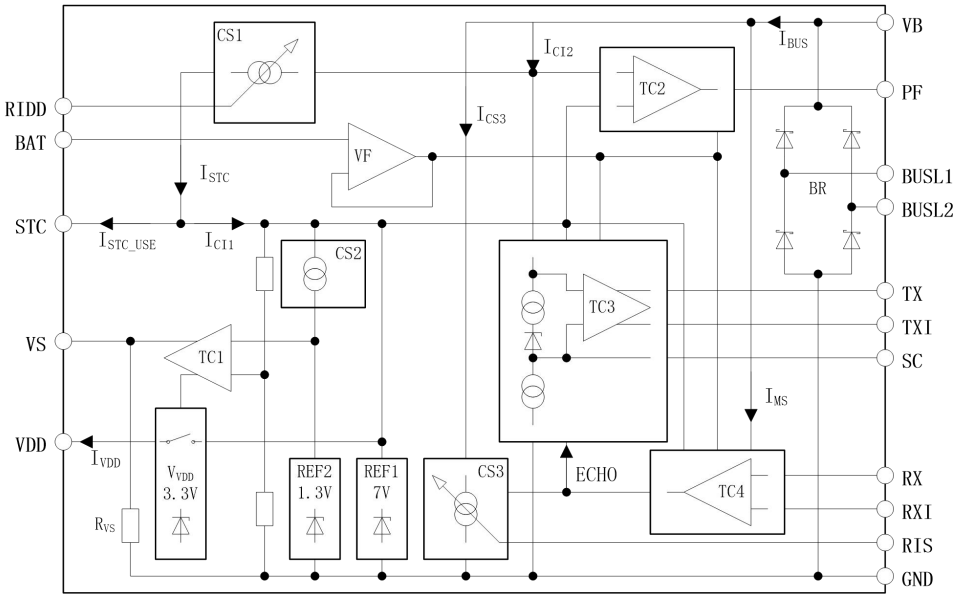
Applications

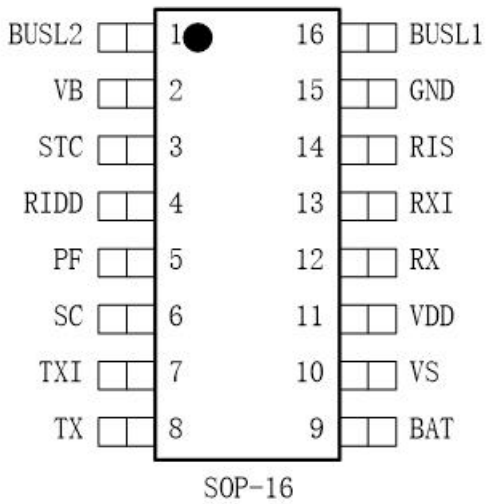
- M-BUS remote meter reading slave station
- M-BUS security slave station
- M-BUS smart home slave station

Order specification

Part No	Package	Manner of Packing	Devices per bag/reel
SSP721A	SOP-16	Reel	2500

Block Diagram and Pin Arrangement Diagram





Pin Assignment

Pin No.	Pin Name	Description
1	BUSL2	Meter-Bus 2
2	VB	Differential bus voltage after rectifier
3	STC	Support capacitor
4	RIDD	Current adjustment input
5	PF	Power fail output
6	SC	Sampling capacitor
7	TXI	Data output inverted
8	TX	Data output
9	BAT	Logic level adjust
10	VS	Switch for bus or battery supply output
11	VDD	Voltage regulator output
12	RX	Data input
13	RXI	Data input inverted
14	RIS	Adjust input for modulation current
15	GND	Ground
16	BUSL1	Meter-Bus 1

Absolute Maximum Ratings

Unless specified otherwise, T_A=25℃

Parameter		Symbol	Value	Unit
Bus voltage(BUSL2-BUSL1)		VMB	±50	V
Input voltage range	Data input	RX	-0.3～5.5	V
	Data input inverted	RXI	-0.3～5.5	V
	Logic level adjust	BAT	-0.3～5.5	V
Operating junction temperature range		T_J	-25～150	℃
Operating free-air temperature range		T_A	-25～85	℃
Storage temperature range		T_{STG}	-65～150	℃
Power derating factor, junction to ambient			8	mW/℃

Recommended Operating Conditions(1)

Parameter		Symbol	Min	Max	Unit
Bus voltage (BUSL2-BUSL1)	Receiver	V_{MB}	10.8	42	V
	Transmitter		12	42	
Input voltage V_I		VB (receive mode)	9.3		V
		BAT(2)	2.5	3.8	
RIDD resistor		R_{RIDD}	13	80	KΩ
RIS resistor		R_{RIS}	100		Ω
Operating free-air temperature		T_A	-25	80	℃

Note 1：All voltage values are measured with respect to the GND terminal unless otherwise noted.

Note 2：VBAT(max)≦VSTA-1V.

Electrical Characteristics(1)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$\triangle V_{BR}$	Voltage drop at rectifier BR	I_{BUS}=3mA				1.5	V
$\triangle V_{CS1}$	Voltage drop at current source CS1	R_{RIDD}=13kΩ				1.8	V
I_{BUS}	BUS current	V_{STC}=6.5V, I_{MC}=0mA	R_{RIDD}=13kΩ			3	mA
			R_{RIDD}=30kΩ			1.5	mA
$\triangle I_{BUS}$	BUS current accuracy	$\triangle V_{BUS}$=10V, I_{MC}=0mA, R_{RIDD}=13～30kΩ				2	%
I_{CC}	Supply current	V_{STC}=6.5V, I_{MC}=0mA, V_{BAT}=3.8V, R_{RIDD}=13kΩ(2)				650	μA
I_{CI1}	CI1current	V_{STC}=6.5V, I_{MC}=0mA, V_{BAT}=3.8V, R_{RIDD}=13kΩ, V_{BUS}=6.5V, RX/RXI=off(2)				350	μA
I_{BAT}	BAT current	V_{BAT}=3.8V		-0.5		0.5	μA
I_{BAT}=I_{VDD}	BAT plus VDD current	V_{BUS}=0V, V_{STC}=0V		-0.5		0.5	μA
V_{VDD}	VDD voltage	-I_{VDD}=1mA, V_{STC}=6.5V		3.1		3.4	V
R_{VDD}	VDD resistance	-I_{VDD}=2～8mA, V_{STC}=4.5V				5	Ω
V_{CTC}	STC voltage	V_{DD}=on, VS=on		5.6		6.4	V
		V_{DD}=off, VS=off		3.8		4.3	
		I_{VDD} < I_{STC_USE}		6.5		7.5	
I_{STC_USE}	STC current	V_{STC}=5V	R_{RIDD}=13kΩ	1.85		2.4	mA
			R_{RIDD}=30kΩ	0.65		1.1	
V_{RIDD}	RIDD voltage	R_{RIDD}=30kΩ		1.23		1.33	V

V_{VS}	VS voltage	V_{DD}=on, I_{VS}=-5μA		V_{BAC} -0.4		V_{BAC}	V
R_{VS}	VS resistance	V_{DD}=off		0.3		1	MΩ
V_{PF}	PF voltage	V_{STC} =6.5V	V_{VB}=V_{STC}+0.8V, I_{PF}=-100μA	V_{BAT} -0.6		V_{BAT}	V
			V_{VB}=V_{STC}+0.3V, I_{PF}=1μA	0		0.6	
			V_{VB}=V_{SC}+0.3V, I_{PF}=5μA	0		0.9	
t_{on}	Turn-on time	C_{STC}=50μF, Bus voltage slew rate: 1V/μs				3	s

Note 1：All voltage values are measured with respect to the GND terminal, unless otherwise noted.

Note 2：Inputs RX/RXI and outputs TX/TXI are open, I_{CC}=I_{CI1}+I_{CI2}.

Receiver Section Electrical Characteristics(1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_T		See Figure 1	MARK-8.2		MARK-5.7	V
V_{SC}	SC voltage				VVB	V
I_{SC_charge}	SC charge current	V_{SC}=24V,V_{VB}=36V	-15		-40	μA
$I_{SC\_discharge}$	SC discharge current	V_{SC}=V_{VB}=24V	0.3		-0.033×I_{SC_charge}	μA
V_{OH}	TX/TXI High-level output voltage	I_{TX}/I_{TXI}=-100μA	V_{BAT}-0.6		V_{BAT}	V
V_{OL}	TX/TXI Low-level output voltage	I_{TX}/I_{TXI}=100μA	0		0.5	V
		I_{TX}=1.1mA	0		1.5	
I_{TX}/I_{TXI}	TX/TXI current	V_{TX}=7.5V,V_{VB}=12V, V_{STC}=6V,V_{BAT}=3.8V			10	μA

Note: All voltage values are measured with respect to the GND terminal, unless otherwise noted.

Transmitter Section Electrical Characteristics(1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{MC}	MC current	R_{RIS}=100Ω	11.5		19.5	mA
V_{RIS}	RIS voltage	R_{RIS}=100Ω	1.4		1.7	V
		R_{RIS}=1kΩ	1.5		1.8	
V_{IH}	RX/RXI High-level input	See Figure 2(2)	V_{BAT}-0.8		5.5	V

	voltage					
V_{IL}	RX/RXI Low-level input voltage	See Figure 2	0		0.8	V
I_{RX}	RX current	$V_{RX}=V_{BAT}=3V$, $V_{VB}=V_{STC}=0V$	-0.5		0.5	μA
		$V_{RX}=0, V_{BAT}=3V$, $V_{STC}=6.5V$	-10		-40	
I_{RXI}	RXI current	$V_{RXI}=V_{BAT}=3V$, $V_{VB}=V_{STC}=0V$	10		40	μA
		$V_{RXI}=V_{BAT}=3V$, $V_{STC}=6.5V$	10		40	

Note 1：All voltage values are measured with respect to the GND terminal, unless otherwise noted.

Note 2：VIH(max) = 5.5 V is valid only when VSTC > 6.5 V.

Functional specifications

Data Transmission, Master to Slave

The transmission of signals from the master station to the slave station is accomplished through bus voltage modulation. The mark level on the bus lines V_{BUS} = MARK is defined by the difference of BUSL1 and BUSL2 at the slave. It is dependent on the distance of Master to Slave, which affects the voltage drop on the wire. To make the receiver independent, a dynamic reference level on the SC pin is used for the voltage comparator TC3 (see Figure 1).

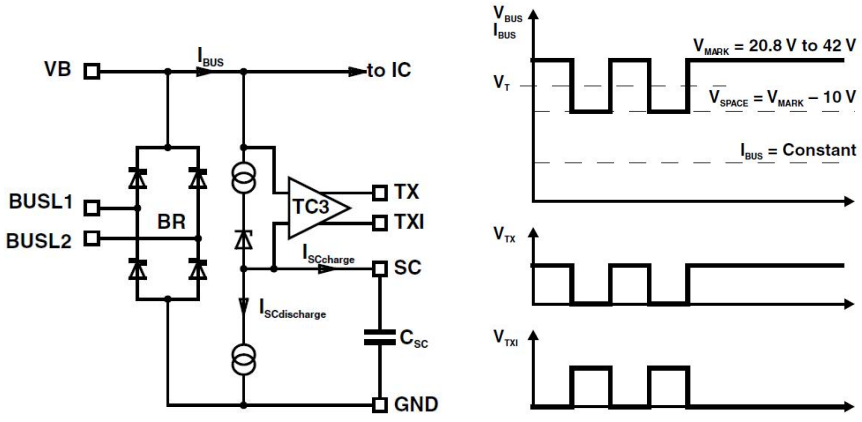


Figure 1. Data Transmission, Master to Slave

A capacitor C_{SC} at pin SC is charged by a current $I_{SCcharge}$ and is discharged with a current $I_{SCdischarge}$ where:

$$I_{SCdischarge} = I_{SCcharge}/40(typ)$$

This ratio is necessary to run any kind of UART protocol independent of the data contents. (for example, if an11-bit UART protocol is transmitted with all data bits at 0 and only the stop bit at

1). There must be sufficient time to recharge the capacitor C_{SC}. The input level detector TC3 detects voltage modulations from the master, V_{BUS} = SPACE/MARK conditions, and switches the inverted output TXI and the non-inverted output TX.

Data Transmission, Slave to Master

The device uses current modulation to transmit information from the slave to the master while the bus voltage remains constant. The current source CS3 modulates the bus current and the master detects the modulation. The constant current source CS3 is controlled by the inverted input RXI or the non-inverted input RX. The current source CS3 can be programmed by an external resistor R_{RIS}. The modulation supply current I_{MS} flows in addition to the current source CS3 during the modulation time.(see Figure 2)

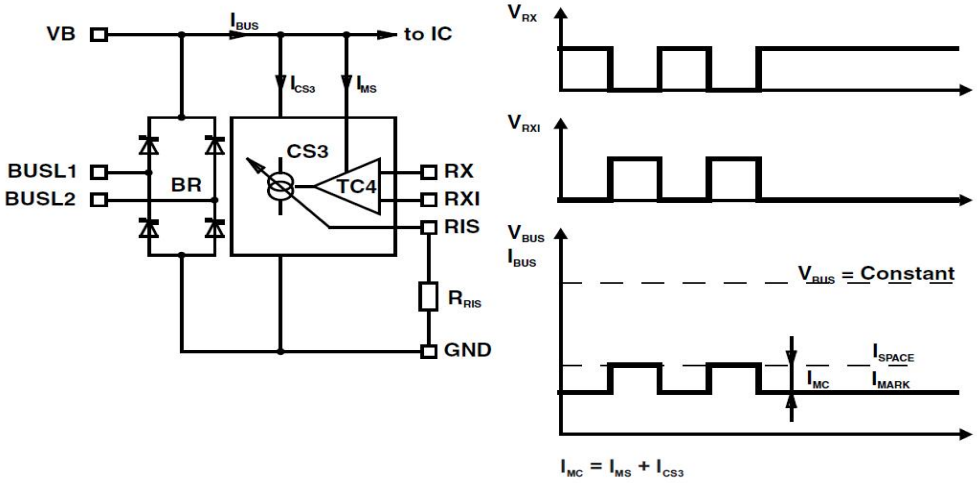
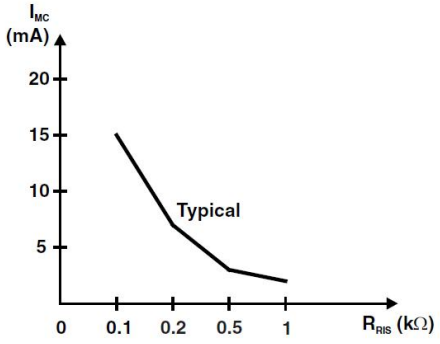


Figure 2. Data Transmission, Slave to Master

Because the SSP721A is configured for half-duplex only, the current modulation from RX or RXI is repeated concurrently as ECHO on the outputs TX and TXI. If the slave, as well as the master, is trying to send information via the lines, the added signals appear on the outputs TX and TXI, which indicates the data collision to the slave(see Functional Schematic)。 The bus topology requires a constant current consumption by each connected slave. To calculate the value of the programming resistor R_{RIS}, use the formula shown in Figure 3.



R_{RIS} =V_{RIS}/I_{CS3} = $V_{RIS}/(I_{MC}-I_{MS})$

V_{RIS} =Voltage on pin RIS

R_{RIS} = Programming resistor

I_{CS3} = Programmable current

I_{MC} = Modulation current

IMS = Modulation supply current (220 µA typ)

Figure 3. Calculate Programming Resistor R_{RIS}

Slave Supply

The SSP721A has an internal 3.3V voltage regulator. The output power of this voltage regulator is supplied by the storage capacitor C_{STC} at pin STC. The storage capacitor C_{STC} at pin STC is charged with constant current I_{STC_use} from the current source CS1. The maximum capacitor voltage is limited to REF1. The charge current I_{STC} has to be defined by an external resistor at pin RIDD.

The adjustment resistor RRIDD can be calculated using Equation：

$$R_{RIID} = 25V_{RIDD}/I_{STC} = 25\ V_{RIDD}/(I_{STC\_use} + I_{IC1})$$

Where,

I_{STC} = current from current source CS1

I_{STC_use} = charge current for support capacitor

I_{C1} = internal current

V_{RIDD} = voltage on pin RIDD

R_{RIDD} = value of adjustment resistor

The voltage level of the storage capacitor C_{STC} is monitored with comparator TC1. Once the voltage V_{STC} reaches V_{VDD_on}, the switch S_{VDD} connects the stabilized voltage V_{VDD} to pin VDD. VDD is turned off if the voltage VSTC drops below the V_{VDD_off} level.

Voltage variations on the capacitor C_{STC} create bus current changes (see Figure 4).

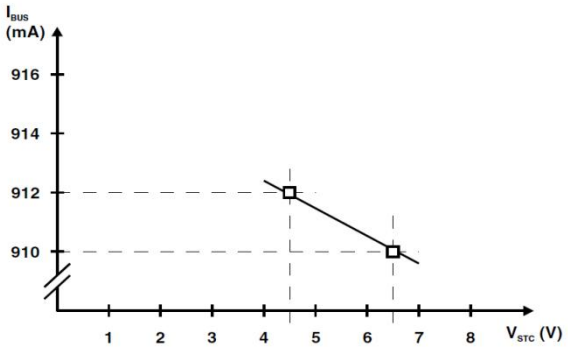


Figure 4. Single Mode Bus Load

At a bus fault the shut down time of VDD (t_{off}) in which data storage can be performed depends on the system current I_{VDD} and the value of capacitor C_{STC}. See Figure 5, which shows a correlation between the shutdown of the bus voltage V_{BUS} and V_{DD_off} and t_{off} for dimensioning the capacitor.

The output VS is meant for slave systems that are driven by the bus energy, as well as from a battery should the bus line voltage fail. The switching of VS is synchronized with VDD and is controlled by the comparator TC1. An external transistor at the output VS allows switching from the Meter-Bus remote supply to battery.

Power On/Off

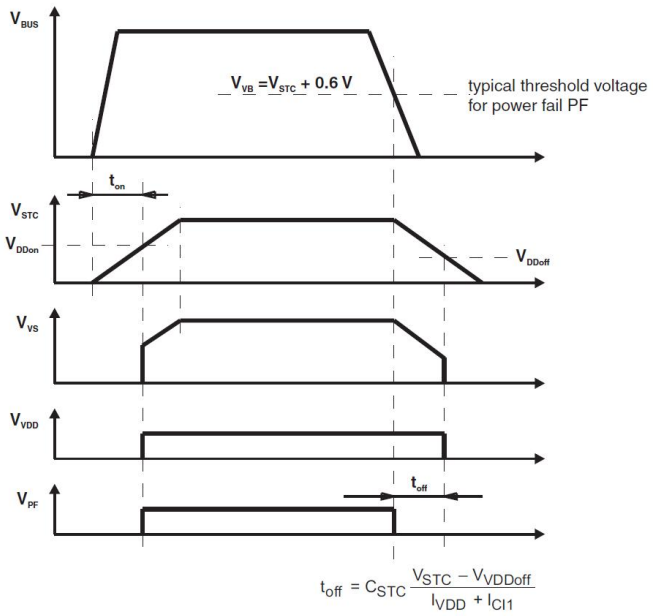
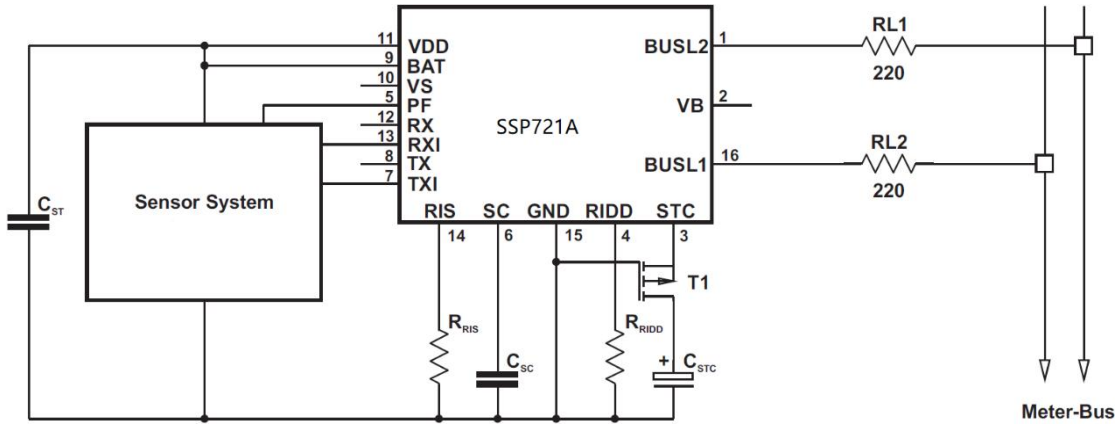


Figure 5. Power On/Off Timing

Power Fail Function

Because of the rectifier bridge BR at the input, BUSL1, and BUSL2, the SSP721A is polarity independent. The pin VB to ground (GND) delivers the bus voltage V_{VB} less the voltage drop over the rectifier BR. The voltage comparator TC2 monitors the bus voltage. If the voltage $V_{VB} > V_{STC} + 0.6$ V, then the output PF = 1. The output level PF = 0 (power fail) provides a warning of a critical voltage drop to the micro-controller to save the data immediately.

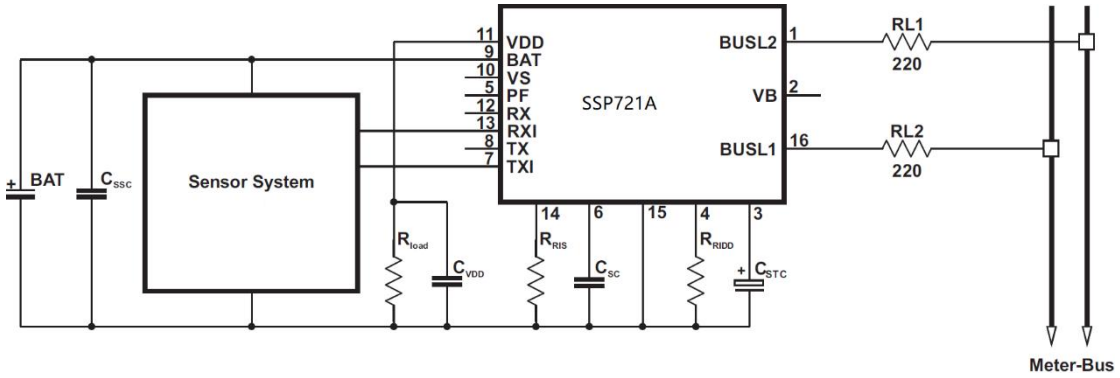
Basic Application Circuit



R_{RIDD}=30KΩ	C_{STC}≧220uF	Single load 1UL
R_{RIDD}=13KΩ	C_{STC}≧470uF	Double load 2UL

NOTE: Transistor T1 should be a BSS84.

Basic Application Circuit for Supply From Battery

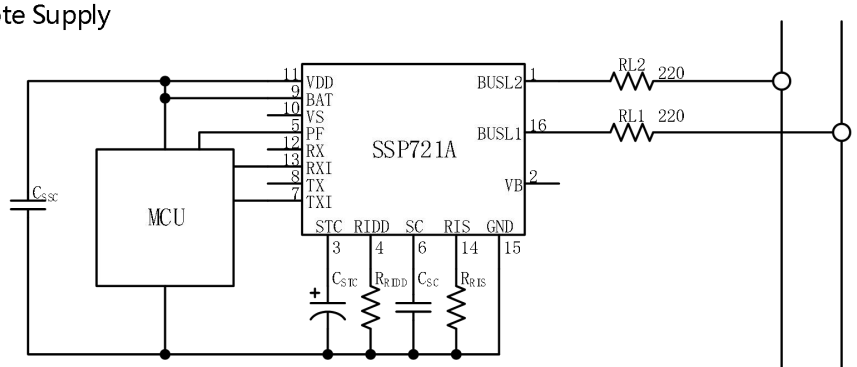


C_{SSC}	system stabilising capacitor	R_{RIDD}	slave-current adjustment resistor
C_{STC}	support capacitor	R_{RIS}	modulation-current resistor
C_{SC}	sampling capacitor	RL1 RL2	protection resistors
C_{VDD}	stabilising capacitor	R_{load}	discharge resistor

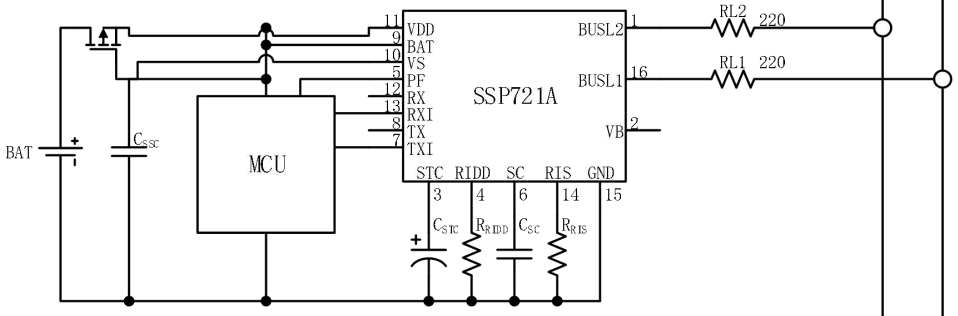
Note：C_{STC}:C_{VDD}≧4:1

Basic Applications for Different Supply Modes

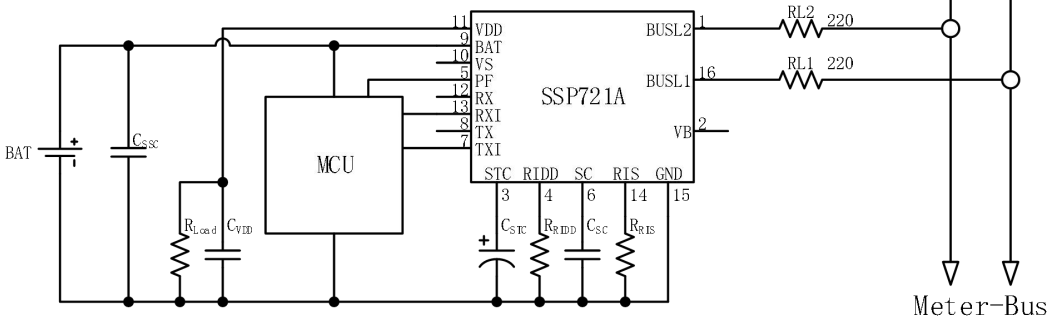
Remote Supply



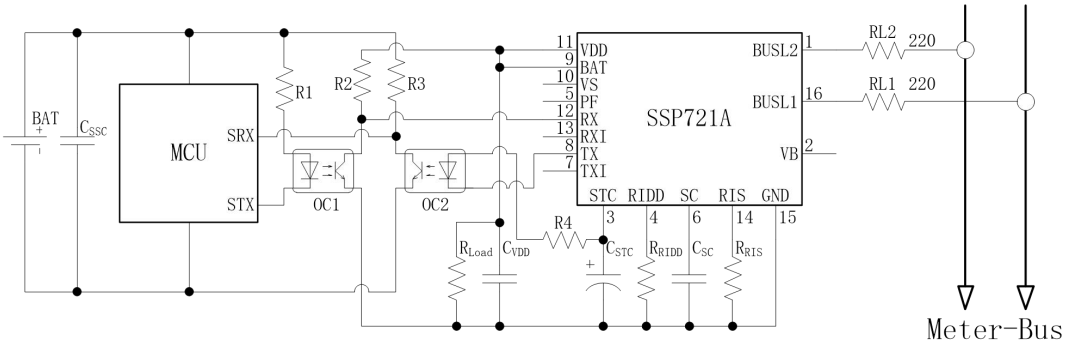
Remote Supply/Battery Support



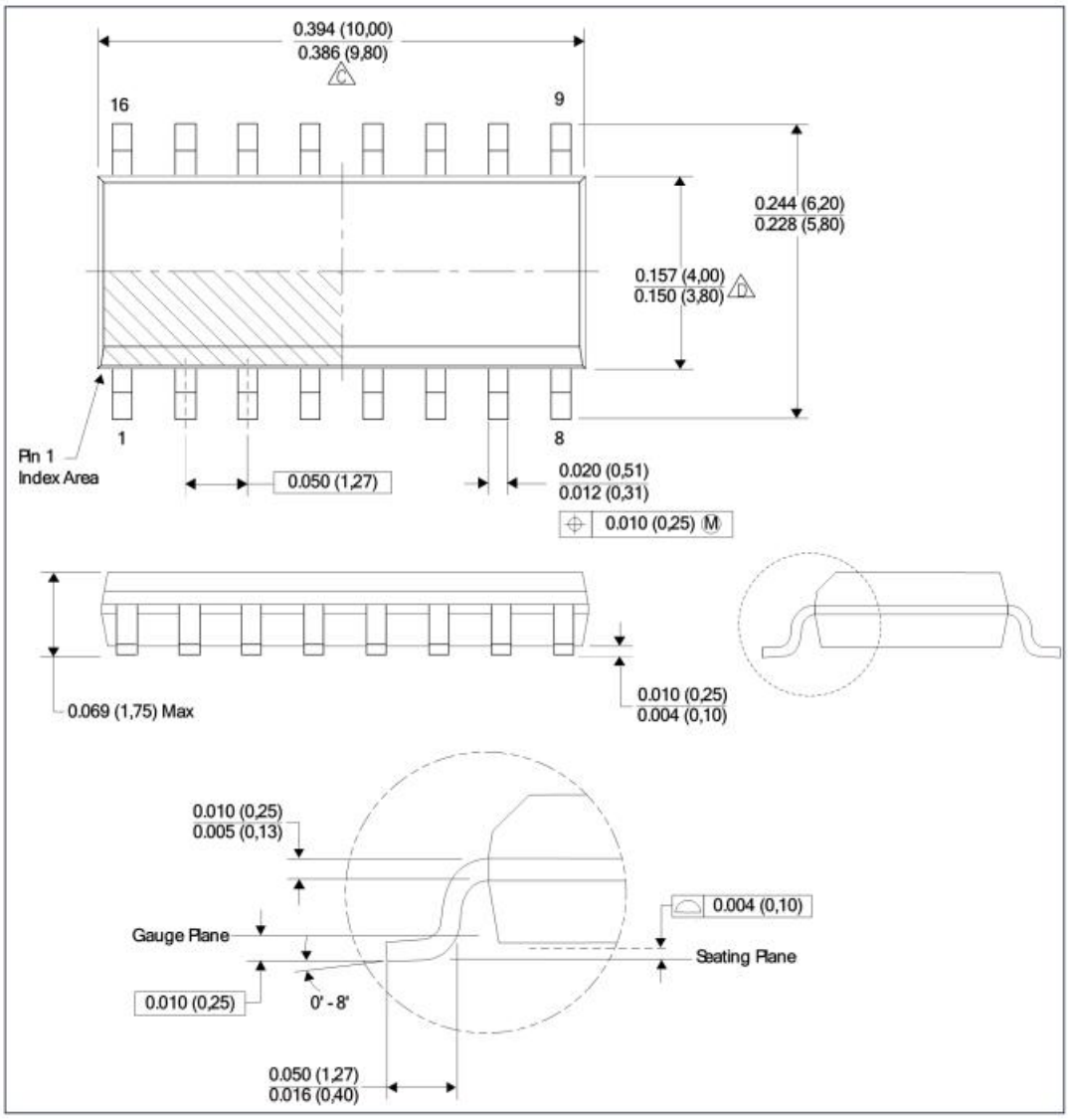
Battery Support



Basic Optocoupler Application



Package Information (SOP-16)



Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version：V1.1	Author：Siyuan Wu	Time：2021.8.23

Modify the record：

1. Re-typesetting the manual and checking some data

Statement

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