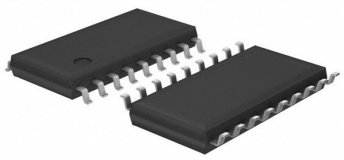
High-voltage High-current Darlington Transistor Arrays

ULN2803

General Description

ULN2803 is a single-chip integrated high voltage, high current Darlington tube array, The circuit contains eight independent Darlington tube drive single channel. The circuit is designed with continuous diode, which can be used to drive relay, stepping motor and other inductive loads. A single darlington collector can output 500mA current. Higher output current capacity can be achieved by connecting darlington tubes in parallel.

SOP-18



Features

- 500mA-Rated Collector Current(single output)
- Input Compatible TTL/CMOS logic signals
- High-Voltage Outputs:50V
- Relay-Driver Applications
- Package：SOP-18

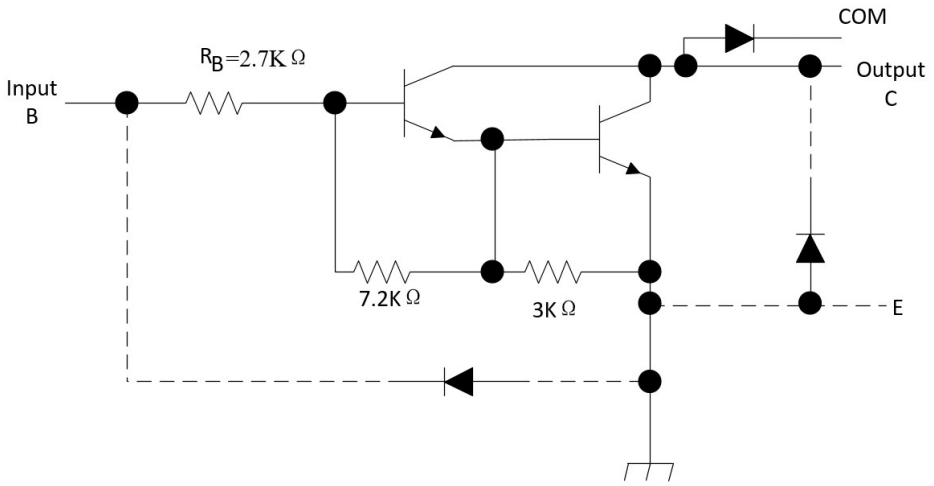
Applications

- Solenoids
- Relays
- DC motors
- LED displays
- Filament lamps
- Thermal print-heads
- High-power buffers

Order information

Product model	Package	manner of packing	Minimum packing quantity
ULN2803	SOP-18	reel	2000

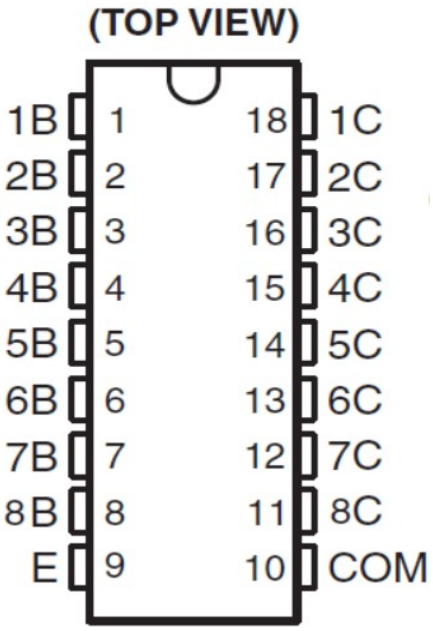
Functional Block Diagram



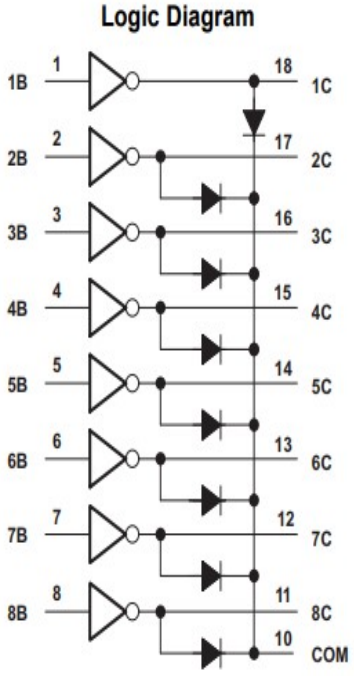
Note: All resistor values shown are nominal.

The collentor-emitter diode is a parasitic structure and should not be used to conduct current.If the collector(s) go below ground an external Schoottky diode should be added to clamp negative undershoots.

Pin Assignments



Connection Diagram



Pin Descriptions

Pin Number	Pin Name	Function
1	1B	Input pair1
2	2B	Input pair2
3	3B	Input pair3
4	4B	Input pair4
5	5B	Input pair5
6	6B	Input pair6
7	7B	Input pair7
8	8B	Input pair8
9	E	Common Emitter (ground)
10	COM	Common Clamp Diodes
11	8C	Output pair8
12	7C	Output pair7
13	6C	Output pair6
14	5C	Output pair5
15	4C	Output pair4
16	3C	Output pair3
17	2C	Output pair2
18	1C	Output pair1

Absolute Maximum Ratings (1)

At 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
VCC	Collector to emitter voltage		50	V
VR	Clamp diode reverse voltage(2)		50	V
VI	Input voltage(2)		30	V
ICP	Peak collector current		500	mA
IOK	Output clamp current		500	mA
ITE	Total emitter-terminal current		–2.5	A
TA	Operating free-air temperature range	–20	70	°C
θJA	Thermal Resistance Junction-to-Ambient(3)		63	°C/W
θJC	Thermal Resistance Junction-to-Case(4)		12	
TJ	Operating virtual junction temperature		150	°C
TSTG	Storage temperature range	–40	85	°C

(1) Exceeding the absolute maximum rating may cause permanent damage to the chip. These are only maximum ratings and prolonged use at absolute maximum ratings may affect the reliability of the chip.

(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

(3) Maximum power dissipation is a function of TJ(max), θJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) – TA)/θJA. Operating at the absolute maximum TJ of 150°C can affect reliability.

(4) Maximum power dissipation is a function of TJ(max), θJC, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) – TA)/θJC. Operating at the absolute maximum TJ of 150°C can affect reliability.

Electrical Characteristics

(TA=+25°C, unless otherwise specified)

Symbol	Parameter	Test Figure	Test Conditions		ULN2803			Unit
					MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	Figure 6	V_{CE}=2V	I_C=200mA	--	--	2.4	V
				I_C=250mA	--	--	2.7	
				I_C=300mA	--	--	3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 5	I_I=250μA,	I_C=100mA	--	0.9	1.1	
			I_I=350μA,	I_C=200mA	--	1	1.3	V
			I_I=500μA,	I_C=350mA	--	1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 1	V_{CE}=50V,	I_I=0	--	--	50	μA
		Figure 2	V_{CE}=50V, T_A=+105°C	I_I=0	--	--	100	
V_F	Clamp forward voltage	Figure 8	I_F=350mA		--	1.7	2	V
$I_{I(off)}$	Off-state input current	Figure 3	V_{CE}=50V， I_C=500 μA		50	65	--	μA
I_I	Input current	Figure 4	V_I=3.85V		--	0.93	1.35	mA
			V_I=5V		--	--	--	
			V_I=12V		--	--	--	
I_R	Clamp reverse current	Figure 7	V_R=50V		--	--	50	μA
				T_A=70°C	--	--	100	
C_i	Input capacitance		V_I=0， f =1MHz		--	15	25	pF

Switching Characteristics

(T_A = +25°C, unless otherwise specified)

Symbol	Parameter	Test pattern	Test Conditions	ULN2803			Unit
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to high-level output	See Figure 9		--	0.25	1	μs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 9		--	0.25	1	μs
V_{OH}	High-level output voltage After switching	See Figure 9	V_S = 50 V, I_O = 300 mA,	VS–20	--	--	mV

Parameter Measurement Information

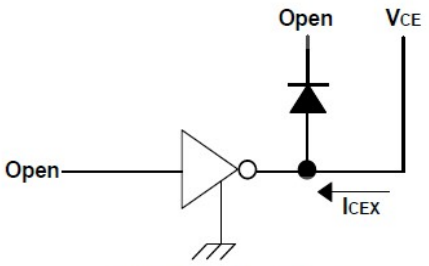


Fig.1 I_{CEX} Test Circuit

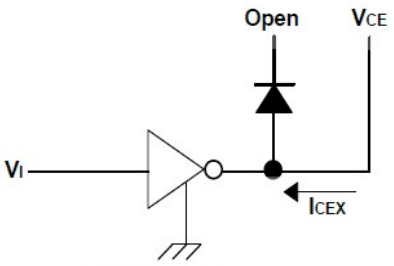


Fig.2 I_{CEX} Test Circuit

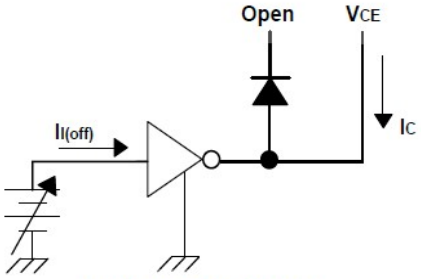


Fig.3 $I_{I(off)}$ Test Circuit

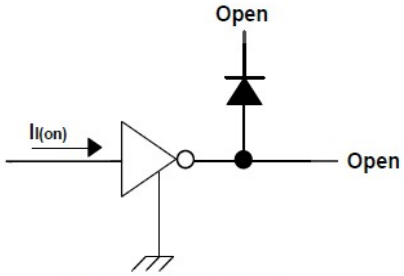


Fig.4 I_I Test Circuit

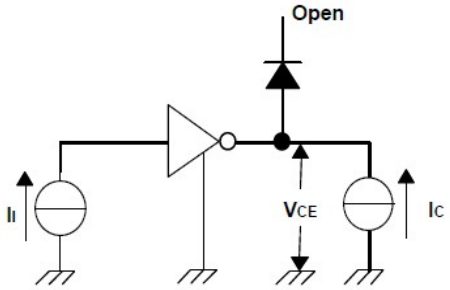


Fig. 5 h_{FE} , $V_{CE(sat)}$ Test Circuit

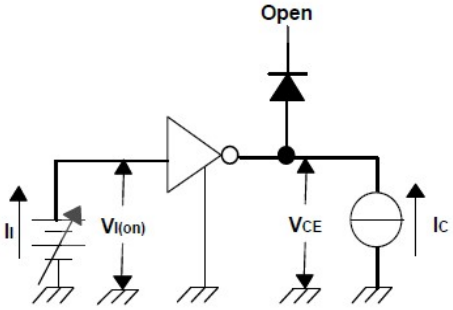


Fig. 6 $V_{I(on)}$ Test Circuit

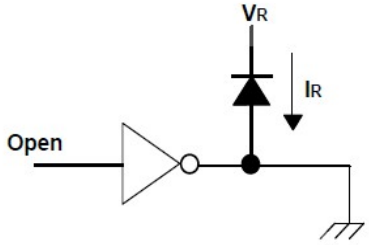


Fig. 7 I_R Test Circuit

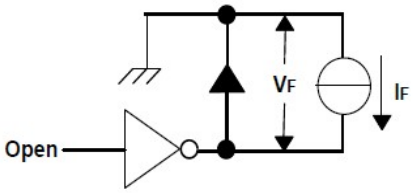
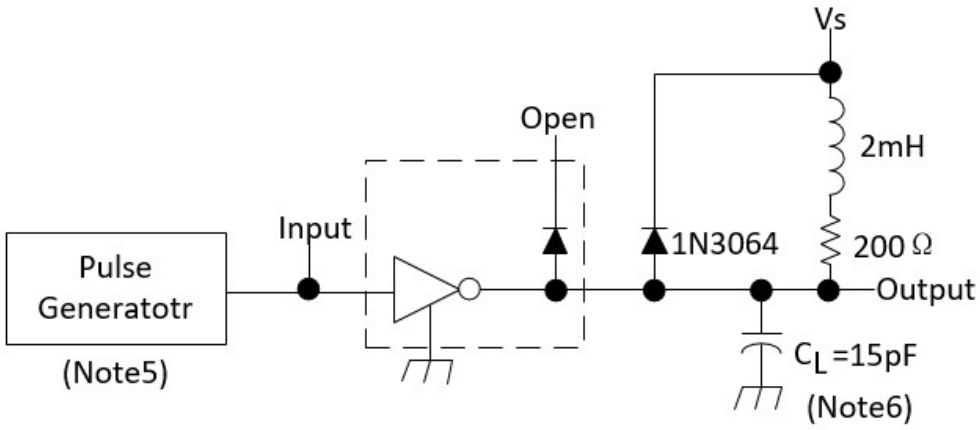
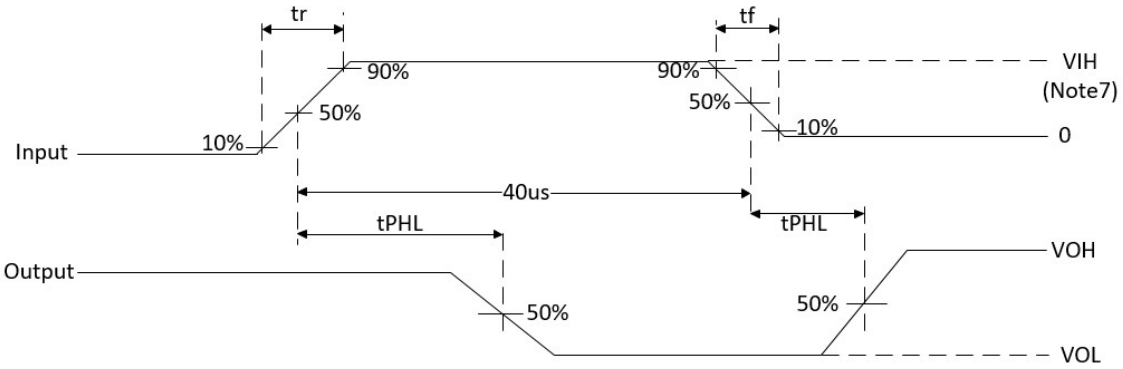


Fig. 8 V_F Test Circuit



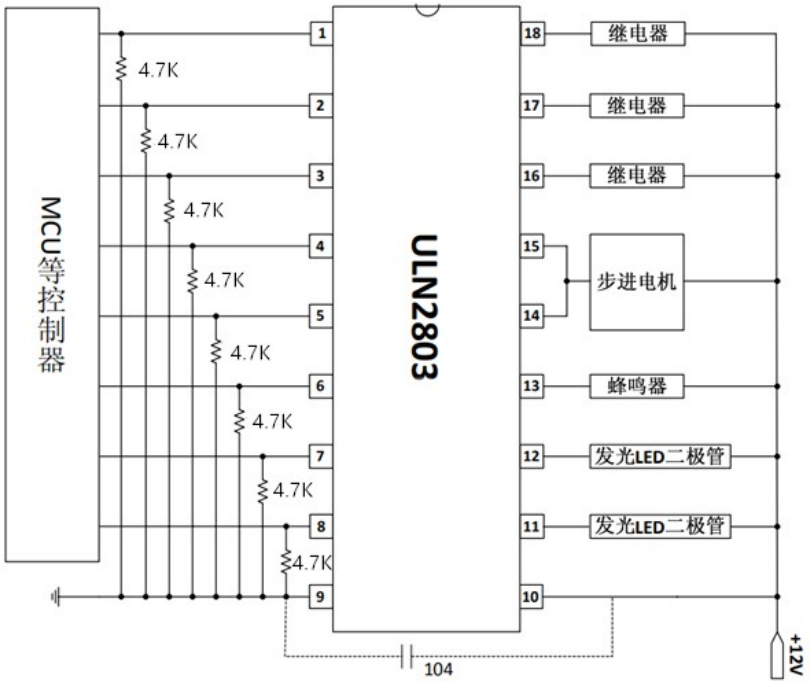


Transmission delay waveform diagram

Fig.

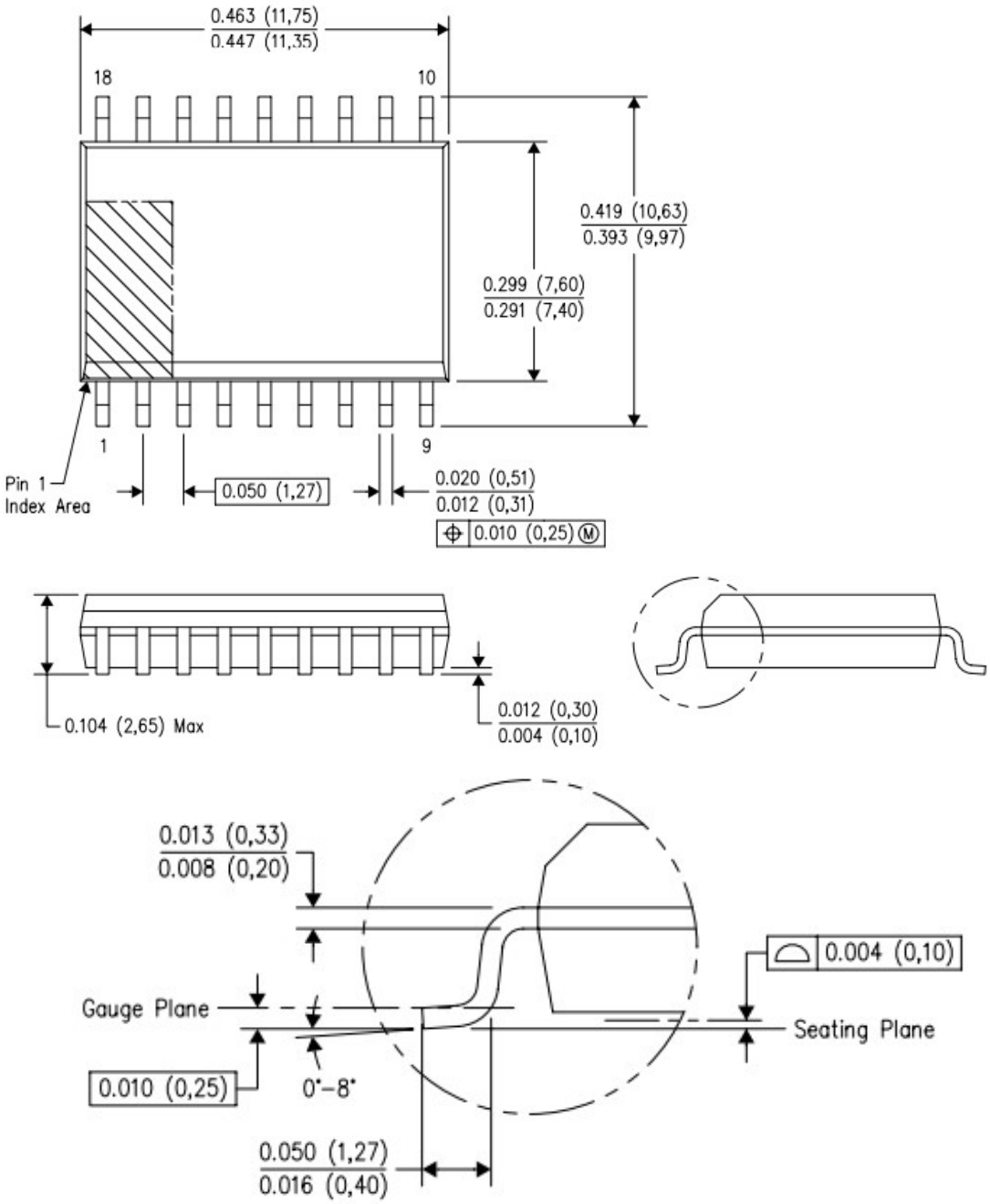
Notes: (5)The pulse generator has the following characteristics:
Pulse Width=12.5Hz, output impedance 50Ω, tr≤5ns, tr≤10ns.
(6)C_L includes prove and jig capacitance.
(7)V_{IH}=3V

Typical application



Considering that some applications use a single-chip machine with pull resistance,The output state of the single chip is unstable during power-up. At this time, the ULN2803 input stage will be affected by the single-chip pull-up resistance and turn on the load. In order to avoid load misoperation, it is recommended that customers with such application problems connect a 4.7K pull-down resistance at the input stage, as shown in the figure above.

SOP18 Outline Dimensions



Special Version

The company reserves the right of final interpretation of this specification.

Version Change Description

Versions: V1.2	Writer: Si Yuan Wu	Time: 2021.9.7

Amendant record:

1.Re-typesetting the manual and checking some data