深圳市海凌科电子有限公司

HLK-N10 Datasheet

版本：V1.0　　修订日期：2020 年 7 月 14 日

Contents

1 Overview

HLK-N10 is a high performance, highly integrated single chip SoC processor targeting on low speed IoT scenarios. It's fully compatible with 3GPP TS 36.211 at physical layer and it incorporates the protocol stack and the sim interface as well for end-user. It's a low cost, low power, low BOM solution for many IoT application.

1.1 Summary of Key Features

The key features of this product are as follows.

1.1.1. NB-IoT communication

- 3GPP R14 specification fully compliant
- Supports all three deployment scenarios (Standalone, in-band, guard-band)
- Supports both single-tone and multi-tone transmission modes in uplink
- Supports PSM and eDRX mode
- Extremely optimized baseband for power saving mode

1.1.2. System

- Various Operational modes with wakeup resources.
  - DEEPSLEEP, STANDBY, OPLPM, ACTIVE
- Various peripherals to satisfy various use cases
  - Master/Slave I2C X2
  - Master/Slave SPI X1
  - Uart X1
  - CSP (Configurable Serial Port) X4
  - AES X1
  - PWM Timer X4
  - UTC
  - Configurable GPIO
- Security support for both USER program and application data
- Integrated DSP and AP core, up to 106 MIPS
- 2M Flash integrated
- SRAM integrated for software, 64~96K usable for application
- Less external components.

1.1.3. RF/Analog subsystem

- Low band (699MHz-960MHz) and high band (1.71GHz-2.2GHz)

- Ultra low power consumption in DEEPSLEEP mode for longer battery life
- Integrated advanced PMU, providing significant power saving
- Integrated CMOS power amplifier delivering more than 23dBm linear output power
- Fractional N PLL support for wide range reference clock frequency
- One channels of sensor interface with single 12-bits on-chip ADC
- On-chip RTC with calibration capability

1.1.4. Algorithm Highlights

- Low-Complexity, Efficient, and Flexible Channel Estimation Algorithm
- Low-Complexity Detection of Mobility Scenarios
- Optimization of Decoders for Very Low SNR

1.1.5. Power consumption at different modes. (3.6v@vbat@25C)

- Rx ACTIVE: 25mA
- Tx ACTIVE: 350mA@21dBm; 78mA@0dBm
- DEEPSLEEP:
  - ✧ without retention memory
  - ✧ with 4K retention memory
- STANDBY: ~180uA WITH XTAL reference design, VDDIO 2.65V@ STANDBY MODE

1.1.6. Environmental

- Ambient temperature range: -40 °C to 85 °C
- Storage temperature: -40 °C to 125 °C
- Humidity: 0~100%

1.2 Applications

- Smart Metering and Smart Grid
- Traffic Management and Monitoring
- Security and Asset Tracking
- White Goods and Automotive Service Data and Diagnostics
- Environmental Monitoring and Control
- Tele-health and Patient Monitoring
- Smart Cities (waste management, lighting, pest control, building climate control, environmental monitoring, etc)

2 Hardware Functional Description

2.1 Functional Block Diagram

The following block diagram shows an overview of the use case scenario. NB-IoT is used as TX/RX transmitter for various sensors with spi/i2c/uart interface.

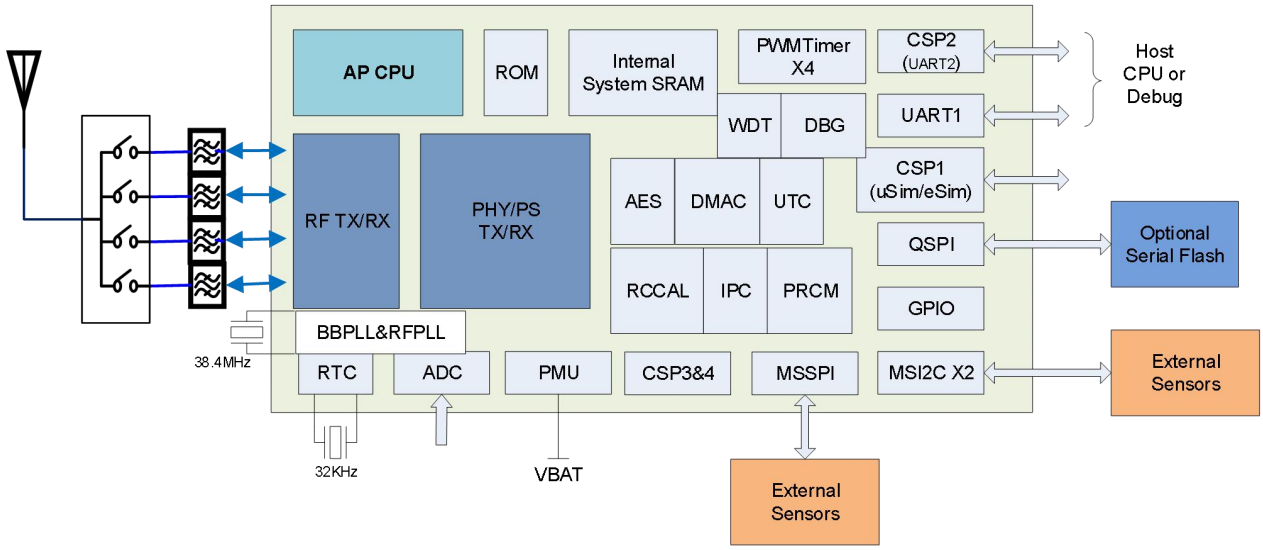


Figure 2- 1 Functional block diagram

2.2 Power Management

The power management system includes one DC-DC converter, two IOLDOs, one CLDO, one PALDO, and multiple internal LDO regulators. The typical power topology of HLK-N10 is shown in Figure 2.

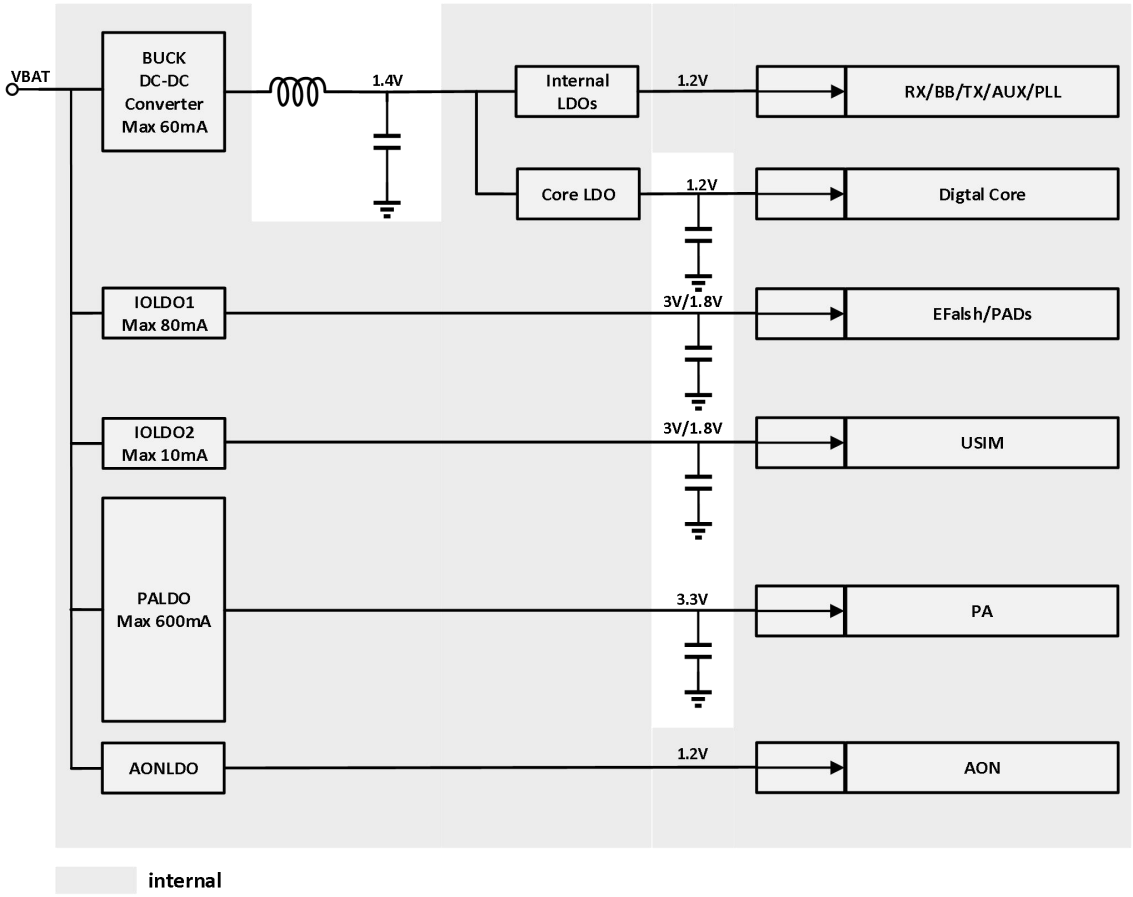


Figure 2- 2 Typical Power Topology

2.3 RF subsystem

RF/Analog Block Diagram is shown as the following figure.

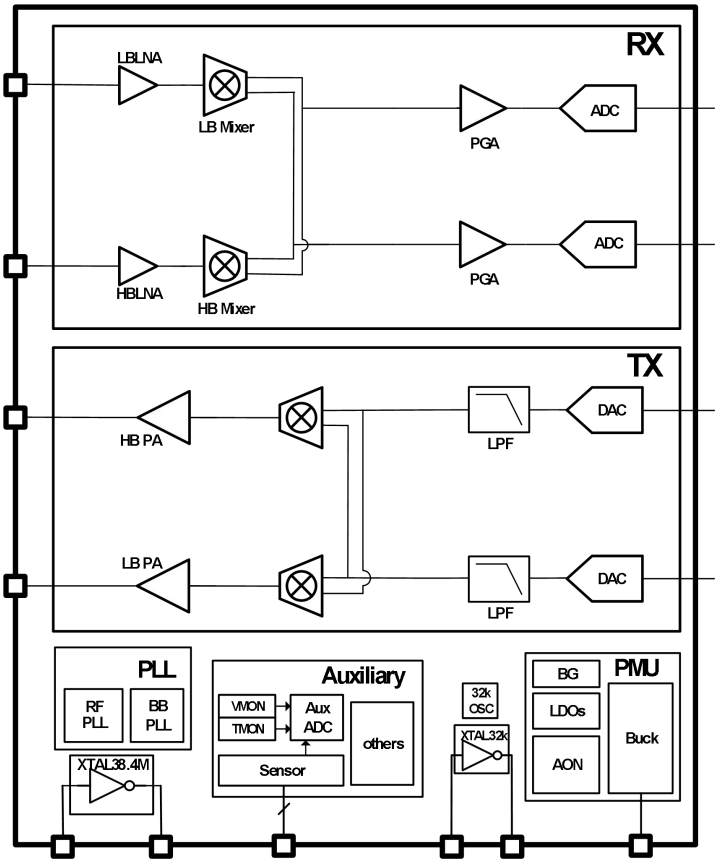


Figure 2- 3 RF/Analog functional block diagram

2.4 AP subsystem

This subsystem is open to customer for application software development. It includes one Cortex M3 MCU and the necessary peripherals APIs are available as well. Typically 96K bytes SRAM could be used for application purpose.

2.5 Peripheral subsystem

2. 5. 1. Universal Asynchronous Receiver Transmitter (UART)

There is one dedicated UART module in the chip. The UART module is a full duplex asynchronous receiver and transmitter that supports a wide range of software programmable baud rates and data formats, and can accommodate automatic parity generation and several error detection schemes. The interface has been developed for a modem to be connected, with both receive and transmit FIFO providing a buffer for the CPU.

Here are the main features supported

- Automatic baud rate detection function
- Programmable baud rate generator
- 64bytes receive FIFO and 64bytes transmit FIFO
- 6, 7 or 8 data bits
- 1, 1.5 or 2 stop bits
- Odd, even, space, mark, or no parity
- Parity, framing and overflow error detection

- Line break generation and detection
- Automatic echo, local loopback and remote loopback channel modes
- Interrupt generation
- Flow control with: CTS, RTS

2. 5. 2. Inter Integrated Circuit (I2C)

There are two MSI2C modules available in the chip. The I2C module is a bus controller that can function as a master or slave in a multi-master, two-wire serial I2C bus.

Here are the main features supported

- Uses I2C bus specification version 2.0 (100Khz and 400KHz)
- Programmable for both normal (100 kHz) and fast bus data rates (400 kHz)
- Programmable as either a master or slave interface
- Programmable to use normal or extended addressing
- Capable of clock synchronization and bus arbitration
- Fully programmable slave response address
- 8 bytes transmit FIFO and 8 bytes receiving FIFO
- Slave monitor mode when set up as master
- Supports I2C bus hold for slow host service
- Supports combined format transfers both as master and slave
- Slave time out detection with programmable period
- Transfer status interrupts and flags

2. 5. 3. Serial Peripheral Interface (SPI)

There is one MSSPI module available in the chip. The SPI module provides full-duplex, synchronous, serial communication between master and slave, or other peripheral devices.

Here are the main features supported

- Full-duplex operation offers simultaneous receive and transmit
- Master or slave SPI modes of operation
- Four wire bus — data RX, data TX, clock, and select
- Supports multi-master environment - Identifies an error condition if more than one master detected
- Buffered operation with separate transmit and receive FIFOs — 512bytes TX fifo and 128 bytes RX fifo.
- Programmable master mode clock frequencies
- Serial clock with programmable polarity
- Programmable transmission format
- Programmable interrupt generation
- Up to two external peripheral selects

2. 5. 4. Configurable Serial Port (CSP)

There are 4 CSP module available in the chip. The CSP module is used for serial communication where only 1 bit is transmitted at a time. The advantage of a serial port is that it requires relatively few pins so it is often more cost-effective than parallel ports (especially in long-range communication). The serial port is a general-purpose interface that transmits or receives data a bit at one time and used for almost any type of devices.

The CSP is a multi-function serial interface to communicate with many common serial ports.

The user can set the transfer frame parameters such as data length, transmitting data length etc to configure the right frame format. According to different connection protocols it can be configured as a full

duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and modems, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, serial EEPROMs, or touch panel controllers.

Functional description and Features

- Depending on the clock, the CSP can be configured in the following modes:
  - Asynchronous (no clock is needed)
    - Sample use cases – UART and IrDA
  - Synchronous – Master (clock is generated by CSP)
    - Same use cases – SPI bus, PCM bus, Smart Card bus.
    - Max clock frequency = 1/6 of PCLK
  - Synchronous – Slave (clock is generated by external chip)
    - Max clock frequency = 1/10 the PCLK
- Depending on the type of the serial bus, the CSP can support the following types of serial ports:
  - ASYNC (UART and IrDA)
  - SPI bus
  - I2S bus
  - Smart Card bus

2. 5. 5. Universal Time Clock (UTC)

There is one UTC module located in AON domain which can work in DEEPSLEEP mode. The UTC module keeps track of time of day, to an accuracy of one hundredth of a second, and has calendar functionality keeping track of the day, month and year.

Here are the main features supported:

- Complete time of day clock: 12/24 hour, hours, minutes, seconds and hundredths
- Calendar function: day of week, date of month, month, year, century, leap year compensation, and year 2000 compliant.
- Alarm function: month, date, hour, minute, second and hundredths resolution
- Event function: can set interrupt for every roll over of month, day, hour, minute, second or hundredth-second
- Accuracy is: 1/100s
- User adjustable shifting accuracy is 1 UTC crystal clock cycle.

2. 5. 6. Timer with Dual PWM(PWMTimer)

There are 4 Timer with Dual PWM modules available in the chip. This block contains up to two 32-bit reloadable timers that can be used for timing, event counting, or generation of pulse-width modulated (PWM) signals.

The timers' features include:

- 32-bit reload counter
- Programmable prescaler with prescale values from 1 to 128
- PWM output generation

- Capture and compare capability
- External input pin for timer input, clock gating, or capture signal. External input pin signal frequency is limited to a maximum of one-fourth the system clock frequency.
- Timer output pin
- Timer interrupt
- Multiple operational mode supported.

2. 5. 7. Watch Dog Timer (WDT)

There is one WDT module available in the chip. WDT is a piece of hardware that can be used to automatically detect software anomalies and reset the processor if any abnormal occur. Generally speaking, a watchdog timer is based on a counter that counts down from some initial value to zero. The embedded software selects the counter's initial value and periodically restarts it. If the counter ever reaches zero before the software restarts it, the software is presumed to be malfunctioning and the processor's reset/interrupt signal is asserted.

This block is mainly used as the watchdog when enable the related bit, generate the reset when the counter counts down to zero(don't generate the interrupt).it can also be used as a regular timer when enable the related bit, generate the interrupt when the counter counts down to zero(don't generate the reset).

2. 5. 8. Advanced Encryption Standard (AES)

There is one AES engine available for customer security control. This block implements the Advanced Encryption Standard (AES), as described in the NIST Federal Information Processing Standard (FIPS) Publication 197 document.

Designed with ultimate flexibility in mind, the cores offer both encryption and decryption functions, plus it can support any available key-sizes (128/192/256-bit).

Here are the main features supported:

- Fully compliant with FIPS PUB 197, 2001 November 26
- Supports both encryption/decryption based on user's configuration
- Support both DMA mode and manual mode operation for encryption and decryption
- Support All NIST SP800-38A& SP800-38C AES operating modes: ECB, CBC, CTR， CFB, OFB, CCM

The AES engine automatically pads or masks misaligned last data blocks with zeroes for AES CCM (including misaligned AAD data).

2. 5. 9. DMA Controller

There is one DMA controller available in the chip. The DMAC module can support maximum 4 channels, two channels are dedicated for AES engine. And two channels are user configurable.

Here are the main features supported:

- Supports scatter-gather with DMA chaining.
- Hardware and software controlled transfer initiation.
- Supports burst transfer to maximize data bandwidth.
- Automatic address increment or decrement.
- Interrupt generation on transfer completion.
- Separate user interface for DMA control register programming.
- Supports misaligned data transfer.

2. 5. 10. GPIO

The GPIO Matrix module includes the general purpose input/output function and pin multiplexer function. The Matrix consists of 25 I/O pads and 60 peripheral pins. Any peripheral can be routed to any I/O pad based on configuration.

Functional description and Features

- Up to 25 GPIOs can be user configurable.
- Up to 60 peripheral pins can be mapped to any GPIO pad.
- Alternative control modes set by software or hardware;
- After reset, all the GPIO lines are configured as default inputs in software mode;
- Each pin can be uniquely setup in different modes.
- All can be used as GPIO, be able to latch input data and output data by software control
- Any GPIO can be configured as interrupt sources
- Data direction control by register or by peripheral behavior
- PAD output driving strength control
- Pull enable/disable control

2. 5. 11. QSPI

There is one QSPI controller available which used to access external Flash or SRAM. It can support single, dual or quad I/O mode. The DMA access is also supported for external Flash access. It can support XiP mode as well for user code.

2.6 System Operation

The chip will first boot from AP core, and AP core will start the firmware download progress.

2. 6. 1. Boot mode

Table 2- 1 Boot modes

BootModes	Notes
0	Boot from external FLASH
1	Boot from UART, can program FLASH at this mode

2. 6. 2. Operational mode

The HLK-N10 supports multiple operational mode for application. Here we'll talk about different mode one by one.

2.6.1.1 DEEPSLEEP mode

The is the ultra low power mode supported, in this mode, only UTC module is working. The 4K retention memory can be user selectable enabled or not. Here are the main operational features of these mode.

- All the CPU core will be off
- UTC keeps tracking the time.
- External pin or utc interrupt can be configurable wake up the system.
- Most of IO pads would lose power

2.6.1.2 STANDBY mode

The is the third level low power mode supported.

Here are the main operational features of these mode.

- All logic's state can be maintained in this mode.
- UTC keeps tracking the time.
- External pin or utc interrupt can be configurable wake up the system.
- All IO's state would be maintained.
- Up to 4 configurable GPIO can be used as wakeup source as well.

2.6.1.3 OPLPM mode

The is the low power mode used in ACTIVE mode.

Here are the main operational features of these mode.

- Each core can be configured to be off or in standby mode.
- Any peripheral or GPI can be used as wakeup source to wake it up..
- All IO's state would be maintained.

2.6.1.4 ACTIVE mode

In this mode, full application can be run, and this is the most power consumption mode as well.

2. 6. 3. Wakeup events from low power mode.

There are multiple wakeup sources available to wake up the system from low power mode. User might need to combine all the mode together to reach a low power goal.

2.7 Clocks

Table 2- 2 Clock Sources

ClockName	Description
Intosc_clk	Internal oscillator clock, 32khz;
Crystal_32k	32000hz or 32768hz crystal.
Crystal_CLK	38.4MHz

2.8 Reset Scheme

There are 3 global Reset in the chip.

- Power on Reset, low active
- External pin reset, high active
- Software reset from PRCM block, low active

3 Electrical Specifications

This section summarizes the electrical specifications supported by HLK-N10.

3.1 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the device, above which permanent damage may occur. These ratings are stress ratings only and functional operation of the device is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability.

Table 3- 1 Absolute Maximum Ratings

Parameter	Pin #	Conditions	MIN	TYP	MAX	Units
VBAT	16,25		-0.3		4.4	V
Reset/Wakeup	27		-0.3		4.0	V
GPIO	1-4, 19-22, 30-33, 35-41, 43-47, 51, 52		-0.3	1.8/3	3.3	V
RF signals	8, 10		-0.3		1.26	V
Analog signals	17, 18		-0.3		4.2	V
Temperature		Operating	-40	25	85	°C
		Storage	-40	25	125	°C
ESD Tolerance		HBM	2			kV

3.2 Operating Conditions

Table 3- 2 Operating Conditions

Specification	Symbol	MIN	TYP	MAX	Units	Notes
VBAT		3.1	3.6	4.2	V	
Reset/Wakeup		1.08	1.2	3.6	V	
Digital Input Voltage	Vih	2.7	3	3.3	V	

for GPIO0 ~ GPIO21	Vil	-0.3	0	0.3	V	
	Voh	2.7	3	3.3	V	
	Vol	-0.3	0	0.3	V	
Digital Input Voltage for GPIO22 ~ GPIO24	Vih	2.7	3	3.3	V	
	Vih1, Voh1	1.62	1.8	1.98	V	
	Vil	-0.3	0	0.3	V	
	Voh	2.7	3	3.3	V	
	Vol	-0.3	0	0.3	V	
IO Voltage for SIM, internal LDO	VDDIO2	2.7	3	3.3	V	Output accuracy ± 5%
	VDDIO2	1.62	1.8	1.98	V	
Current VDDIO2 output			30		mA	

3.3 Peripheral interface timing

3. 3. 1. SPI Interface

The SPI controller is working at typical temperature (25°C), assume the pin capacitance 10pF. The diagram below illustrates the worst scenario HLK-N10 supported.

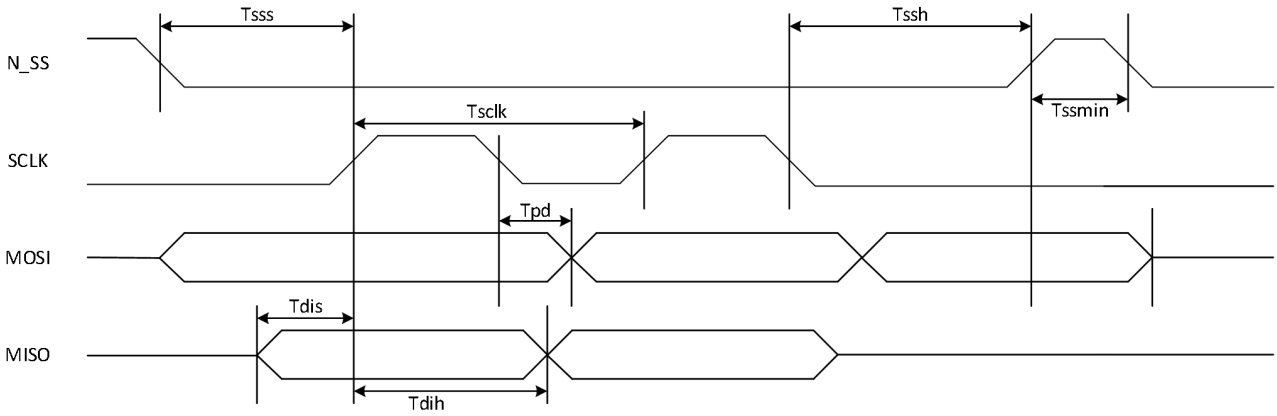


Figure 3- 1 SPI Master interface (CPOL=0,CPHA=0)

Table 3- 3 Timing of Master mode SPI

Work Mode	Symbol (ns)	Characteristics	Min(ns)	Max(ns)
Master	Tsss	N_SS Setup Time	27	
	Tssh	N_SS Hold Time	27	
	Tssmin	N_SS HIGH	54	
	Tpd	Output Delay	0.7	3.8
	Tdis	Data in Setup Time	25	
	Tdih	Data in Hold Time	29	
	Tsclk	SCLK period	54	

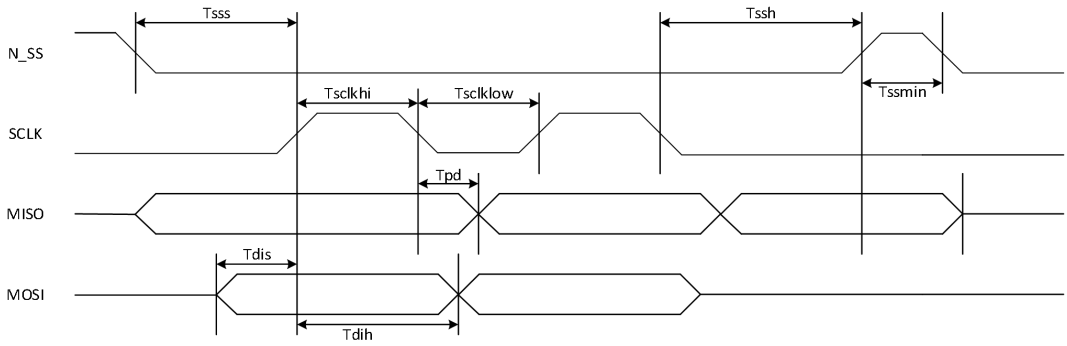


Figure 3- 2 SPI Slave interface (CPOL=0,CPHA=0)

Table 3- 4 Timing of Slaver mode SPI

Work Mode	Symbol (ns)	Characteristics	Min(ns)	Max(ns)
Slave	Tsss	N_SS Setup Time	16	
	Tssh	N_SS Hold Time	23.5	
	Tssmin	N_SS HIGH	53	
	Tpd	Output Delay	2.7	19.5
	Tdis	Data in Setup Time	-0.2	
	Tdih	Data in Hold Time	25.5	
	Tsclkhi	SCLK High period	26	
	Tsclklow	SCLK Low period	26	

3. 3. 2. CSP Interface (Configure as SPI, the other synchronous interface is similar as this)

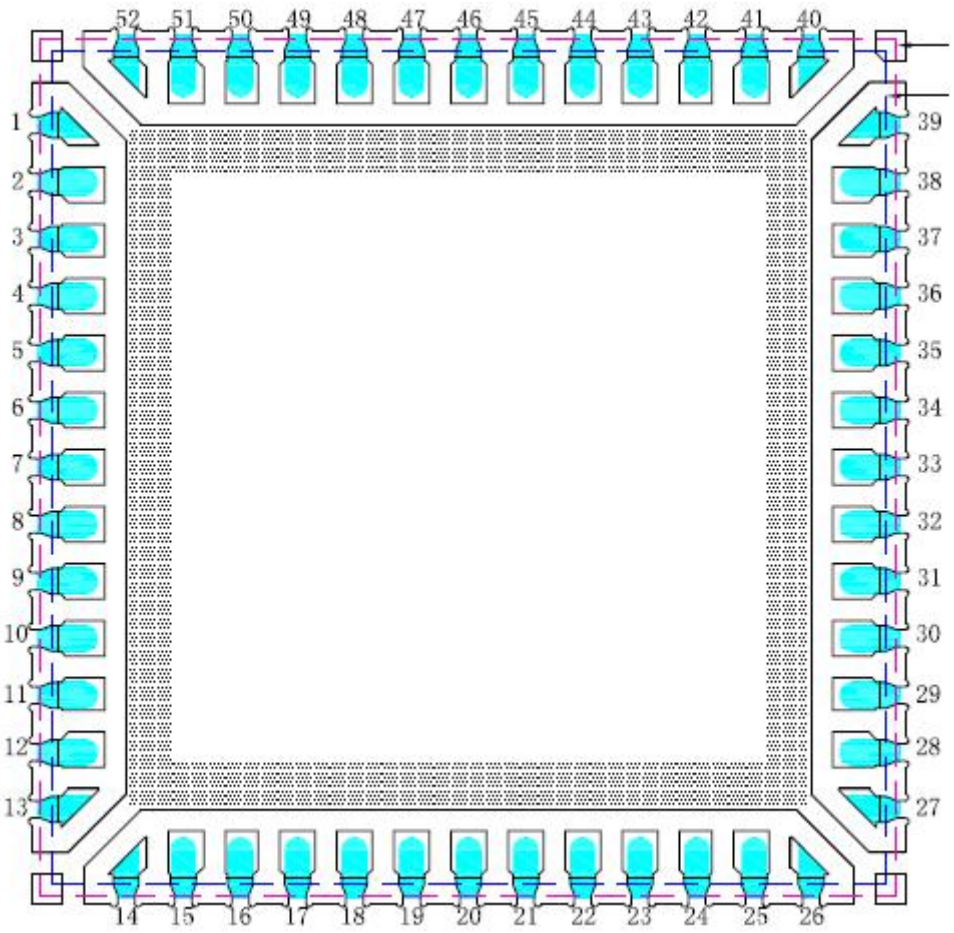
Assume 10pF load on all the connected pins.

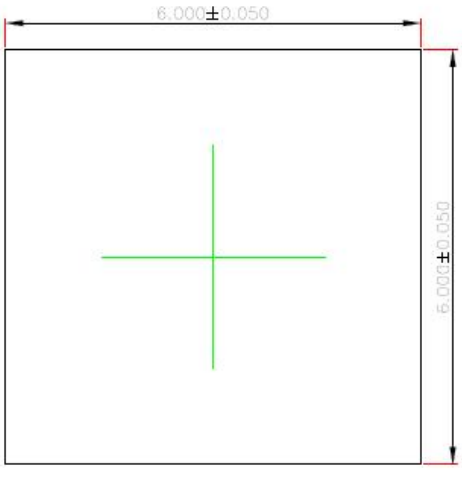
Work Mode	Symbol (ns)	Characteristics	Min	Max
Master	Tsss	N_SS Setup Time	35.5	
	Tssh	N_SS Hold Time	34	
	Tssmin	N_SS HIGH	69	
	Tpd	Output Delay	-1.4	1
	Tdis	Data in Setup Time	31	
	Tdih	Data in Hold Time	38	
	Tsclk	SCLK period	70	
Slave	Tsss	N_SS Setup Time	21	
	Tssh	N_SS Hold Time	23	
	Tssmin	N_SS HIGH	51.5	
	Tpd	Output Delay	4.0	25
	Tdis	Data in Setup Time	6.6	
	Tdih	Data in Hold Time	25	
	Tsclkhi	SCLK High period	26	
	Tsclklow	SCLK Low period	26	

3. 3. 3. UART Interface

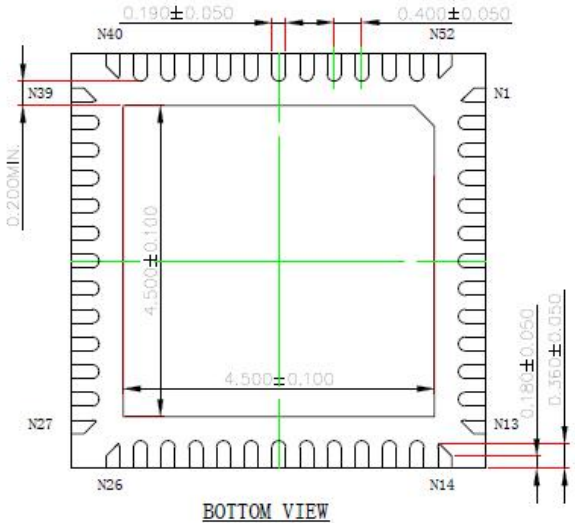
No matter user uses dedicated UART controller or use CSP to config as UART, the maximum baudrate could be up to 1Mbps

4 Package (QFN6X6-52L)

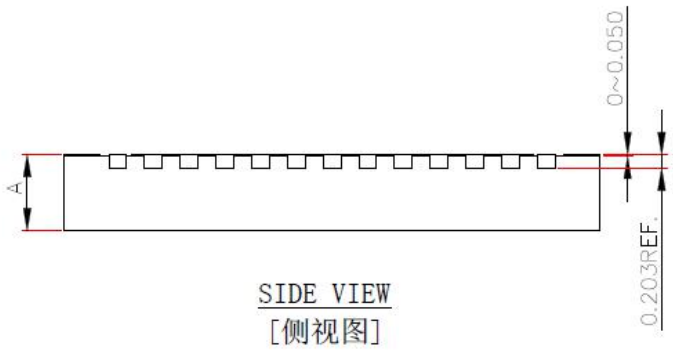




TOP VIEW
[顶视图]



BOTTOM VIEW
[背视图]



A	MIN.	NORM.	MAX.
	0.800	0.850	0.900

Figure 4- 1 52-pin 6mm x 6mm package information

Table 4- 1 Pinout Description

PIN NO.	PIN NAME	Description
1	GPIO3	Configurable GPIO
2	GPIO2	Configurable GPIO
3	GPIO1	Configurable GPIO
4	GPIO0	Configurable GPIO
5	Pad_i_VDD1P4_TRX_1	LDO input; 1.4v
6	Pad_i_VDD1P4_TRX_2	LDO input; 1.4v
7	AVSS	Analog ground
8	Pad_i_VIN_LNA_LB	LNA input for Low band
9	AVSS_LNA_LB	Low band LNA ground
10	Pad_i_VIN_LNA_HB	LNA input for high band
11	AVSS_LNA_HB	High band LNA ground
12	Pad_o_PAOUT_HB	PA output for high band
13	Pad_i_VDD3P3_PA	PA supply;
14	Pad_o_PAOUT_LB	PA output for Low band
15	Pad_o_VOUT3P3_PALDO	PA supply; from PALDO
16	Pad_i_VBATA	Battery input for other circuit, clean; 3.1-4.2
17	Pad_io_Sensor_Test1	Sensor ADC ch1 input/Test

18	Pad_io_Sensor_Test2	Sensor ADC ch2 input/Test
19	GPIO24	Configurable GPIO
20	GPIO23	Configurable GPIO
21	GPIO22	Configurable GPIO
22	VDDIO2	IO supply 1.8/3v selectable for GPIO22~GPIO24, put external cap here
23	Pad_i_XTAL32K	32kHz XTAL input
24	Pad_o_XTAL32K	32kHz XTAL output
25	Pad_i_VBATP	Battery supply. 3.1-4.2
26	Pad_o_VSW	BUCK switching output;
27	Pad_i_WKUP_EN	Force wake-up pin for customer and user Reset pin. Internal pulldown resistor. High active Range: Low: < 0.3v; High, 1.1v ~3.3v;
28	Pad_i_VDD1P4	LDO input, 1.4v
29	VDDCORE_R	Connect with VDDCORE_T pad on board, external cap here
30	GPIO21	Configurable GPIO
31	GPIO20	Configurable GPIO
32	GPIO19	Configurable GPIO
33	GPIO18	Configurable GPIO
34	VDDIO1_R	IO supply, from IOLDO, external cap is needed, Connect with VDDIO1_T externally
35	GPIO17	Configurable GPIO
36	GPIO16	Configurable GPIO
37	GPIO15	Configurable GPIO
38	GPIO14	Configurable GPIO
39	GPIO13	Configurable GPIO
40	GPIO11	Configurable GPIO

41	GPIO12	Configurable GPIO
42	VDDIO1_T	IO supply, connect with VDDIO1_R on board
43	GPIO10	Configurable GPIO
44	GPIO9	Configurable GPIO
45	GPIO8	Configurable GPIO
46	GPIO7	Configurable GPIO
47	GPIO6	Configurable GPIO
48	VDDCORE_T	Connect with VDDCORE_R, put external cap here
49	Pad_o_XTAL	Typical Crystal 38.4M output
50	Pad_i_XTAL	Typical Crystal 38.4M input
51	GPIO5	Configurable GPIO
52	GPIO4	Configurable GPIO

5 Revision History

Revision	Date	Description
1.0	2020/7/14	First draft