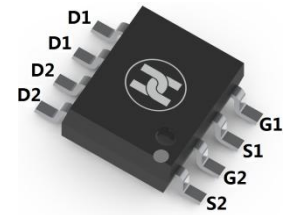
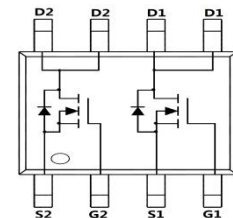


Dual N-Channel Enhancement Mode Field Effect Transistor
FEATURES

- Low on-resistance: $V_{DS}=30V, I_D=10A, R_{DS(ON)} \leq 13m\Omega @ V_{GS}=10V$
- Low gate charge
- For high side switch in SMPS and general purpose applications.
- Surface Mount device


SOP-8

MECHANICAL DATA

- Case: SOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Weight: 0.3 grams (approximate)

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current	I_D	$T_A = 25^\circ\text{C}$	10
		$T_A = 70^\circ\text{C}$	8
Pulsed drain current	I_{DM}	55	A
Avalanche current	I_{AS}, I_{AR}	22	A
Avalanche energy $L=0.1\text{mH}$	E_{AS}, E_{AR}	24	mJ
Power dissipation	P_D	$T_A = 25^\circ\text{C}$	2
		$T_A = 70^\circ\text{C}$	1.3
Thermal resistance from Junction to ambient	$R_{\theta JA}$	90	$^\circ\text{C/W}$
Thermal resistance from Junction to Lead	$R_{\theta JL}$	40	$^\circ\text{C/W}$
Junction temperature	T_J	150	$^\circ\text{C}$
Storage temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DSS}^*$	30			V	$V_{GS}=0V, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}^*			1	μA	$V_{DS}=30V, V_{GS}=0V$
Gate-body leakage current	I_{GSS}^*			± 100	nA	$V_{DS}=0V, V_{GS}=\pm 20V$
Gate-threshold voltage	$V_{GS(th)}^*$	1.5	1.9	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
On-State Drain Current	$I_{D(ON)}$	55			A	$V_{DS}=5V, V_{GS}=10V$
Drain-source on-resistance	$R_{DS(ON)}^*$		10.8	13	m Ω	$V_{GS}=10V, I_D=10A,$
			15.5	19	m Ω	$V_{GS}=10V, I_D=10A, T_J=125^\circ\text{C}$
			14	17.5	m Ω	$V_{GS}=4.5V, I_D=8A$
Forward transconductance	g_{FS}		43		S	$V_{DS}=5V, I_D=10A$
Diode forward voltage	V_{SD}		0.75	1	V	$I_S=1A, V_{GS}=0V$
Diode forward current	I_S			2.5	A	
Input capacitance	C_{iss}	610	760	910	pF	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$
Output capacitance	C_{oss}	88	125	160	pF	
Reverse transfer capacitance	C_{rss}	40	70	100	pF	
Gate resistance	R_g	0.8	1.6	2.4	Ω	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$
Total gate charge	Q_g	5	6.6	8	nC	$V_{GS}=4.5V, V_{DS}=15V, I_D=10A$
		11	14	17	nC	
Gate-source charge	Q_{gs}		2.4		nC	$V_{GS}=10V, V_{DS}=15V, I_D=10A$
Gate-drain charge	Q_{gd}		3		nC	
Turn-on delay time	$t_{d(on)}$		4.4		nS	$V_{GS}=10V, V_{DS}=15V,$ $R_{GEN}=3\Omega, R_L=1.5\Omega$
Turn-on rise time	t_r		9		nS	
Turn-off delay time	$t_{d(off)}$		17		nS	
Turn-off fall time	t_f		6		nS	
Body Diode Reverse Recovery Time	t_{rr}	5.5	7	8	nS	
Body Diode Reverse Recovery Charge	Q_{rr}	6.4	8	9.6	nC	$I_F=10A, di/dt=500A/\mu s$

*Pulse test ; Pulse width =80 μs , Duty cycle $\leq 0.5\%$.

Dual N-Channel Enhancement Mode Field Effect Transistor

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

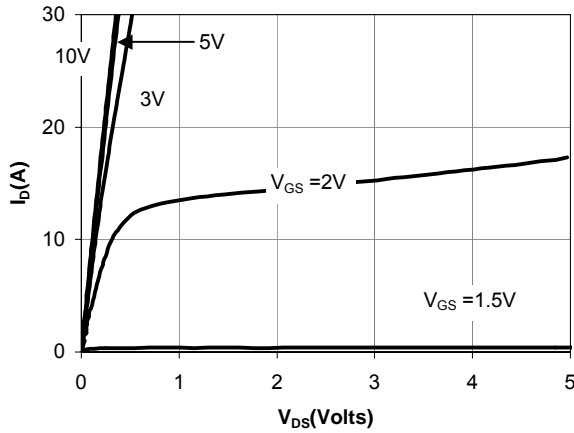


Figure 1: On-Regions Characteristics

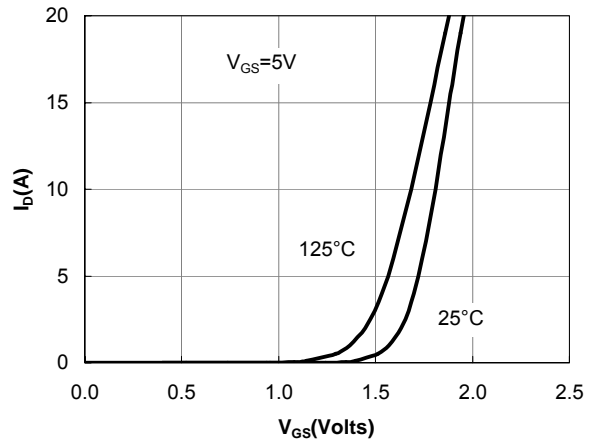


Figure 2: Transfer Characteristics

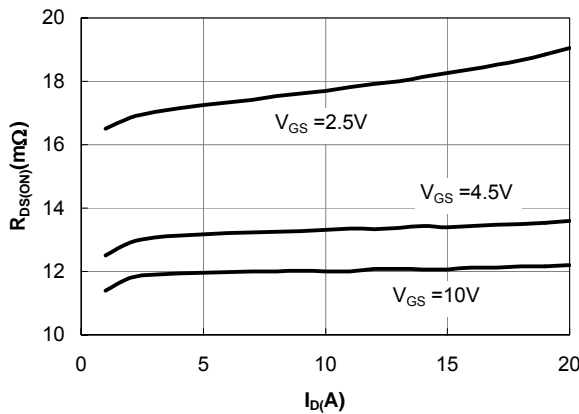


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

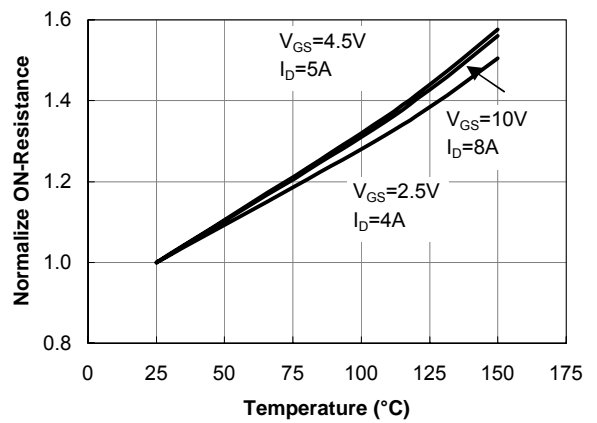


Figure 4: On-Resistance vs. Junction Temperature

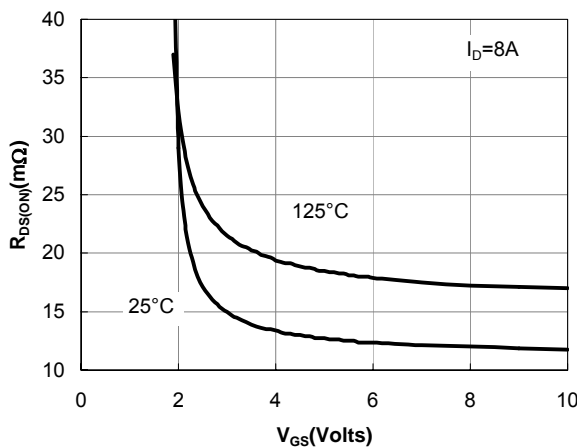


Figure 5: On-Resistance vs. Gate-Source Voltage

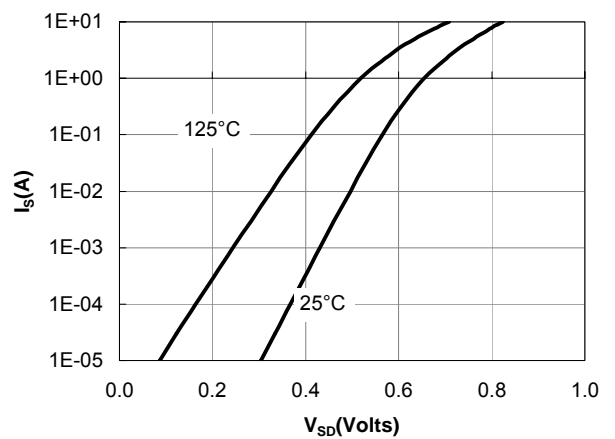


Figure 6: Body-Diode Characteristics

Dual N-Channel Enhancement Mode Field Effect Transistor

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

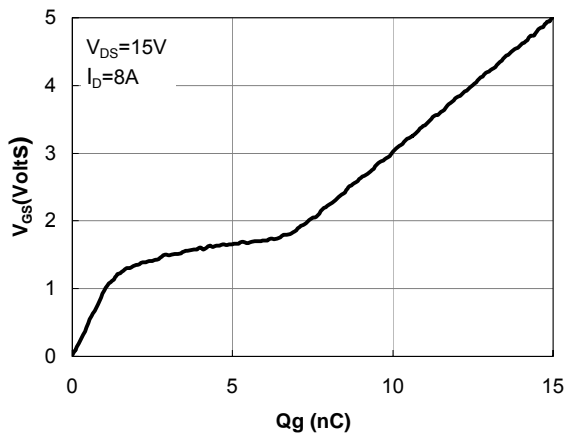


Figure 7: Gate-Charge Characteristics

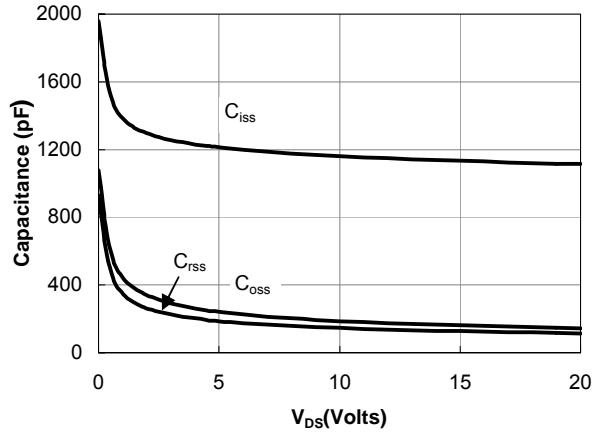


Figure 8: Capacitance Characteristics

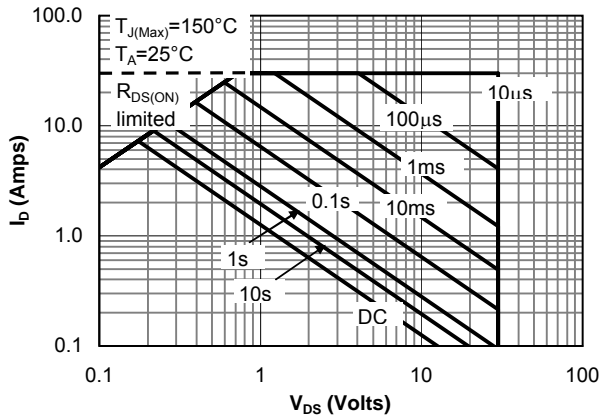


Figure 9: Maximum Forward Biased Safe Operating Area

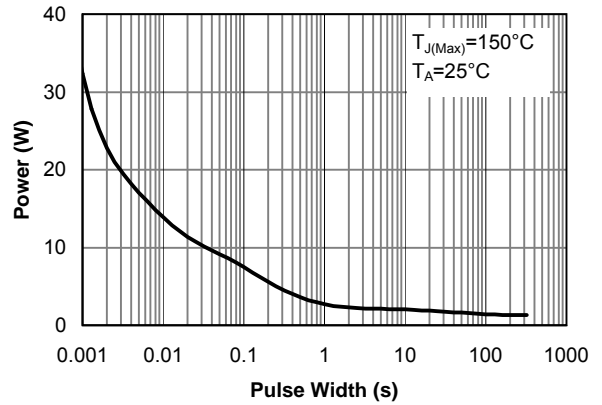


Figure 10: Single Pulse Power Rating Junction-to-Ambient

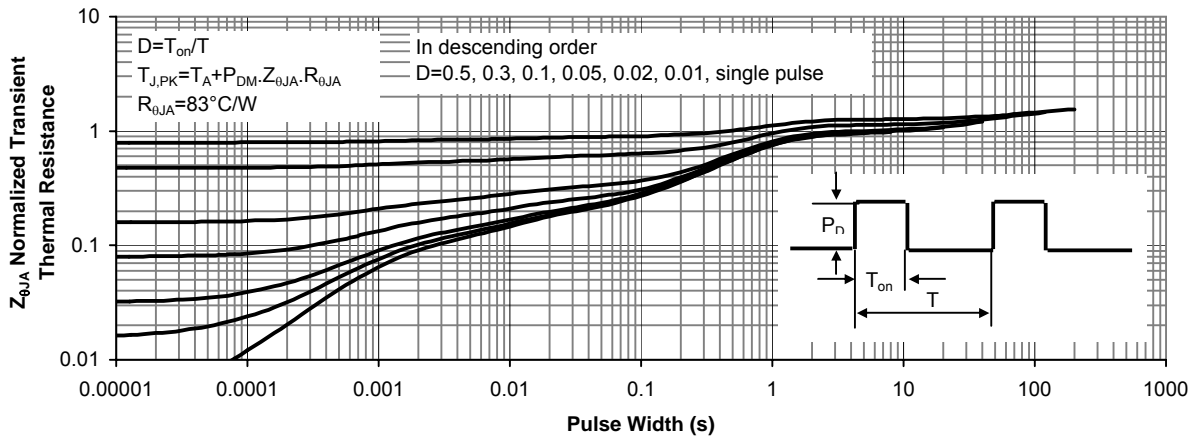


Figure 11: Normalized Maximum Transient Thermal Impedance

Dual N-Channel Enhancement Mode Field Effect Transistor

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

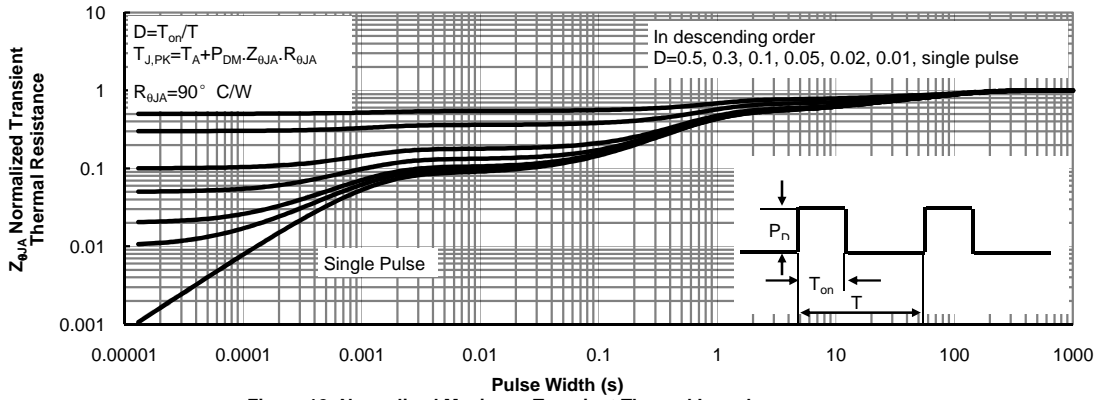
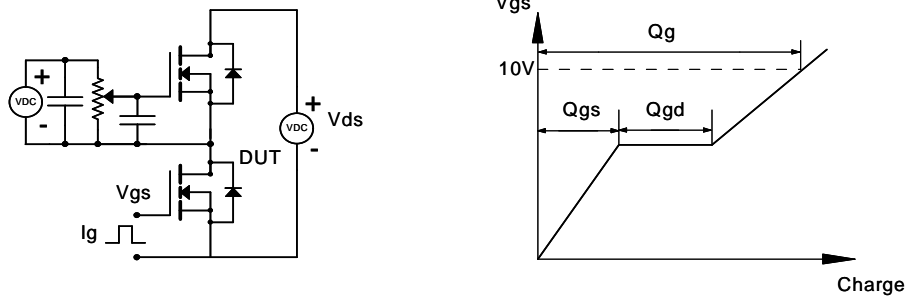


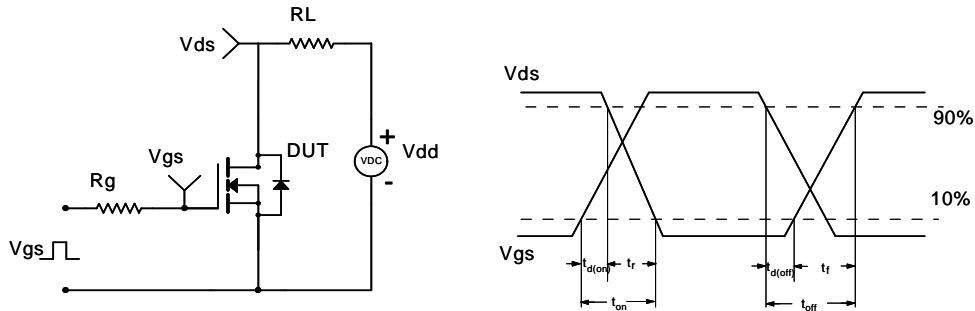
Figure 12: Normalized Maximum Transient Thermal Impedance

Dual N-Channel Enhancement Mode Field Effect Transistor

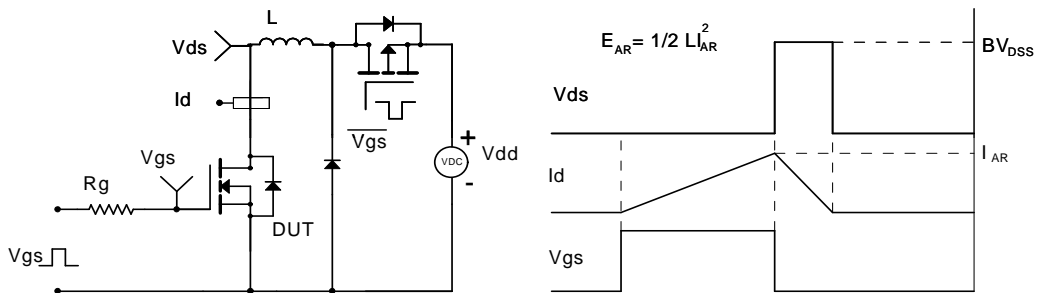
Gate Charge Test Circuit & Waveform



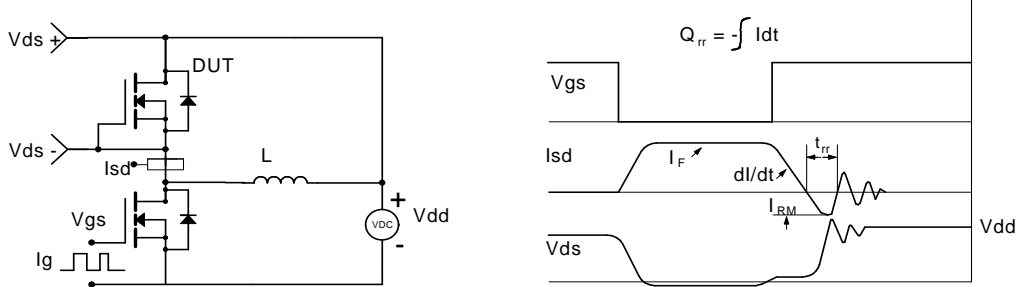
Resistive Switching Test Circuit & Waveforms

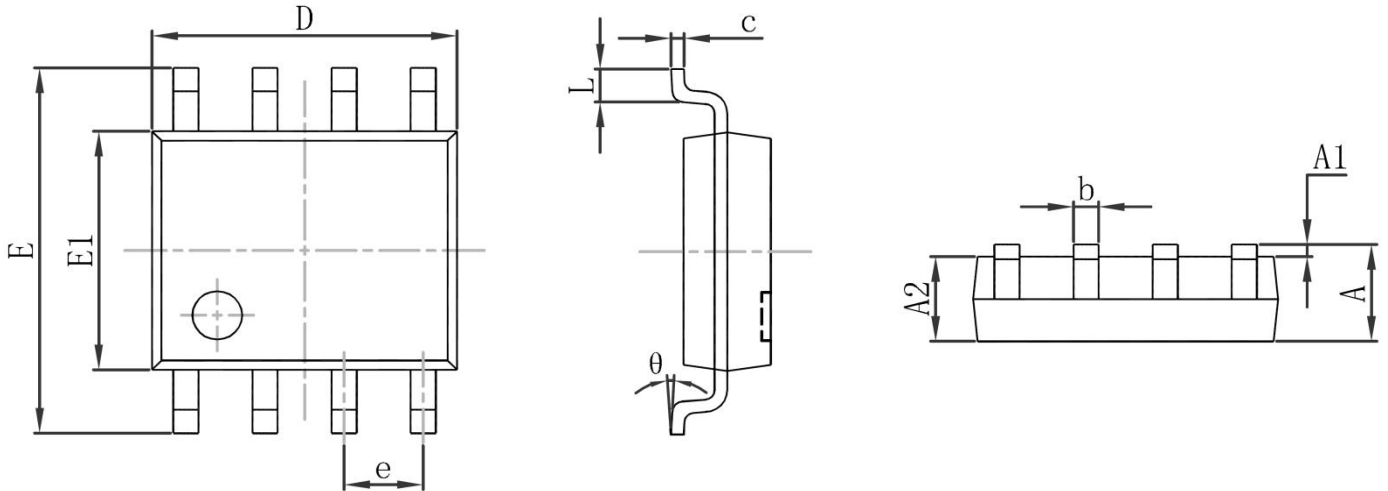


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

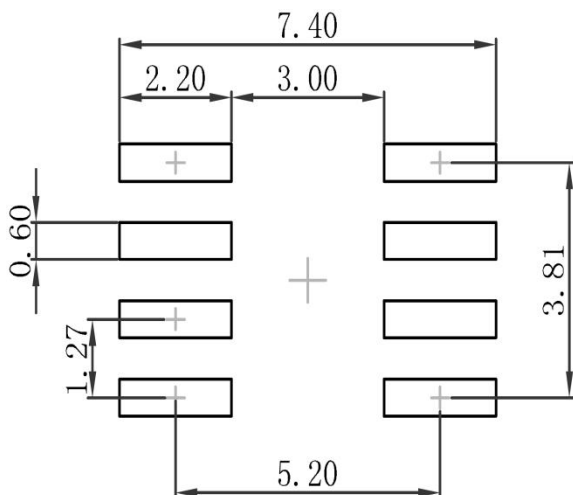


Diode Recovery Test Circuit & Waveforms



Dual N-Channel Enhancement Mode Field Effect Transistor
SOP-8 Package Outline Dimensions


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

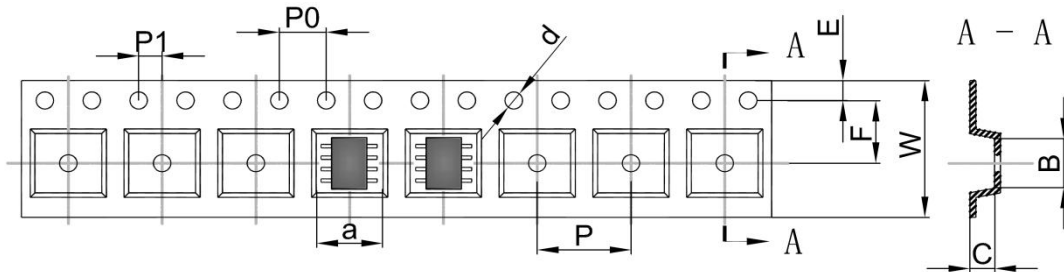
SOP-8 Suggested Pad Layout

Note:

1. Controlling dimension: in millimeters
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only

Dual N-Channel Enhancement Mode Field Effect Transistor

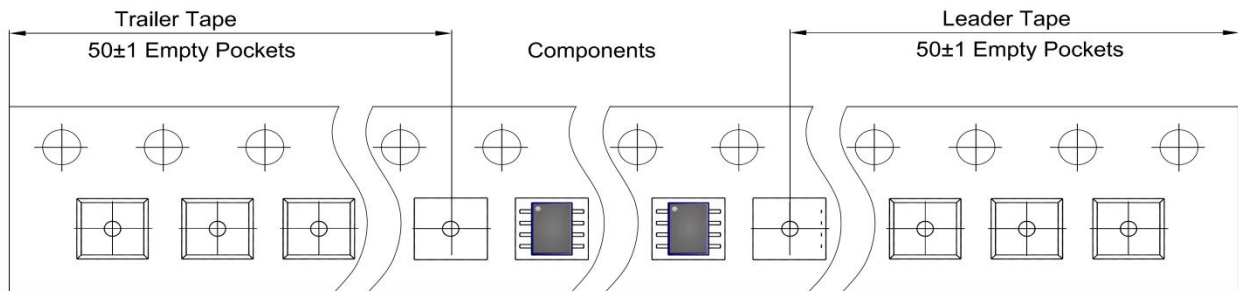
SOP-8 Tape and Reel

SOP-8 Embossed Carrier Tape

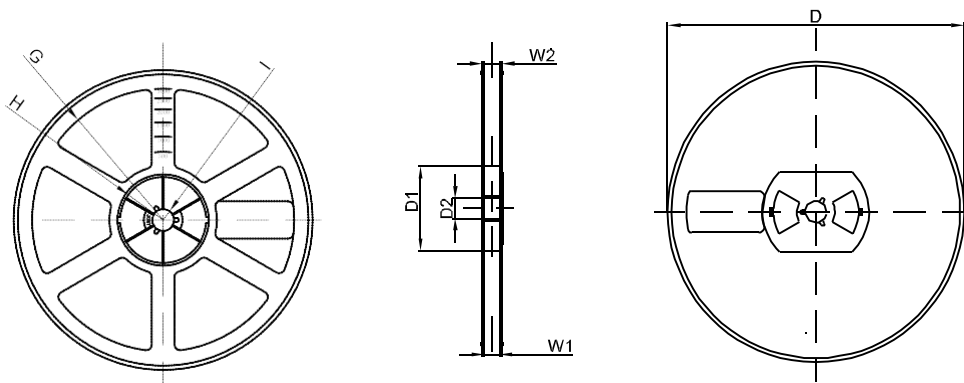


DIMENSIONS ARE IN MILLIMETER										
TYPE	A	B	C	d	E	F	P0	P	P1	W
SOP-8	6.40	5.40	2.10	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

SOP-8 Tape Leader and Trailer



SOP-8 Reel



DIMENSIONS ARE IN MILLIMETER								
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13" DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1