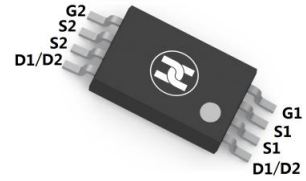
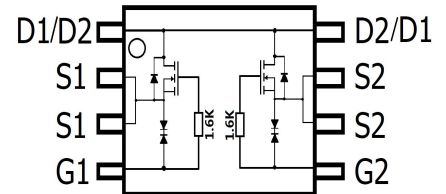


**DUAL N-CHANNEL ENHANCEMENT MODE FET**
**FEATURES**

- Ultra low on-resistance:  $V_{DS}=20V, I_D=6A, R_{DS(ON)} \leq 27m\Omega @ V_{GS}=10V$
- Low gate charge
- ESD protected
- Surface Mount device


**TSSOP-8**

**MECHANICAL DATA**

- Case: TSSOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Weight: not available

**MAXIMUM RATINGS ( $T_A = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Value	Unit
Drain-source voltage	$V_{DS}$	20	V
Gate-source voltage	$V_{GS}$	$\pm 12$	V
Continuous drain current	$I_D$	$T_A = 25^\circ C$	6
		$T_A = 70^\circ C$	4.8
Pulsed drain current	$I_{DM}$	30	A
Power dissipation	$P_D$	$T_A = 25^\circ C$	1.5
		$T_A = 70^\circ C$	0.94
Thermal resistance from Junction to ambient	$R_{\theta JA}$	140	$^\circ C/W$
Thermal resistance from Junction to Lead	$R_{\theta JL}$	85	$^\circ C/W$
Junction temperature	$T_J$	150	$^\circ C$
Storage temperature	$T_{STG}$	-55 ~ +150	$^\circ C$

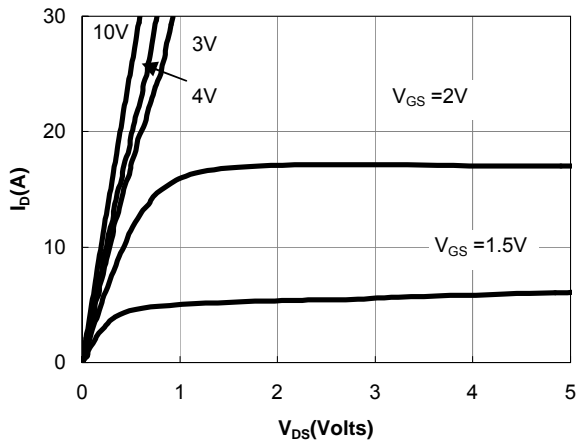
**ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ C$  unless otherwise specified)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DSS}^*$	20			V	$V_{GS}=0V, I_D=250\mu A$
Zero gate voltage drain current	$I_{DSS}^*$			1	$\mu A$	$V_{DS}=16V, V_{GS}=0V$
Gate-body leakage current	$I_{GSS}^*$			$\pm 10$	$\mu A$	$V_{DS}=0V, V_{GS}=\pm 10V$
					V	$V_{DS}=0V, I_G=\pm 250\mu A$
Gate-threshold voltage	$V_{GS(th)}^*$	0.5	0.6	1	V	$V_{DS}=V_{GS}, I_D=1mA$
On-State Drain Current	$I_{D(ON)}^*$	30			A	$V_{DS}=5V, V_{GS}=4.5V$
Drain-source on-resistance	$R_{DS(ON)}^*$	16	22	27	m $\Omega$	$V_{GS}=10V, I_D=6A$
				31	m $\Omega$	$V_{GS}=10V, I_D=6A, T_J=125^\circ C$
		19	25	30	m $\Omega$	$V_{GS}=4.5V, I_D=5A$
		22	30	37	m $\Omega$	$V_{GS}=3.1V, I_D=4A$
		25	32	41	m $\Omega$	$V_{GS}=2.5V, I_D=4A$
		32	42	55	m $\Omega$	$V_{GS}=1.8V, I_D=2A$
Forward transconductance	$g_{FS}$		21		S	$V_{DS}=5V, I_D=6A$
Diode forward voltage	$V_{SD}$		0.75	1	V	$I_S=1A, V_{GS}=0V$
Diode forward current	$I_S$			2.5	A	
Input capacitance	$C_{iss}$		290		pF	$V_{DS}=10V, V_{GS}=0V, f=1MHz$
Output capacitance	$C_{oss}$		120		pF	
Reverse transfer capacitance	$C_{rss}$		40		pF	
Gate resistance	$R_g$		1.6		K $\Omega$	$V_{DS}=0V, V_{GS}=0V, f=1MHz$
Total gate charge	$Q_g$		5.2		nC	$V_{GS}=4.5V, V_{DS}=10V, I_D=6A$
Gate-source charge	$Q_{gs}$		2.1		nC	
Gate-drain charge	$Q_{gd}$		1.9		nC	
Turn-on delay time	$t_{d(on)}$		280		nS	$V_{GS}=4.5V, V_{DS}=10V, R_{GEN}=3\Omega, R_L=1.7\Omega$
Turn-on rise time	$t_r$		972		nS	
Turn-off delay time	$t_{d(off)}$		2.35		$\mu S$	
Turn-off fall time	$t_f$		2.2		$\mu S$	
Body Diode Reverse Recovery Time	$t_{rr}$		25		nS	
Body Diode Reverse Recovery Charge	$Q_{rr}$		8		nC	$I_F=6A, di/dt=100A/\mu S, V_{GS}=-9V$

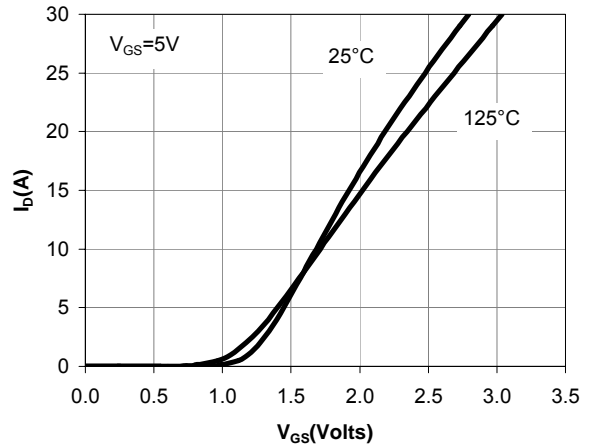
\*Pulse test ; Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 0.5\%$  .

**DUAL N-CHANNEL ENHANCEMENT MODE FET**

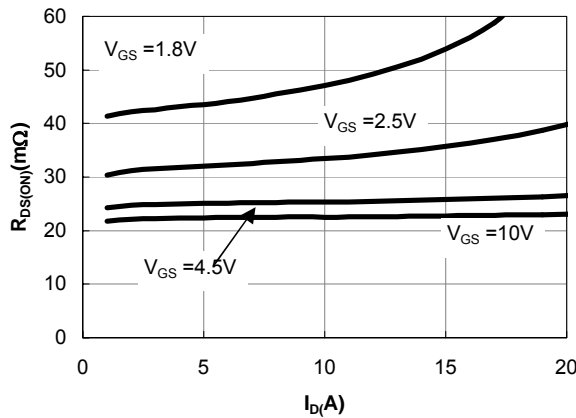
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



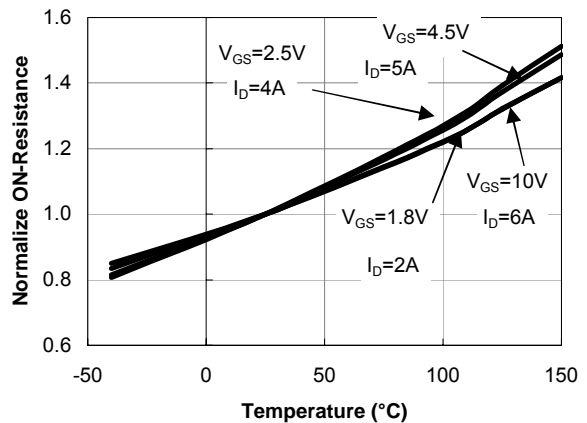
**Figure 1: On-Regions Characteristic CS**



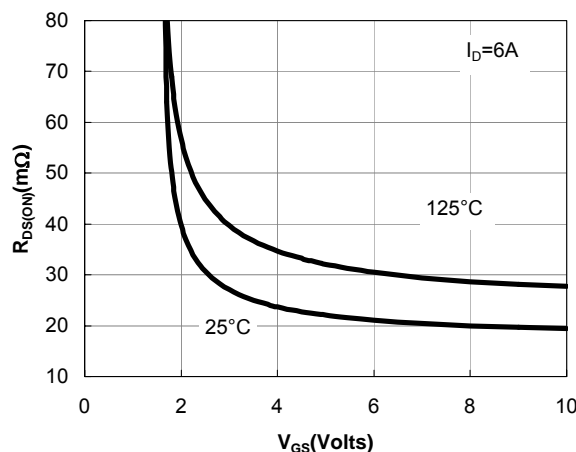
**Figure 2: Transfer Characteristics**



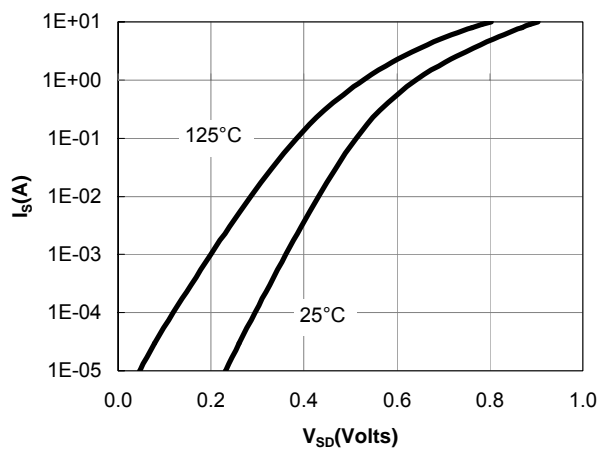
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



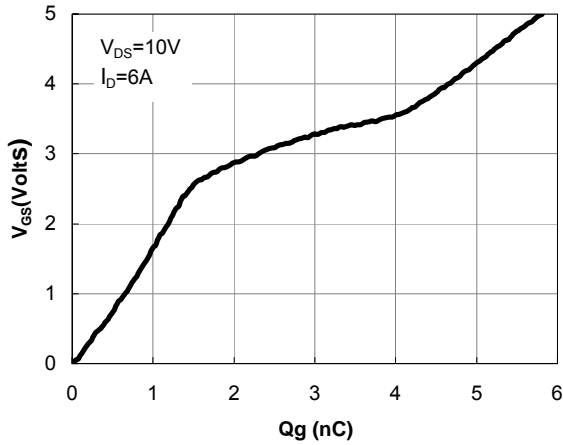
**Figure 5: On-Resistance vs. Gate-Source Voltage**



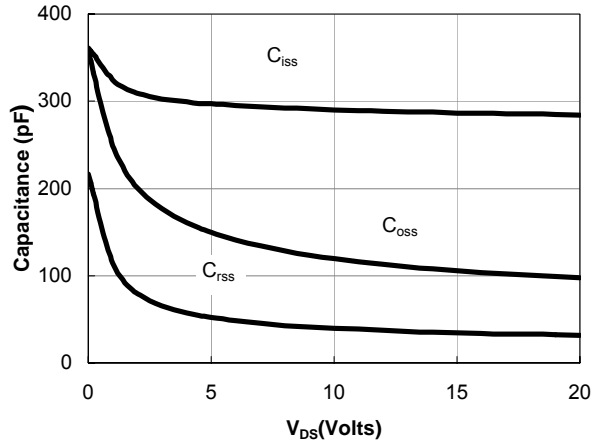
**Figure 6: Body-Diode Characteristics**

**DUAL N-CHANNEL ENHANCEMENT MODE FET**

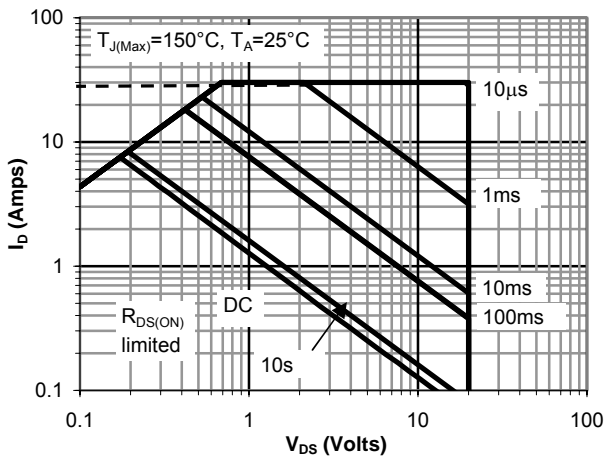
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



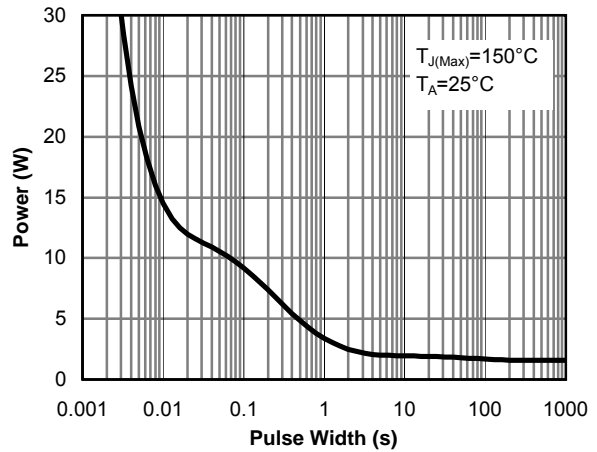
**Figure 7: Gate-Charge Characteristics**



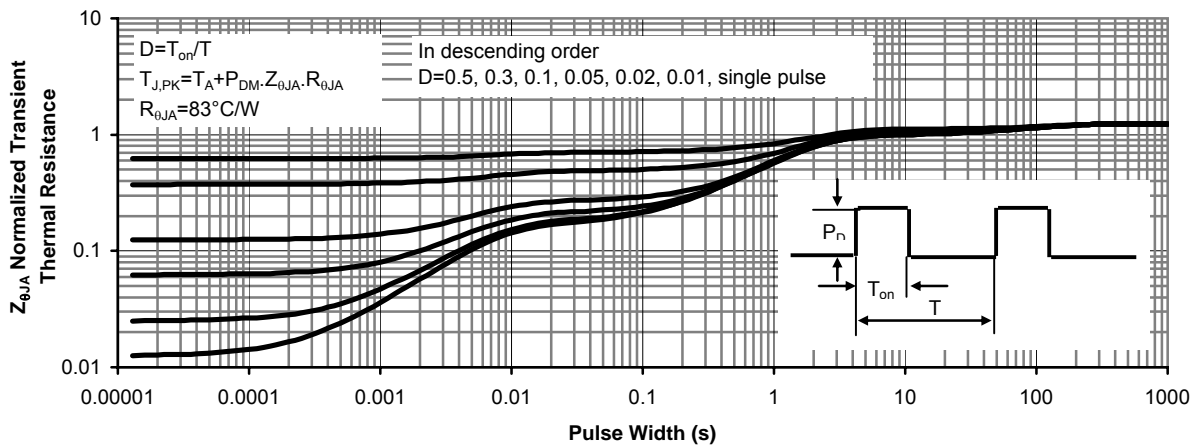
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area**



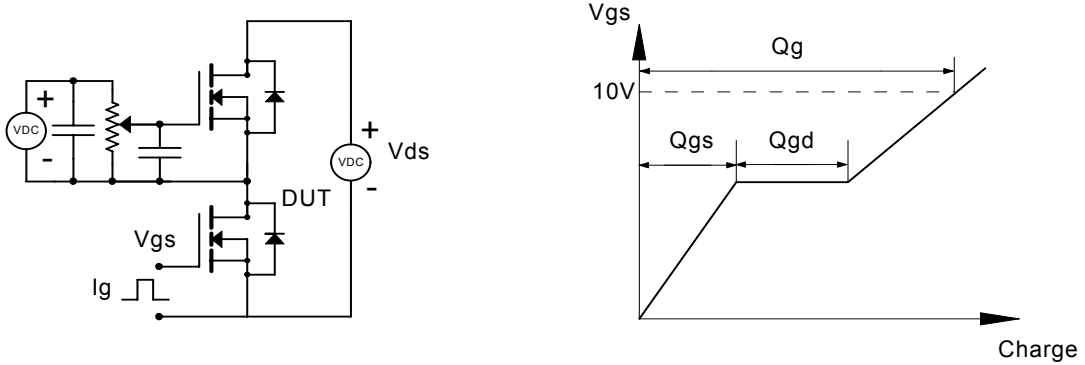
**Figure 10: Single Pulse Power Rating Junction-to-Ambient**



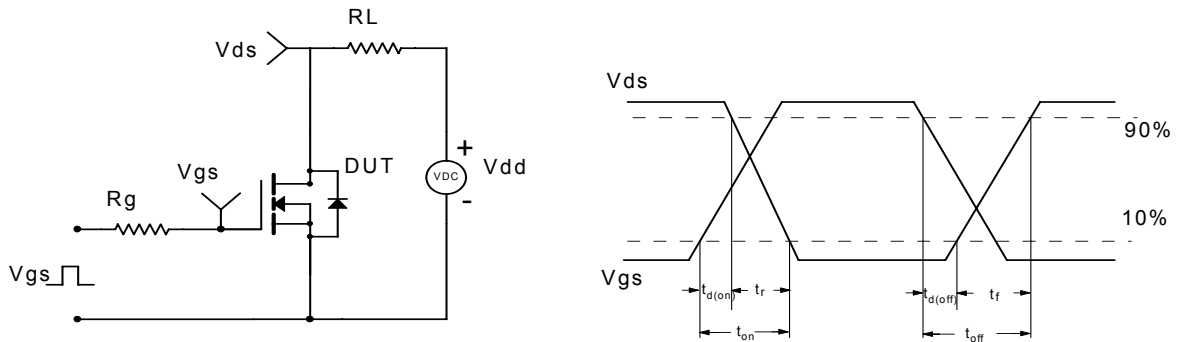
**Figure 11: Normalized Maximum Transient Thermal Impedance**

**DUAL N-CHANNEL ENHANCEMENT MODE FET**

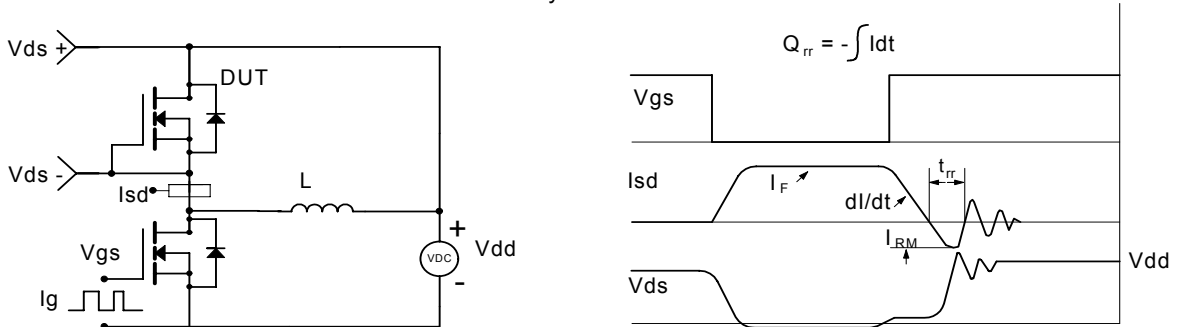
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

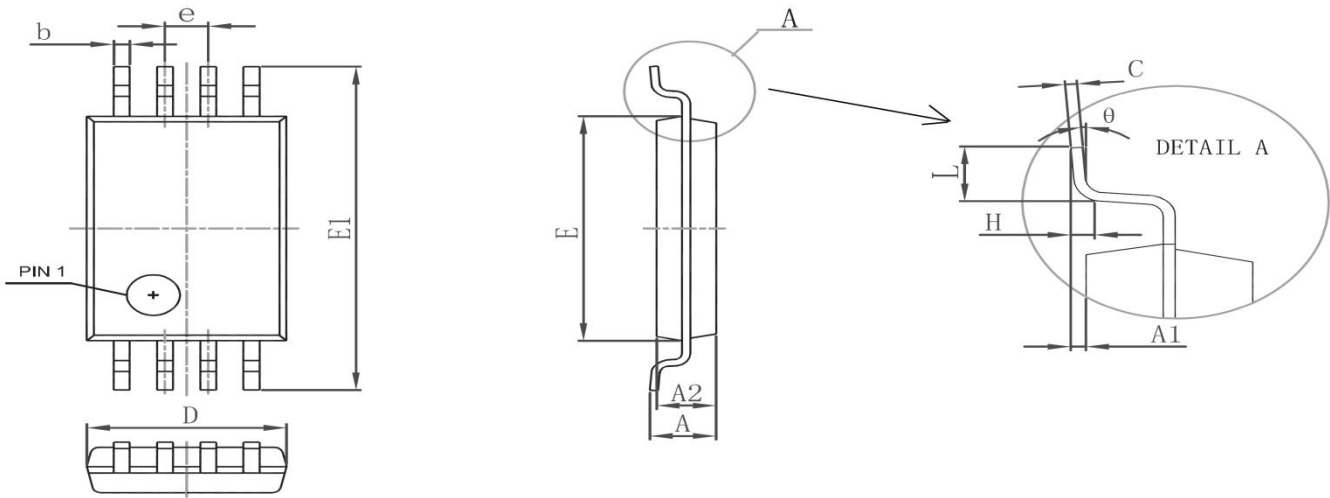


Diode Recovery Test Circuit & Waveforms



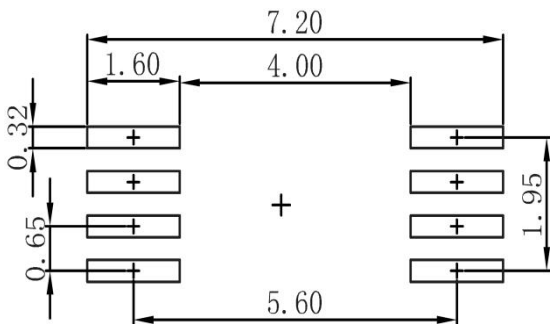
**DUAL N-CHANNEL ENHANCEMENT MODE FET**

**SOP-8 Package Outline Dimensions**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
$\theta$	1°	7°	1°	7°

**SOP-8 Suggested Pad Layout**



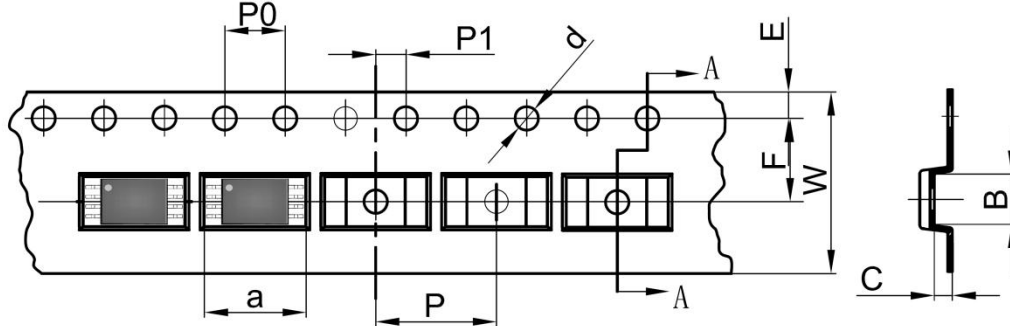
**Note:**

1. Controlling dimension: in millimeters
2. General tolerance:  $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only

## DUAL N-CHANNEL ENHANCEMENT MODE FET

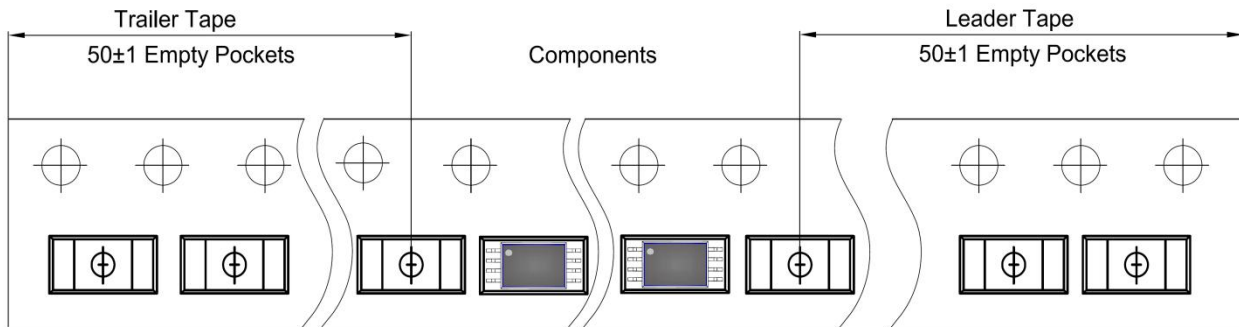
### SOP-8 Tape and Reel

#### SOP-8 Embossed Carrier Tape

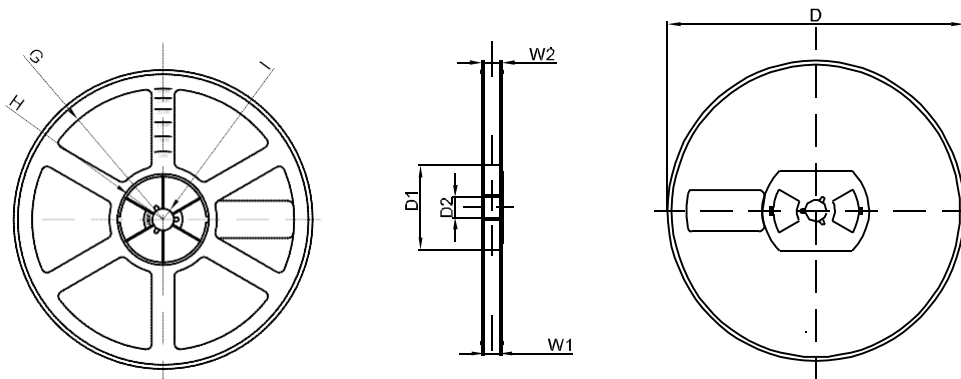


DIMENSIONS ARE IN MILLIMETER										
TYPE	a	B	C	d	E	F	P0	P	P1	W
SOP-8	6.76	3.30	1.20	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

#### SOP-8 Tape Leader and Trailer



#### SOP-8 Reel



DIMENSIONS ARE IN MILLIMETER								
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13" DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1