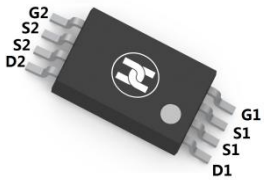
DUAL P-CHANNEL ENHANCEMENT MODE FET

FEATURES

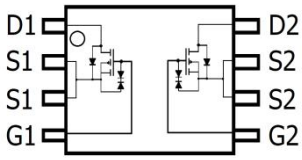
- Ultra low on-resistance:V_{DS}=-12V,I_D=-6.5A,$R_{DS(ON)}$≤20mΩ@V_{GS}=-4.5V
- Low gate charge
- ESD protected
- Surface Mount device



TSSOP-8

MECHANICAL DATA

- Case: TSSOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Weight: not available



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-source voltage		V_{DS}	-12	V
Gate-source voltage		V_{GS}	±8	V
Continuous drain current	T_A = 25°C	I_D	-6.5	A
	T_A = 70°C		-5	A
Pulsed drain current		I_{DM}	-60	A
Power dissipation	T_A = 25°C	P_D	1.4	W
	T_A = 70°C		0.9	W
Thermal resistance from Junction to ambient		$R_{\theta JA}$	125	°C/W
Thermal resistance from Junction to Lead		$R_{\theta JL}$	75	°C/W
Junction temperature		T_J	150	°C
Storage temperature		T_{STG}	-55 ~+150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DSS}$*	-12			V	V_{GS}=0V, I_D=250μA
Zero gate voltage drain current	I_{DSS}*			-1	μA	V_{DS}=-12V, V_{GS}=0V
				-5	μA	V_{DS}=-12V,V_{GS}=0V,T_J=55°C
Gate-body leakage current	I_{GSS}*			±10	μA	V_{DS}=0V, V_{GS}=±8V
Gate-threshold voltage	$V_{GS(th)}$*	-0.35	-0.53	-0.85	V	V_{DS}=V_{GS}, I_D=-250μA
On-State Drain Current	$I_{D(ON}$	-60			A	V_{DS}=-5V, V_{GS}=-4.5V
Drain-source on-resistance	$R_{DS(ON)}$*		16	20	mΩ	V_{GS}=-4.5V, I_D=-6.5A
			23	28	mΩ	V_{GS}=-4.5V,I_D=-6.5A,T_J=125°C
			19	24	mΩ	V_{GS}=-2.5V, I_D=-6A
			23	30	mΩ	V_{GS}=-1.8V, I_D=-5.5A
			28	36	mΩ	V_{GS}=-1.5V, I_D=-5A
Forward transconductance	g_{FS}		45		S	V_{DS}=-5V, I_D=-6.5A
Diode forward voltage	V_{SD}		-0.56	-1	V	I_S=-1A, V_{GS}=0V
Diode forward current	I_S			-1.4	A	
Input capacitance	C_{iss}		1740	2100	pF	V_{DS}=-6V, V_{GS}=0V, f=1MHz
Output capacitance	C_{oss}		334		pF	
Reverse transfer capacitance	C_{rss}		200		pF	
Gate resistance	R_g		1.3	1.7	Ω	V_{DS}=0V, V_{GS}=0V, f=1MHz
Total gate charge	Q_g		19	23	nC	V_{GS}=-4.5V,V_{DS}=-6V,I_D=-6.5A
Gate-source charge	Q_{gs}		4.5		nC	
Gate-drain charge	Q_{gd}		5.3		nC	
Turn-on delay time	$t_{d(on)}$		240		nS	V_{GS}=-4.5V, V_{DS}=-6V, R_{GEN}=3Ω,R_L=0.9Ω
Turn-on rise time	t_r		580		nS	
Turn-off delay time	$t_{d(off)}$		7		nS	
Turn-off fall time	t_f		4.2		nS	
Body Diode Reverse Recovery Time	t_{rr}		22	27	nS	I_F=-6.5A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge	Q_{rr}		17		nC	I_F=-6.5A, dI/dt=100A/μs

*Pulse test ; Pulse width ≤300μs, Duty cycle ≤ 0.5% .

DUAL P-CHANNEL ENHANCEMENT MODE FET

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

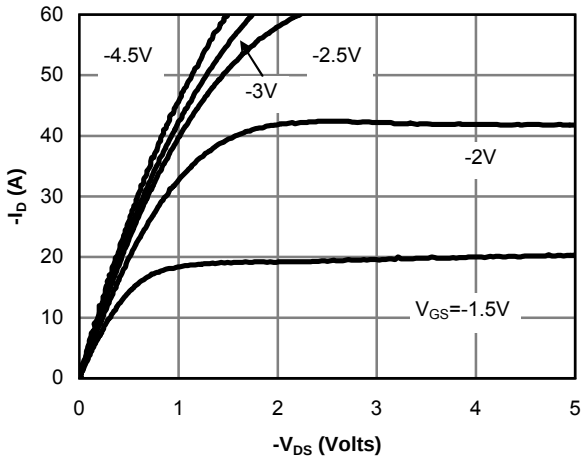


Figure 1: On-Region Characteristics

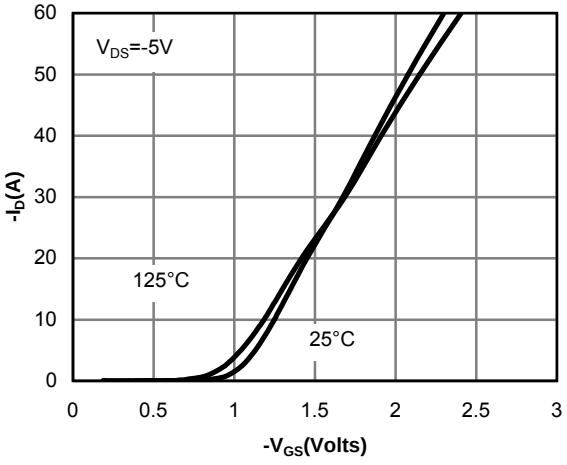


Figure 2: Transfer Characteristics

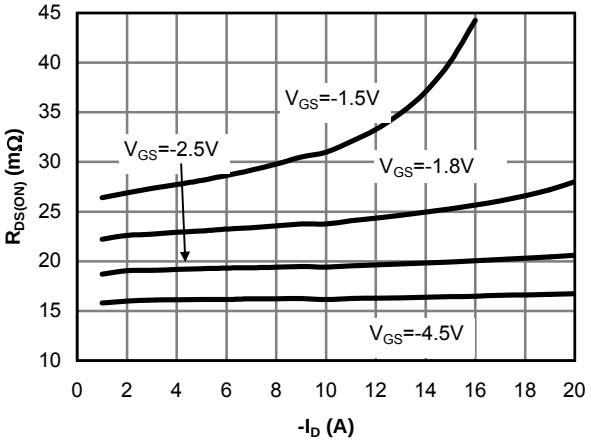


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

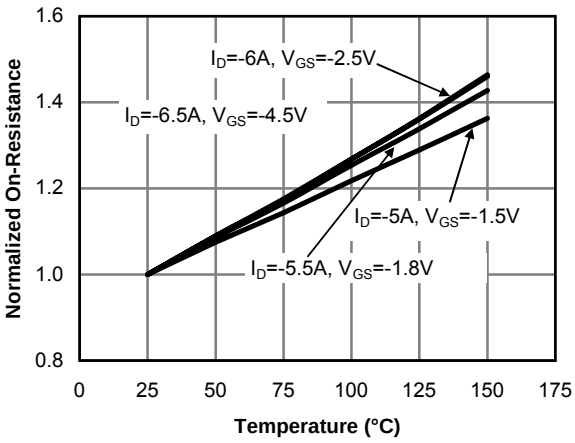


Figure 4: On-Resistance vs. Junction Temperature

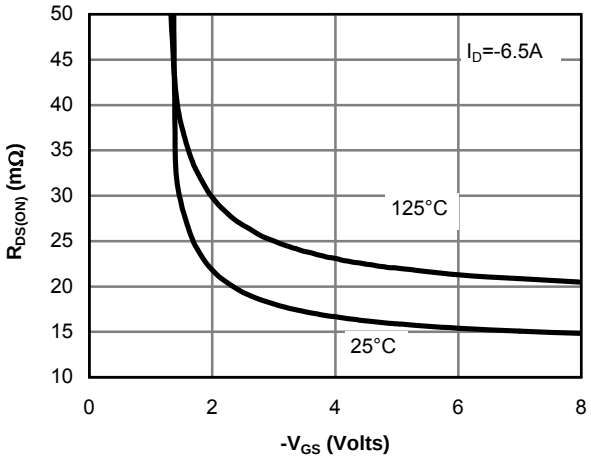


Figure 5: On-Resistance vs. Gate-Source Voltage

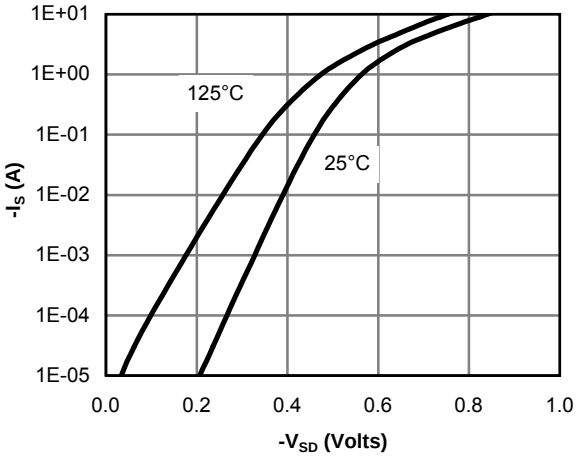


Figure 6: Body-Diode Characteristics

DUAL P-CHANNEL ENHANCEMENT MODE FET

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

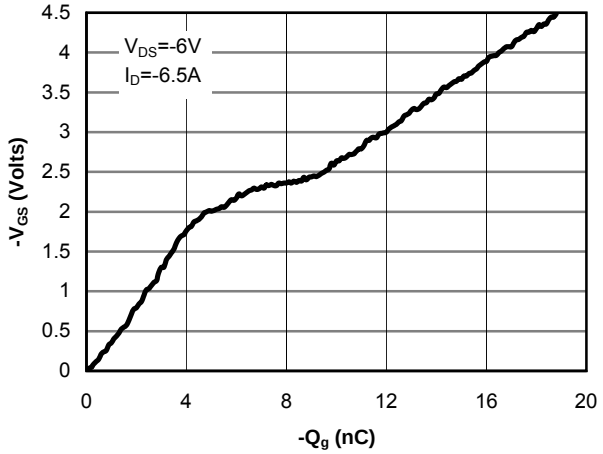


Figure 7: Gate-Charge Characteristics

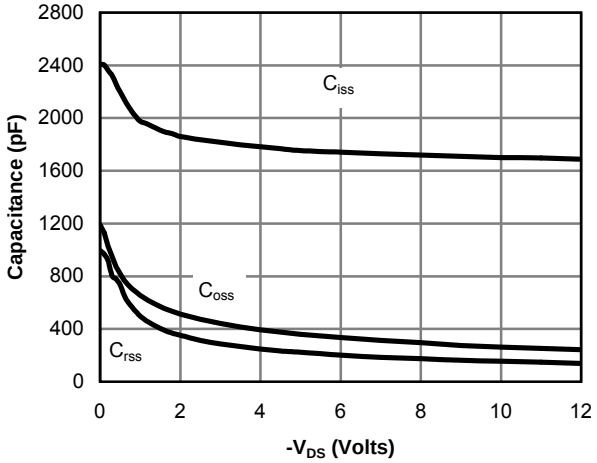


Figure 8: Capacitance Characteristics

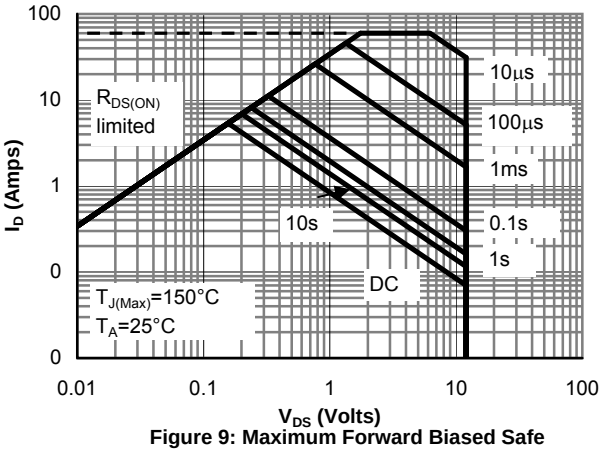


Figure 9: Maximum Forward Biased Safe Operating Area

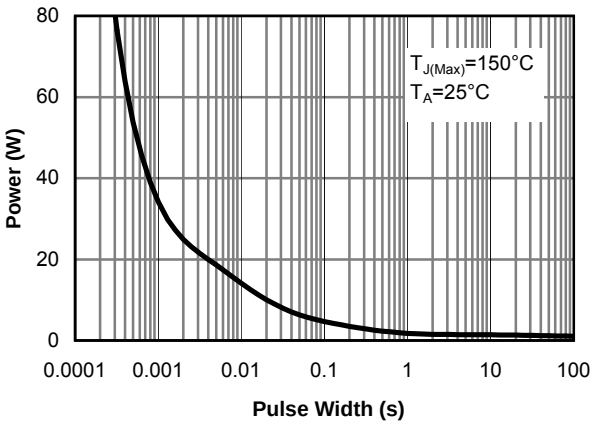


Figure 10: Single Pulse Power Rating Junction-to-Ambient

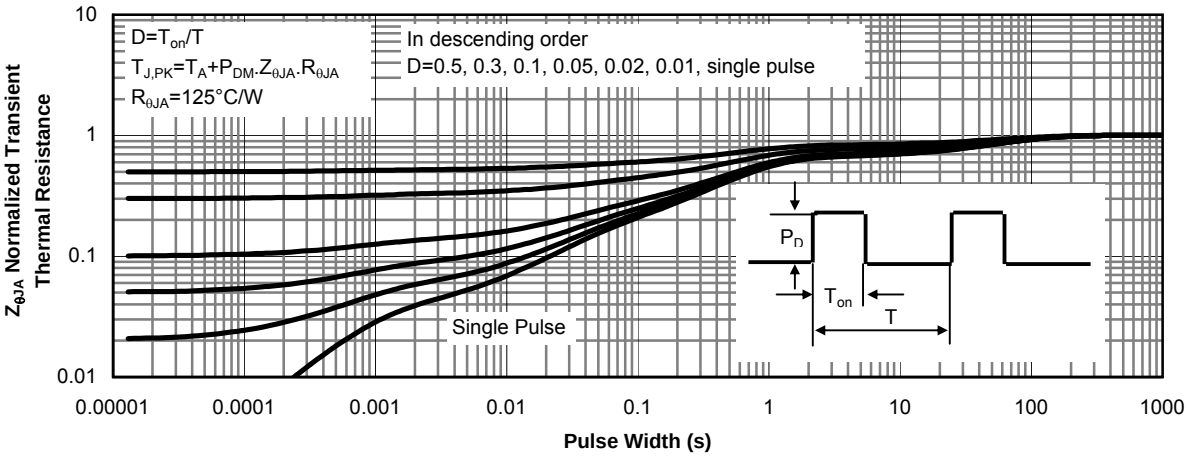
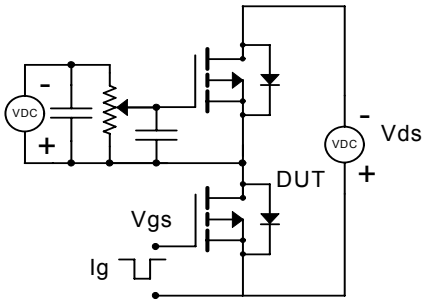
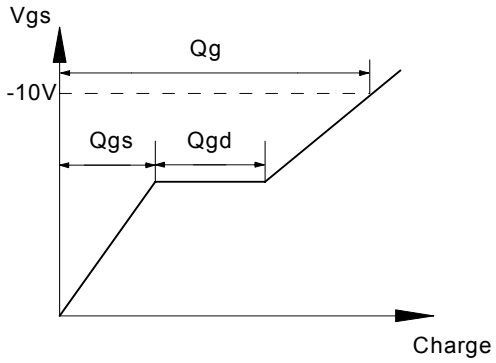


Figure 11: Normalized Maximum Transient Thermal Impedance

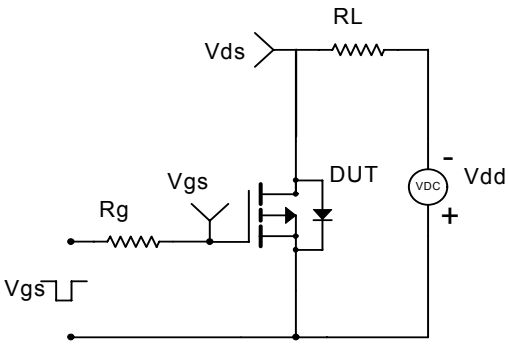
DUAL P-CHANNEL ENHANCEMENT MODE FET

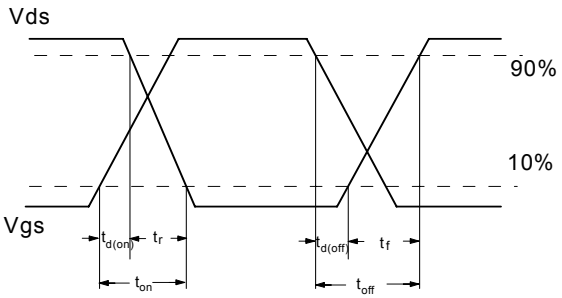
Gate Charge Test Circuit & Waveform



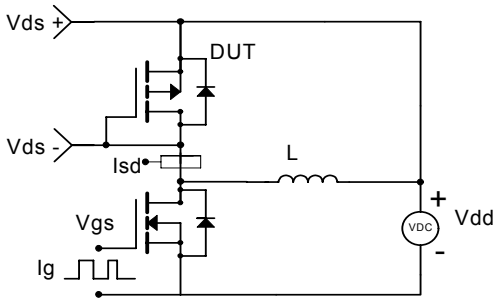


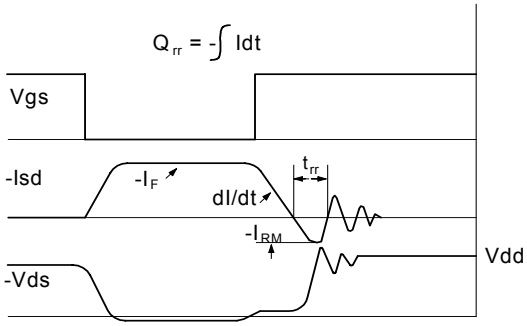
Resistive Switching Test Circuit & Waveforms





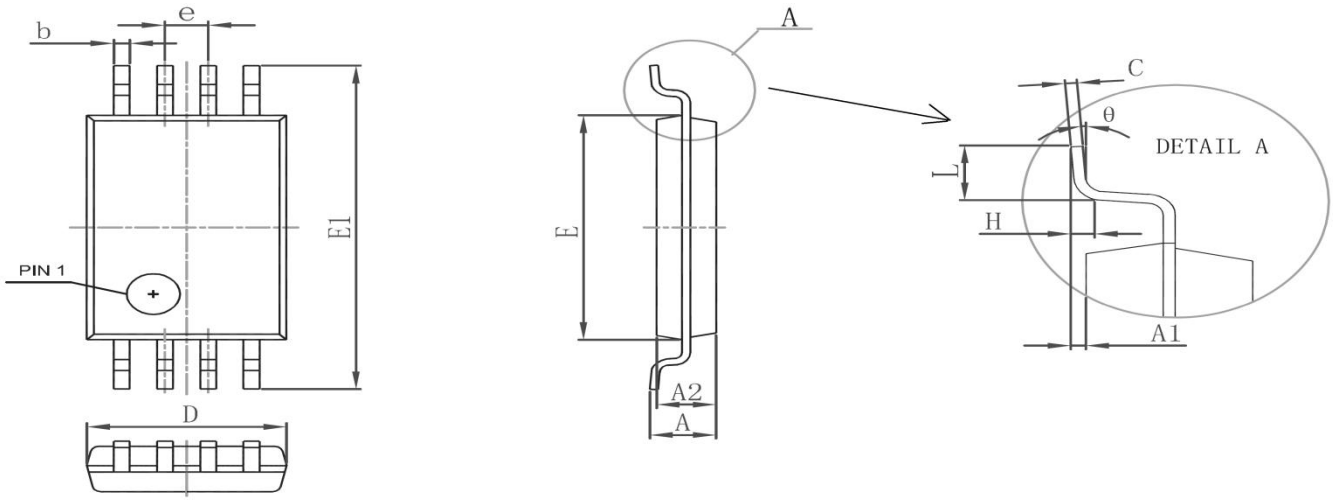
Diode Recovery Test Circuit & Waveforms





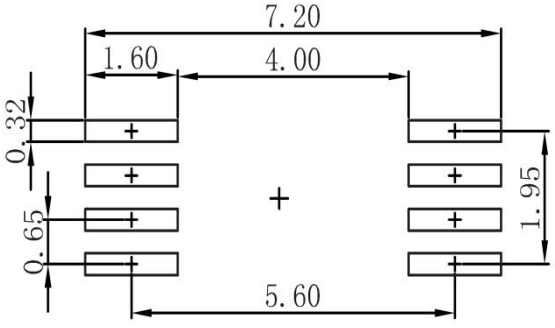
DUAL P-CHANNEL ENHANCEMENT MODE FET

SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

SOP-8 Suggested Pad Layout



Note:

1.Controlling dimension: in millimeters

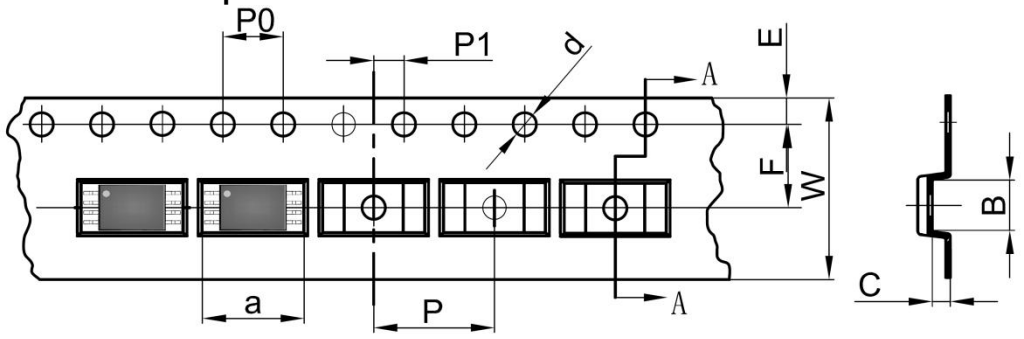
2.General tolerance: ±0.05mm

3.The pad layout is for reference purposes only

DUAL P-CHANNEL ENHANCEMENT MODE FET

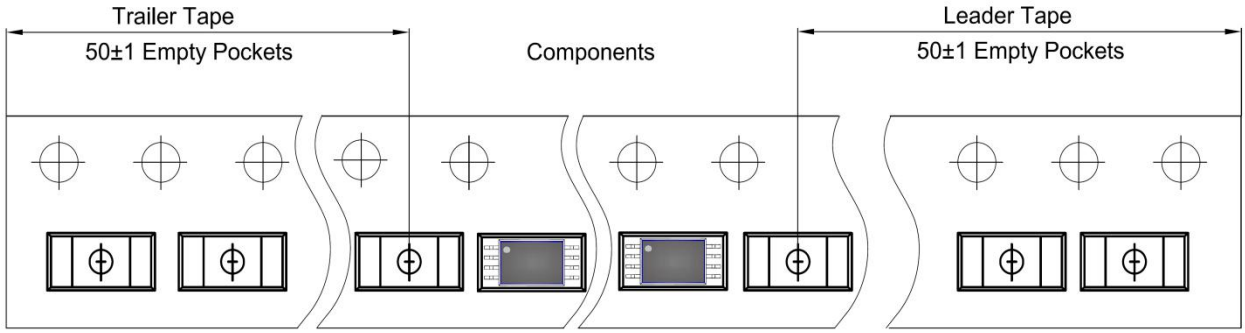
SOP-8 Tape and Reel

SOP-8 Embossed Carrier Tape

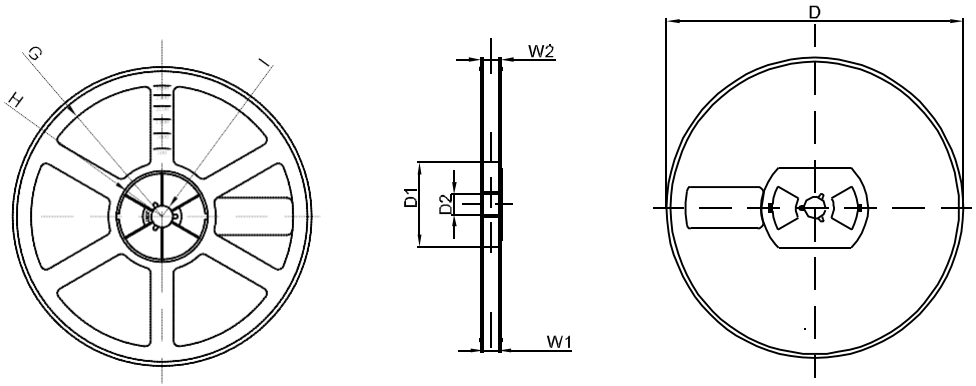


	DIMENSIONS ARE IN MILLIMETER									
TYPE	a	B	C	d	E	F	P0	P	P1	W
SOP-8	6.76	3.30	1.20	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

SOP-8 Tape Leader and Trailer



SOP-8 Reel



	DIMENSIONS ARE IN MILLIMETER							
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13” DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1