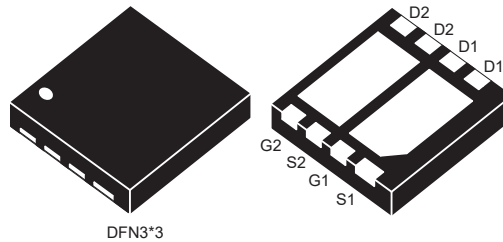
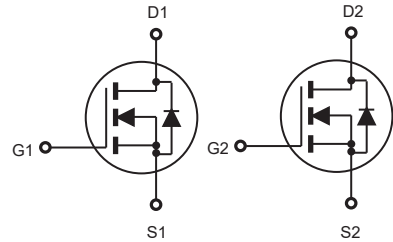


## Dual N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 60V, 21A,  $R_{DS(ON)} = 22m\Omega$  @  $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 30m\Omega$  @  $V_{GS} = 4.5V$ .
- Super High dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

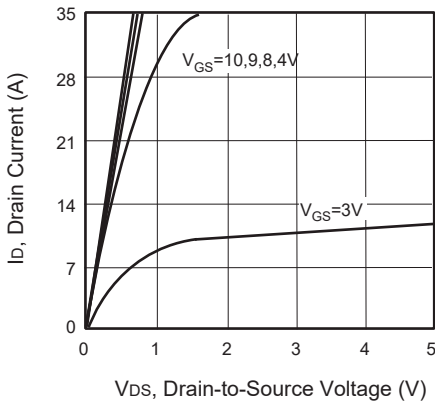
Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D @ R_{\theta Jc}$	21	A
	$I_D @ R_{\theta JA}$	8	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM} @ R_{\theta Jc}$	84	A
	$I_{DM} @ R_{\theta JA}$	32	A
Maximum Power Dissipation	$P_D$	18	W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

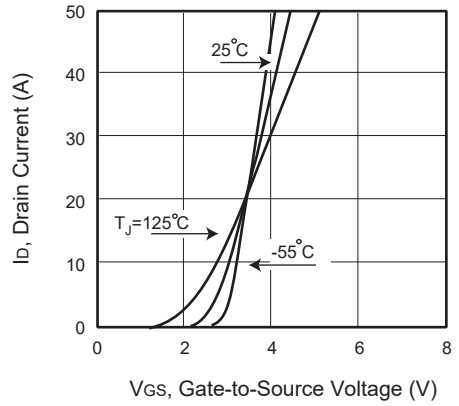
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case <sup>b</sup>	$R_{\theta Jc}$	7	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	50	$^\circ C/W$

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

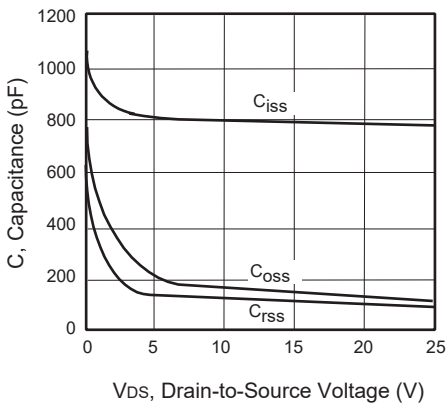
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics <sup>c</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6A$		18	22	$m\Omega$
		$V_{GS} = 4.5V, I_D = 4A$		23	30	$m\Omega$
<b>Dynamic Characteristics <sup>d</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		780		pF
Output Capacitance	$C_{oss}$			115		pF
Reverse Transfer Capacitance	$C_{rss}$			95		pF
<b>Switching Characteristics <sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30V, I_D = 7A,$ $V_{GS} = 10V, R_{GEN} = 4.7\Omega$		15		ns
Turn-On Rise Time	$t_r$			7		ns
Turn-Off Delay Time	$t_{d(off)}$			43		ns
Turn-Off Fall Time	$t_f$			8		ns
Total Gate Charge	$Q_g$	$V_{DS} = 48V, I_D = 7A,$ $V_{GS} = 4.5V$		14		nC
Gate-Source Charge	$Q_{gs}$			2		nC
Gate-Drain Charge	$Q_{gd}$			9		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				14	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 1.5A$			1.2	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . d.Guaranteed by design, not subject to production testing.						



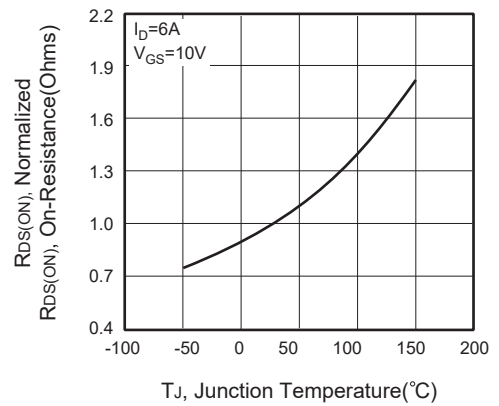
**Figure 1. Output Characteristics**



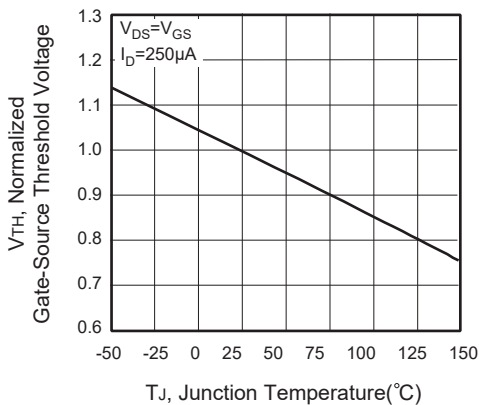
**Figure 2. Transfer Characteristics**



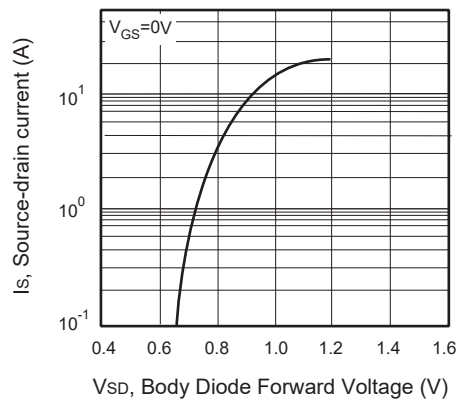
**Figure 3. Capacitance**



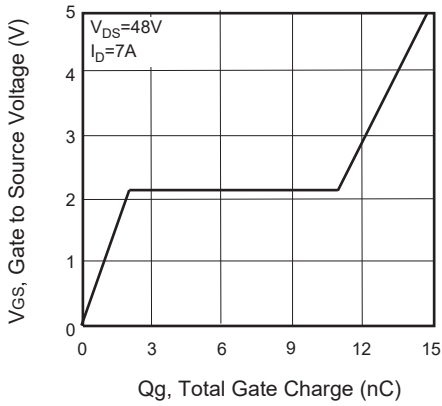
**Figure 4. On-Resistance Variation with Temperature**



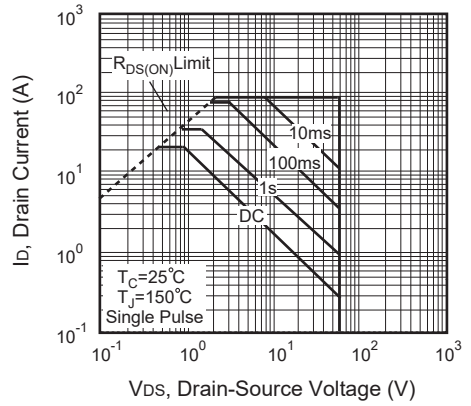
**Figure 5. Gate Threshold Variation with Temperature**



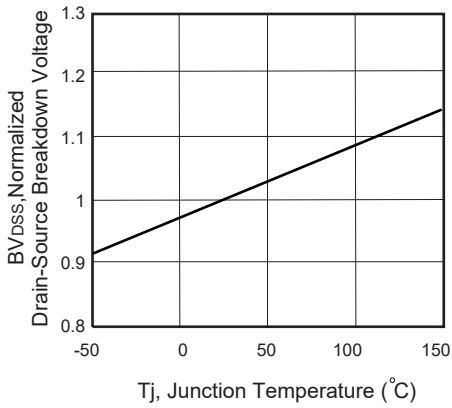
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



**Figure 7. Gate Charge**



**Figure 8. Maximum Safe Operating Area**



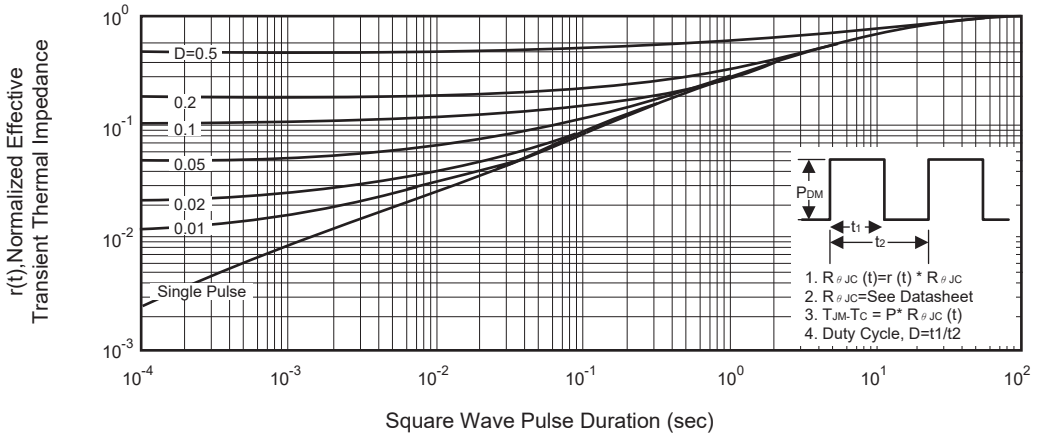
**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



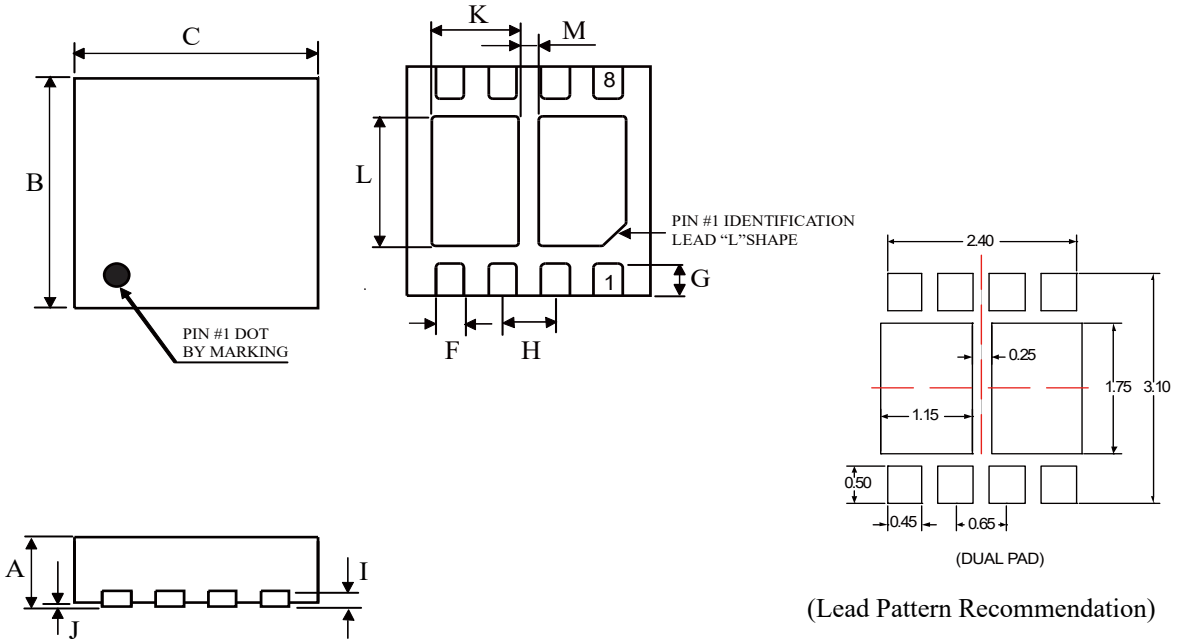
**Figure 11. Switching Waveforms**



**Figure 12. Normalized Thermal Transient Impedance Curve**

## DFN 3X3 產品外觀尺寸圖 (Product Outline Dimension)

### DUAL PAD 尺寸圖



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.85	0.028	0.033
B	2.90	3.10	0.114	0.122
C	2.90	3.10	0.114	0.122
F	0.30	0.40	0.012	0.016
G	0.35	0.48	0.014	0.019
H	0.65(BSC)		0.026(BSC)	
I	0.203(REF)		0.008(REF)	
J	0	0.05	0	0.002
K	1.025	1.125	0.040	0.044
L	1.65	1.75	0.065	0.069
M	0.25		0.01	