

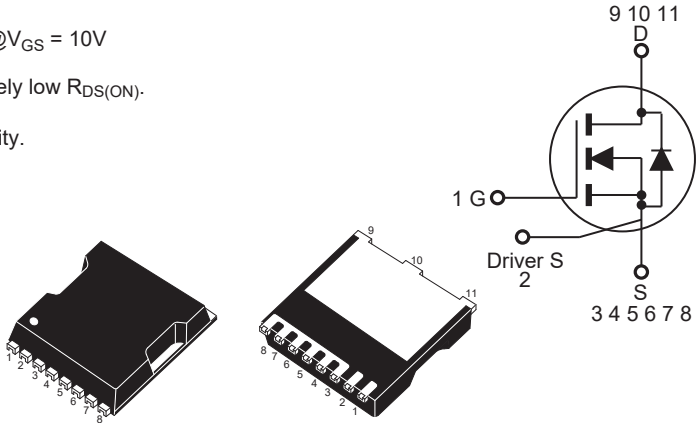
N-Channel Enhancement Mode Field Effect Transistor With Fast Body Diode

FEATURES

- 650V@ $T_{J\max}$, 68A, $R_{DS(ON)} = 37m\Omega$ @ $V_{GS} = 10V$
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Pb-free lead plating ;RoHS compliant.
- Halogen Free.
- Fast reverse recovery time(T_{rr}).
- TOLL package.

Applications

- PV Inverter.
- EV Charging.
- SMPS.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current-Continuous@ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$	I_D	68 43	A A
Drain Current-Pulsed ^a	I_{DM}	272	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	P_D	416 3.3	W W/ $^\circ C$
Single Pulsed Avalanche Energy ^f	E_{AS}	364	mJ
Single Pulsed Avalanche Current ^f	I_{AS}	9	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.3	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	$^\circ C/W$



CEP60N60SF/CEB60N60SF CEF60N60SF

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	600			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600V, V_{GS} = 0V$			5	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	3		5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		31	37	m Ω
Gate input resistance	R_g	f=1MHz, open Drain		1.8		Ω
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 400V, V_{GS} = 0V,$ $f = 250KHz$		3455		pF
Output Capacitance	C_{oss}			110		pF
Reverse Transfer Capacitance	C_{rss}			20		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 16A,$ $V_{GS} = 10V, R_{GEN} = 5.3\Omega$		57		ns
Turn-On Rise Time	t_r			10		ns
Turn-Off Delay Time	$t_{d(off)}$			132		ns
Turn-Off Fall Time	t_f			10		ns
Total Gate Charge	Q_g	$V_{DS} = 400V, I_D = 16A,$ $V_{GS} = 10V$		130		nC
Gate-Source Charge	Q_{gs}			33		nC
Gate-Drain Charge	Q_{gd}			54		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				60	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 20A$			1.5	V
Reverse Recovery Time	T_{rr}	$I_F = 20A, di/dt = 100A/\mu s$		191		ns
Reverse Recovery Charge	Q_{rr}			1.56		μC
Peak Reverse Recovery Current	I_{rr}			15		A
Reverse diode dv/dt ruggedness, $V_{DS} = 0 \dots 480V, I_{SD} \leq I_D$	dv/dt	$I_{DR} = 10A, V_{GS} = 0V,$ $V_{DD} = 400V$		100		V/ns
MOSFET dv/dt ruggedness, $V_{DS} = 0 \dots 480V$				100		V/ns
Notes :						
a. Repetitive Rating : Pulse width limited by maximum junction temperature .						
b. Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.						
c. Guaranteed by design, not subject to production testing.						
d. Limited only by maximum temperature allowed .						
e. Pulse width limited by safe operating area .						
f. Full package $I_{S(max)} = 31A$.						
g. L = 9mH, $I_{AS} = 9A, V_{DD} = 60V, R_G = 25\Omega$, Starting $T_J = 25^\circ C$.						

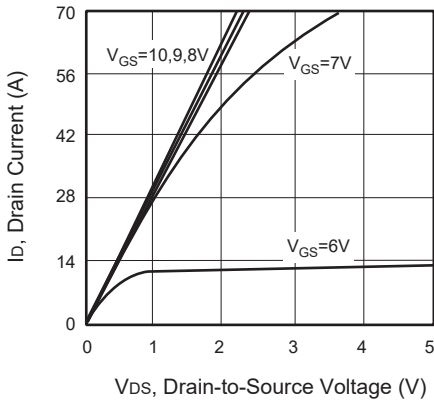


Figure 1. Output Characteristics

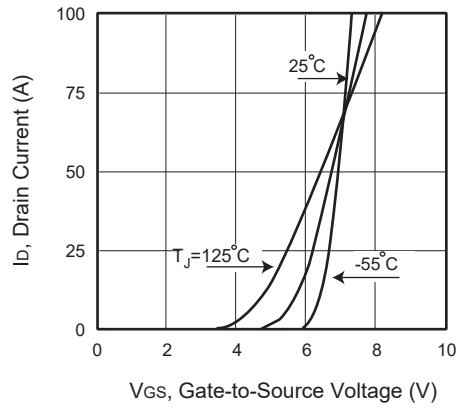


Figure 2. Transfer Characteristics

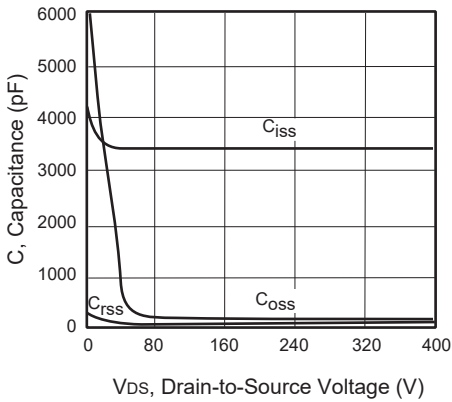


Figure 3. Capacitance

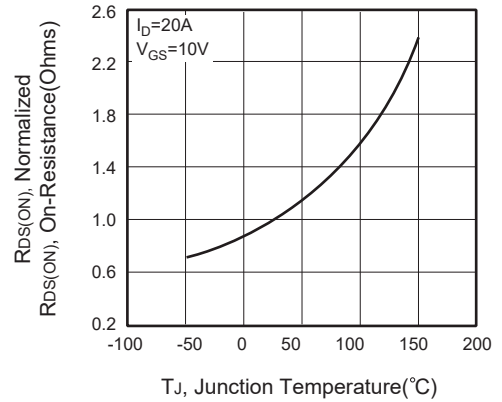


Figure 4. On-Resistance Variation with Temperature

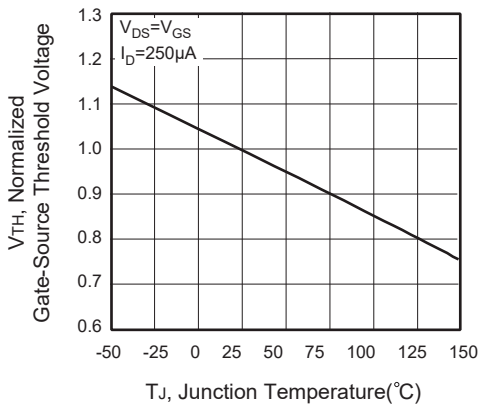


Figure 5. Gate Threshold Variation with Temperature

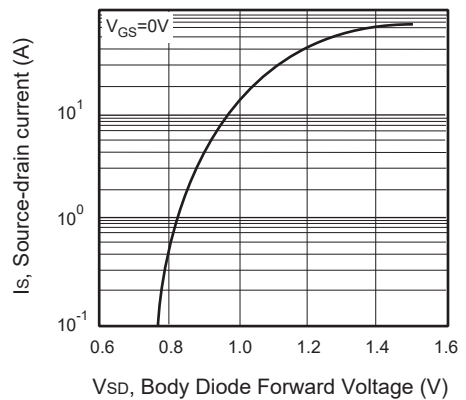


Figure 6. Body Diode Forward Voltage Variation with Source Current

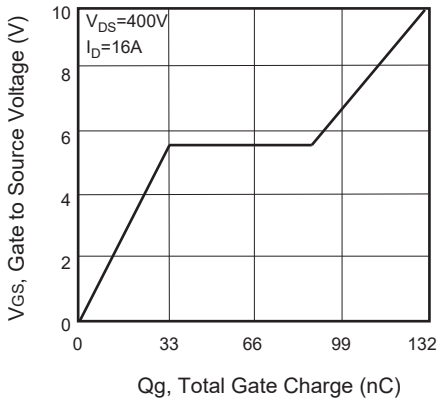


Figure 7. Gate Charge

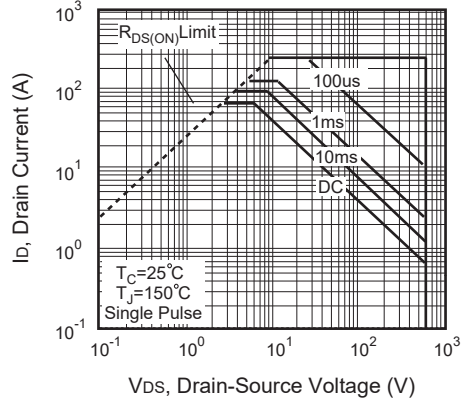


Figure 8. Maximum Safe Operating Area

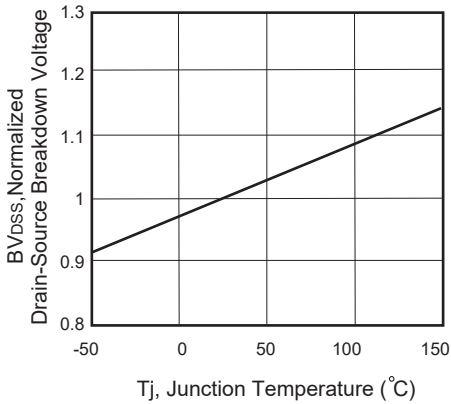


Figure 9. Breakdown Voltage Variation VS Temperature

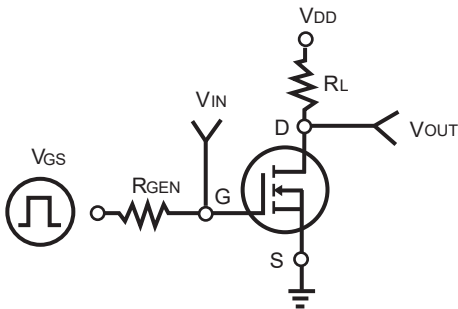


Figure 10. Switching Test Circuit

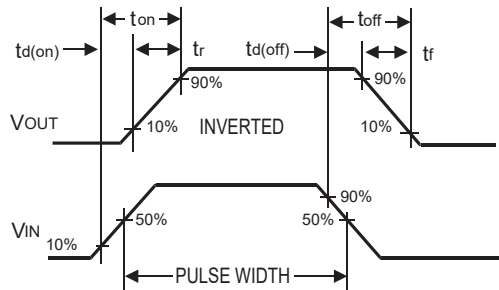


Figure 11. Switching Waveforms

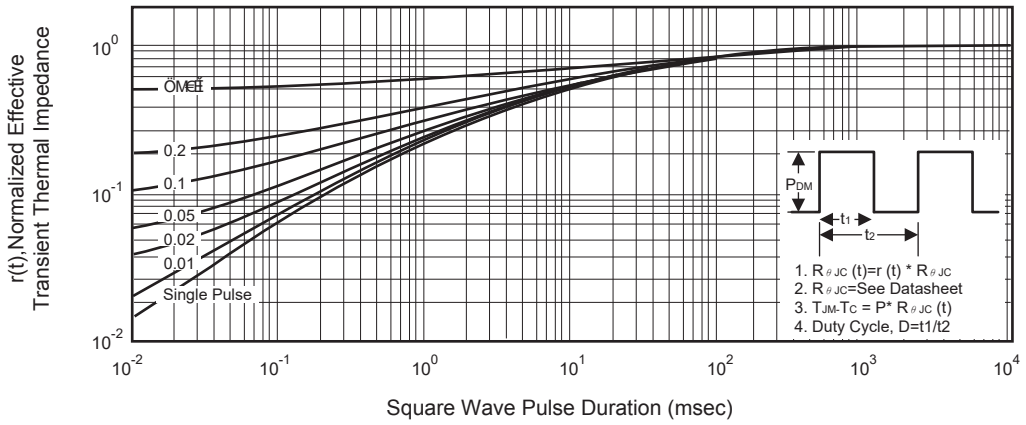
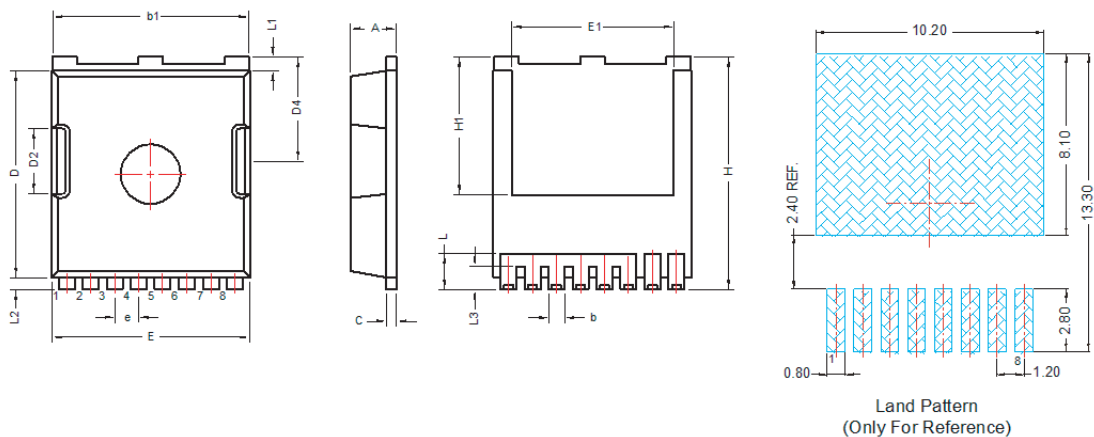


Figure 12. Normalized Thermal Transient Impedance Curve

TOLL產品外觀尺寸圖(Product Outline Dimension)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.150	2.450	0.085	0.096
b	0.700	0.900	0.028	0.035
b1	9.650	9.950	0.380	0.392
c	0.400	0.600	0.016	0.024
D	10.180	10.580	0.401	0.417
D2	3.150	3.450	0.124	0.136
D4	4.400	4.700	0.173	0.185
E	9.700	10.100	0.382	0.398
E1	7.950	8.250	0.313	0.325
e	1.20BSC		0.047BSC	
H	11.480	11.880	0.452	0.468
H1	6.800	7.100	0.268	0.280
L	1.500	2.100	0.059	0.083
L1	0.500	0.900	0.020	0.035
L2	0.500	0.720	0.020	0.028
L3	1.000	1.300	0.039	0.051