



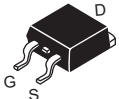
# CEP20N65SF/CEB20N65SF CEF20N65SF

## N-Channel Enhancement Mode Field Effect Transistor

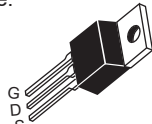
### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP20N65SF	650V	0.19Ω	20A	10V
CEB20N65SF	650V	0.19Ω	20A	10V
CEF20N65SF	650V	0.19Ω	20A <sup>d</sup>	10V

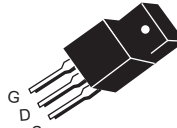
- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- RoHS compliant.
- Fast reverse recovery time.
- Drive circuits can be simple.



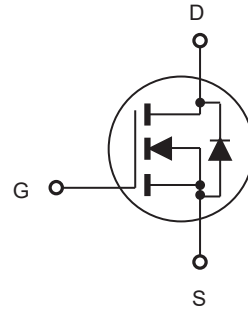
CEB SERIES  
TO-263(DD-PAK)



CEP SERIES  
TO-220



CEF SERIES  
TO-220F



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	650		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current-Continuous @ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 100°C	I <sub>D</sub>	20	20 <sup>d</sup>	A
		12	12 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	80	80 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	205	35	W
		1.64	0.28	W/°C
Single Pulsed Avalanche Energy <sup>h</sup>	E <sub>AS</sub>	486		mJ
Single Pulsed Avalanche Current <sup>h</sup>	I <sub>AS</sub>	4.5		A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	0.61	3.6	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



# CEP20N65SF/CEB20N65SF CEF20N65SF

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650V, V_{GS} = 0V$			5	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	3		5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		0.162	0.19	$\Omega$
Gate input resistance	$R_g$	f=1MHz, open Drain		4.3		$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 150V, V_{GS}=0V,$ $f = 1.0\text{ MHz}$		1630		pF
Output Capacitance	$C_{oss}$			85		pF
Reverse Transfer Capacitance	$C_{rss}$			10		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520V, I_D = 10A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		34		ns
Turn-On Rise Time	$t_r$			9		ns
Turn-Off Delay Time	$t_{d(off)}$			66		ns
Turn-Off Fall Time	$t_f$			7		ns
Total Gate Charge	$Q_g$	$V_{DS} = 520V, I_D = 10A,$ $V_{GS} = 10V$		43		nC
Gate-Source Charge	$Q_{gs}$			10		nC
Gate-Drain Charge	$Q_{gd}$			18		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^f$				20	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 20A^g$			1.5	V
Reverse Recovery Time	$T_{rr}$	$I_D = 20A, di/dt = 100A/\mu s$		92		ns
Reverse Recovery Charge	$Q_{rr}$			0.34		$\mu C$
Peak Reverse Recovery Current	$I_{rr}$			6.9		A
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 8A$ . g.Full package $V_{SD}$ test condition $I_S = 8A$ . h.L = 48mH, $I_{AS} = 4.5A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25^\circ C$ .						



# CEP20N65SF/CEB20N65SF CEF20N65SF

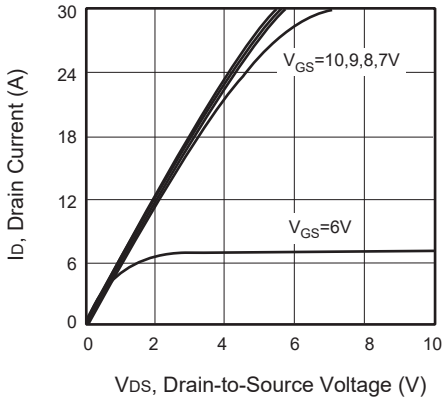


Figure 1. Output Characteristics

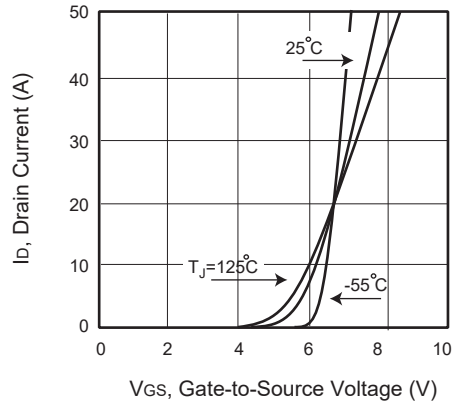


Figure 2. Transfer Characteristics

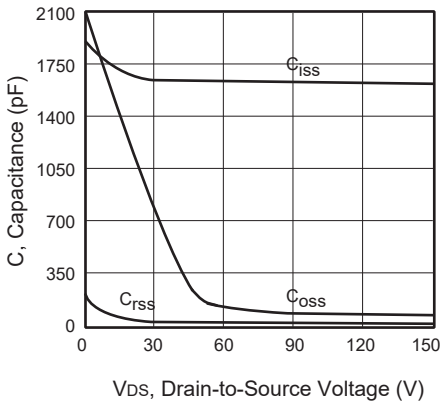


Figure 3. Capacitance

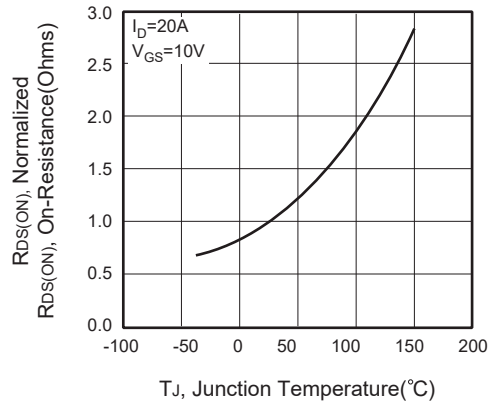


Figure 4. On-Resistance Variation with Temperature

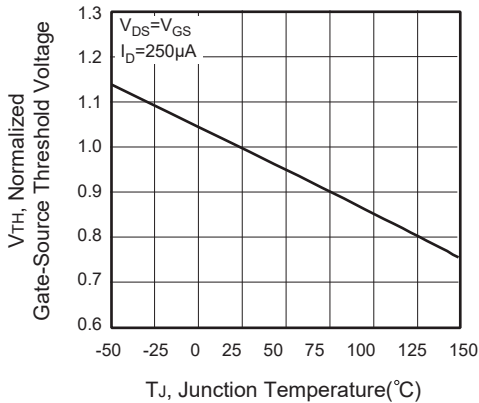


Figure 5. Gate Threshold Variation with Temperature

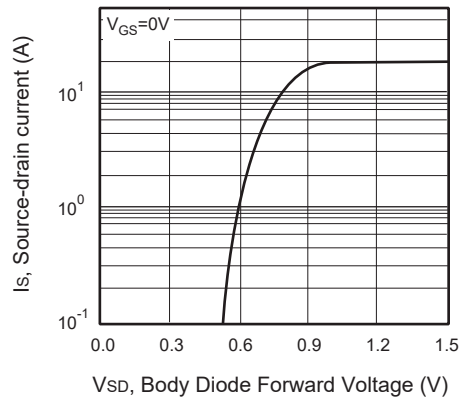


Figure 6. Body Diode Forward Voltage Variation with Source Current



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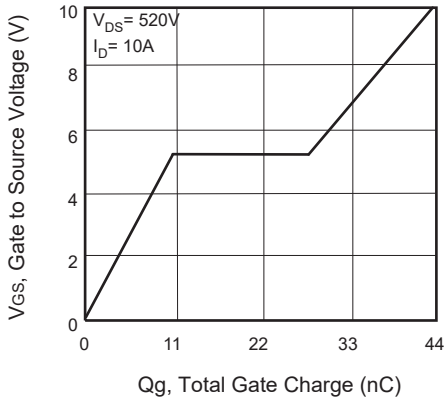


Figure 7. Gate Charge

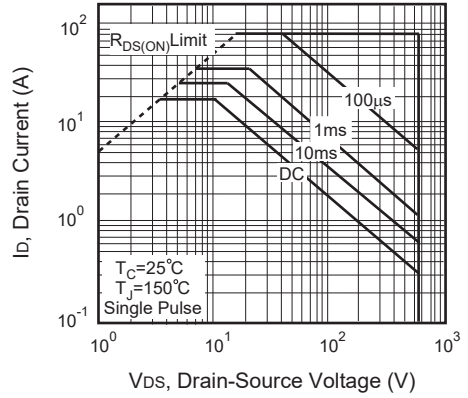


Figure 8. Maximum Safe Operating Area

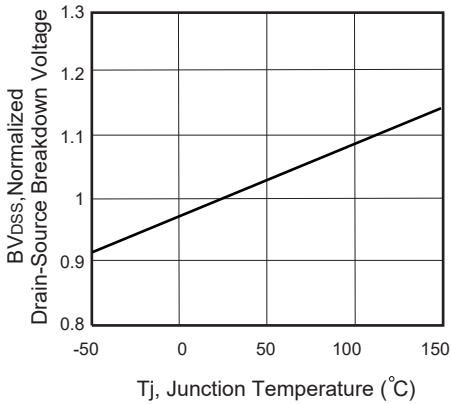


Figure 9. Breakdown Voltage Variation VS Temperature

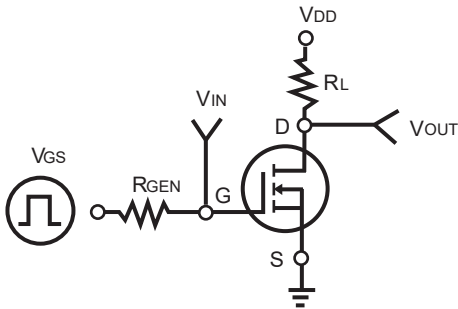


Figure 10. Switching Test Circuit

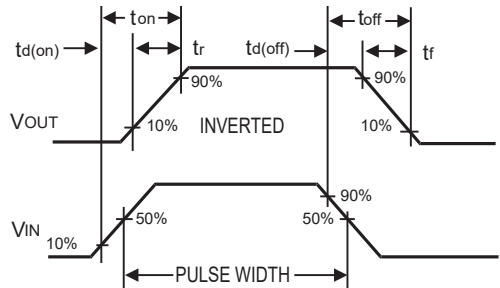


Figure 11. Switching Waveforms



# CEP20N65SF/CEB20N65SF CEF20N65SF

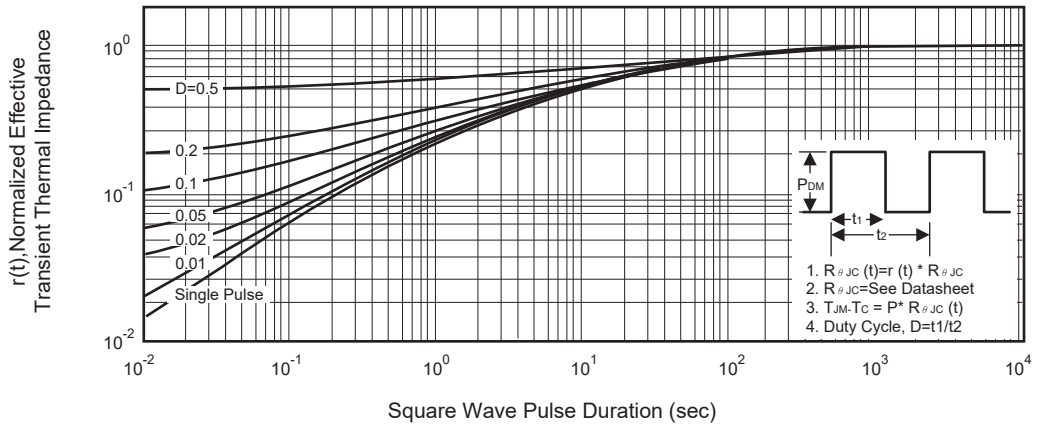


Figure 12. Normalized Thermal Transient Impedance Curve