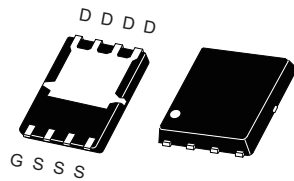


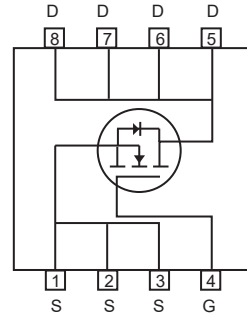
N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 150V, 57A, $R_{DS(ON)} = 16\text{ m}\Omega$ @ $V_{GS} = 10\text{V}$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- RoHS compliant.
- Surface mount Package.



P-PAK 5X6



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Limit | Units |
|--|--------------------------|------------|------------------|
| Drain-Source Voltage | V_{DS} | 150 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Drain Current-Continuous | $I_D @ R_{\theta JC}$ | 57 | A |
| Drain Current-Continuous | $I_D @ R_{\theta JA}$ | 15 | A |
| Drain Current-Pulsed ^a | $I_{DM} @ R_{\theta JC}$ | 228 | A |
| Drain Current-Pulsed ^a | $I_{DM} @ R_{\theta JA}$ | 60 | A |
| Maximum Power Dissipation | P_D | 89 | W |
| Single Pulsed Avalanche Energy ^e | E_{AS} | 31.25 | mJ |
| Single Pulsed Avalanche Current ^e | I_{AS} | 25 | A |
| Operating and Store Temperature Range | T_J, T_{stg} | -55 to 150 | $^\circ\text{C}$ |

Thermal Characteristics

| Parameter | Symbol | Limit | Units |
|--|-----------------|-------|--------------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 1.4 | $^\circ\text{C/W}$ |
| Thermal Resistance, Junction-to-Ambient ^b | $R_{\theta JA}$ | 20 | $^\circ\text{C/W}$ |

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|--------------|--|-----|------|------|-----------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS} = 0V, I_D = 250\mu A$ | 150 | | | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 150V, V_{GS} = 0V$ | | | 1 | μA |
| Gate Body Leakage Current, Forward | I_{GSSF} | $V_{GS} = 20V, V_{DS} = 0V$ | | | 100 | nA |
| Gate Body Leakage Current, Reverse | I_{GSSR} | $V_{GS} = -20V, V_{DS} = 0V$ | | | -100 | nA |
| On Characteristics ^c | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS} = V_{DS}, I_D = 250\mu A$ | 2 | | 4 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS} = 10V, I_D = 20A$ | | 13 | 16 | $m\Omega$ |
| Dynamic Characteristics ^d | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 75V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$ | | 1920 | | pF |
| Output Capacitance | C_{oss} | | | 225 | | pF |
| Reverse Transfer Capacitance | C_{rss} | | | 15 | | pF |
| Switching Characteristics ^d | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 75V, I_D = 20A,$ $V_{GS} = 10V, R_{GEN} = 10\Omega$ | | 25 | | ns |
| Turn-On Rise Time | t_r | | | 6 | | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 38 | | ns |
| Turn-Off Fall Time | t_f | | | 7 | | ns |
| Total Gate Charge | Q_g | $V_{DS} = 75V, I_D = 20A,$ $V_{GS} = 10V$ | | 30 | | nC |
| Gate-Source Charge | Q_{gs} | | | 9 | | nC |
| Gate-Drain Charge | Q_{gd} | | | 6 | | nC |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| Drain-Source Diode Forward Current ^b | I_S | | | | 57 | A |
| Pulsed Source Current | I_{SM} | | | | 228 | A |
| Drain-Source Diode Forward Voltage ^c | V_{SD} | $V_{GS} = 0V, I_S = 20A$ | | | 1.2 | V |
| Reverse Recovery Time | T_{rr} | $I_F = 20A, di/dt = 100A/\mu s$ | | 64 | | ns |
| Reverse Recovery Charge | Q_{rr} | | | 120 | | nC |
| Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec}$. c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing. e.L = 0.1mH, $I_{AS} = 25A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$. | | | | | | |

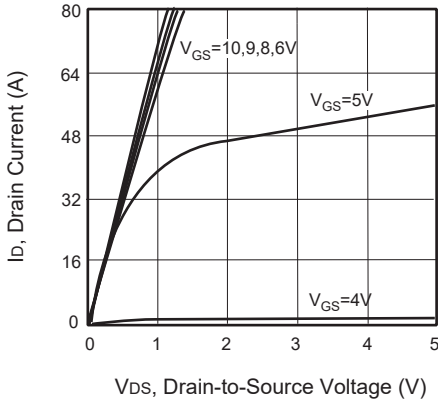


Figure 1. Output Characteristics

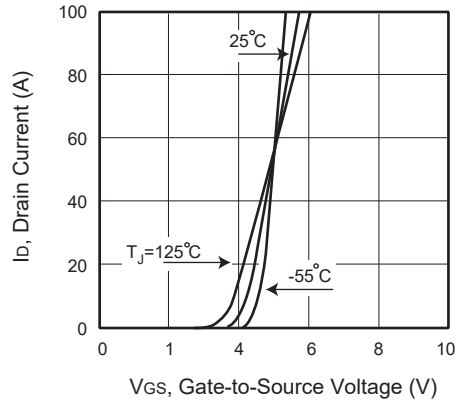


Figure 2. Transfer Characteristics

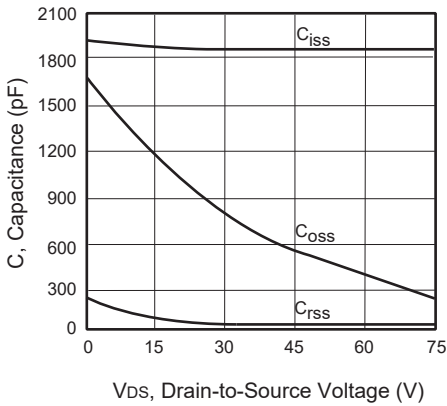


Figure 3. Capacitance

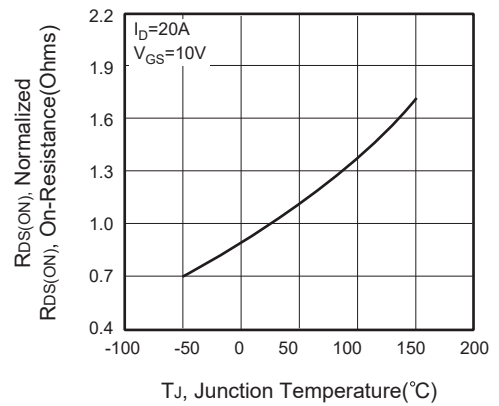


Figure 4. On-Resistance Variation with Temperature

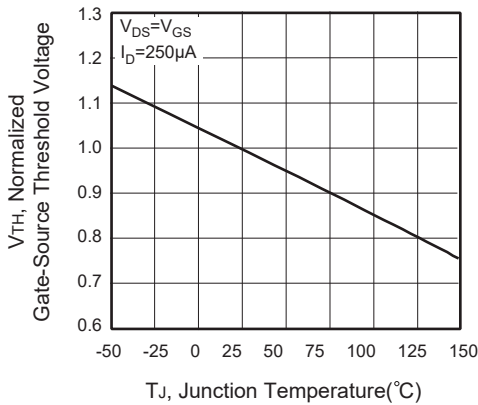


Figure 5. Gate Threshold Variation with Temperature

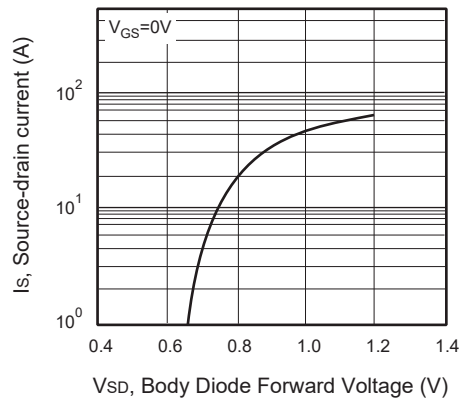


Figure 6. Body Diode Forward Voltage Variation with Source Current

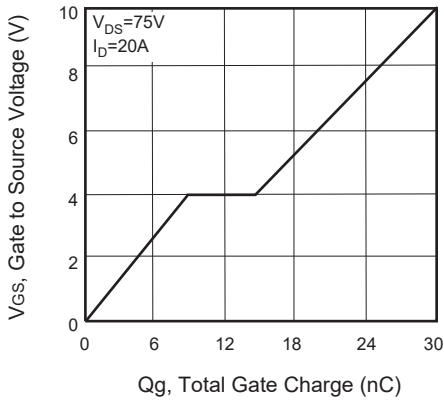


Figure 7. Gate Charge

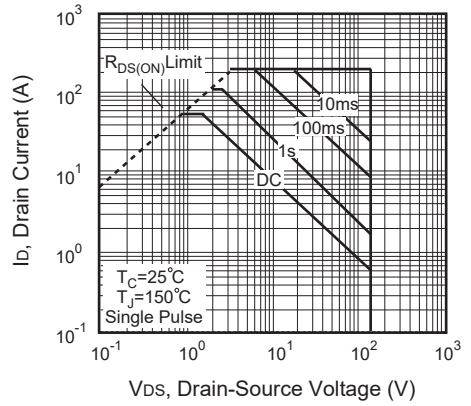


Figure 8. Maximum Safe Operating Area

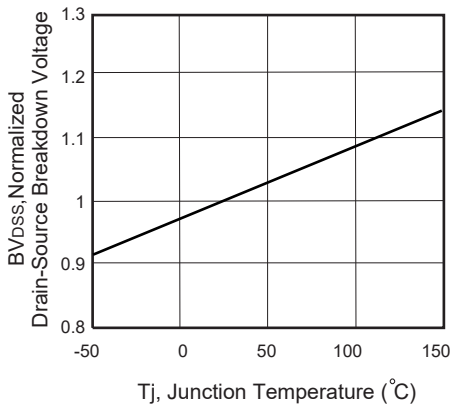


Figure 9. Breakdown Voltage Variation VS Temperature

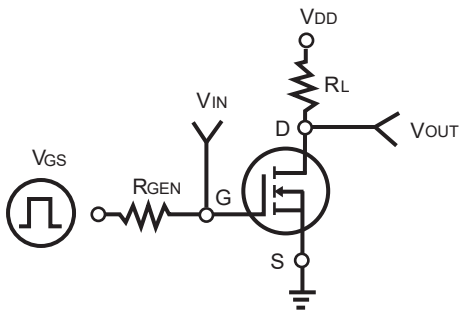


Figure 10. Switching Test Circuit

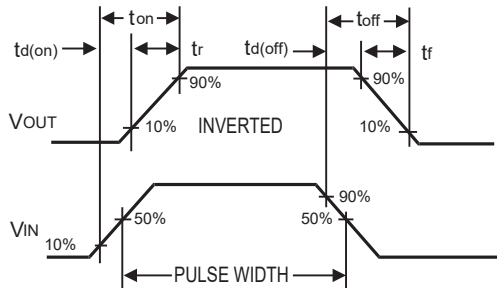


Figure 11. Switching Waveforms

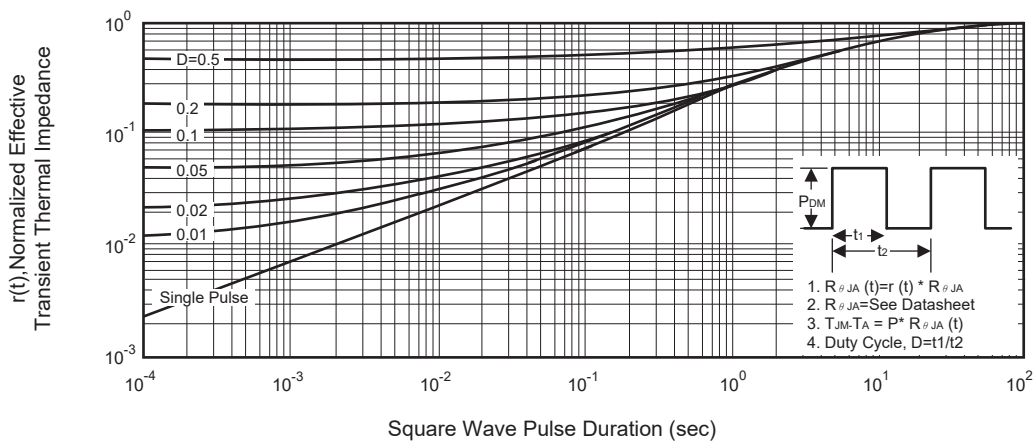
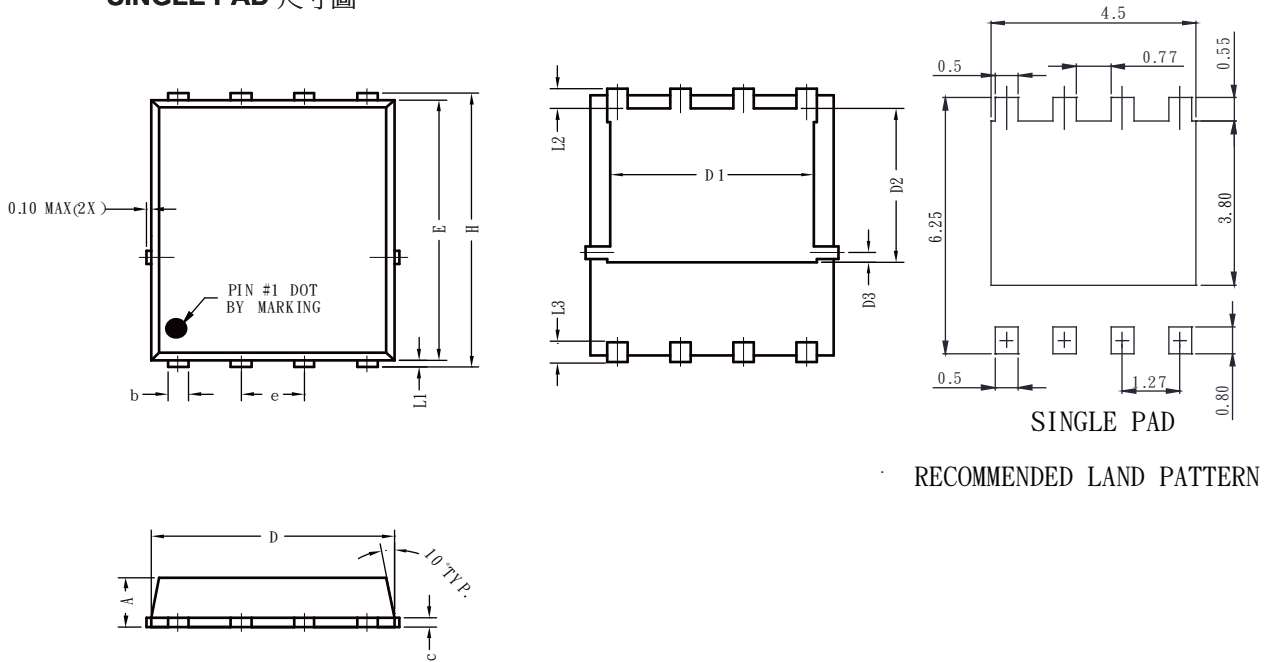


Figure 12. Normalized Thermal Transient Impedance Curve

P-PAK5X6 產品外觀尺寸圖 (Product Outline Dimension)

SINGLE PAD 尺寸圖



RECOMMENDED LAND PATTERN

| SYMBOLS | MILLIMETERS | | INCHES | |
|---------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.800 | 1.170 | 0.031 | 0.046 |
| b | 0.340 | 0.490 | 0.013 | 0.019 |
| c | 0.20 | 0.34 | 0.008 | 0.013 |
| D | 4.800 | 5.100 | 0.009 | 0.011 |
| D1 | 3.800 | 4.200 | 0.150 | 0.165 |
| D2 | 3.180 | 3.78 | 0.125 | 0.149 |
| D3 | 0.150 | 0.360 | 0.006 | 0.142 |
| E | 5.650 | 5.900 | 0.222 | 0.232 |
| e | 1.270 TYP | | 0.050 TYP | |
| H | 5.900 | 6.150 | 0.232 | 0.242 |
| L1 | 0.050 | 0.250 | 0.002 | 0.010 |
| L2 | 0.380 | 0.620 | 0.015 | 0.024 |
| L3 | 0.380 | 0.75 | 0.015 | 0.030 |