PD - 94300C

International
IOR Rectifier

SMPS MOSFET

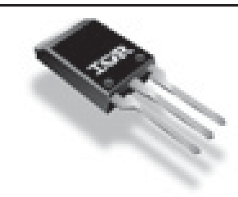
IRFBA90N20D

HEXFET® Power MOSFET

Applications
- High frequency DC-DC converters

V_{DSS}	$R_{DS(on)}$ max	I_D
200V	**0.023Ω**	**98A⑥**

Benefits
- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Super-220™

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	98⑥	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	71⑥	A
I_{DM}	Pulsed Drain Current ①	390	
P_D @T_C = 25°C	Power Dissipation	650	W
	Linear Derating Factor	4.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	6.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Recommended Clip Force	20	N

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.23	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	–––	°C/W
$R_{\theta JA}$	Junction-to-Ambient	–––	58	

Notes ① through ⑥ are on page 8

1/20/04

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.22	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.023	Ω	V_{GS} = 10V, I_D = 59A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	–––	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25	µA	V_{DS} = 200V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -30V

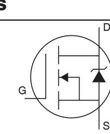
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	41	–––	–––	S	V_{DS} = 50V, I_D = 59A
Q_g	Total Gate Charge	–––	160	240	nC	I_D = 59A
Q_{gs}	Gate-to-Source Charge	–––	45	67		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	75	110		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	–––	23	–––	ns	V_{DD} = 100V
t_r	Rise Time	–––	160	–––		I_D = 59A
$t_{d(off)}$	Turn-Off Delay Time	–––	39	–––		R_G = 1.2Ω
t_f	Fall Time	–––	77	–––		V_{GS} = 10V ④
C_{iss}	Input Capacitance	–––	6080	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	1040	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	150	–––		ƒ = 1.0MHz
C_{oss}	Output Capacitance	–––	7500	–––		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	–––	410	–––		V_{GS} = 0V, V_{DS} = 160V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	790	–––		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	960	mJ
I_{AR}	Avalanche Current①	–––	59	A
E_{AR}	Repetitive Avalanche Energy①	–––	65	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	98	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	390		
V_{SD}	Diode Forward Voltage	–––	–––	1.5	V	T_J = 25°C, I_S = 59A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	220	340	nS	T_J = 25°C, I_F = 59A
Q_{rr}	Reverse RecoveryCharge	–––	1.9	2.8	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

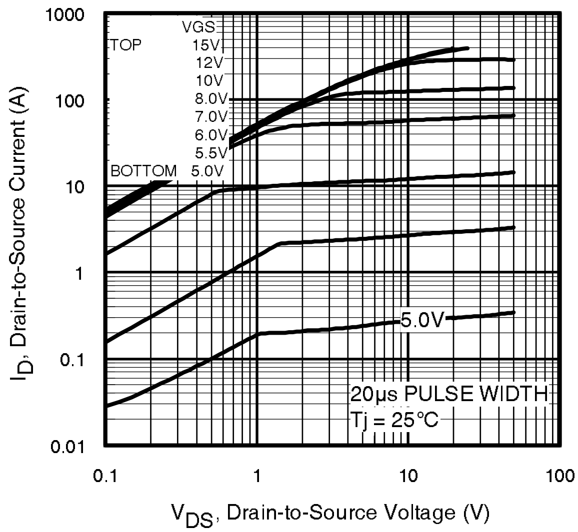


Fig 1. Typical Output Characteristics

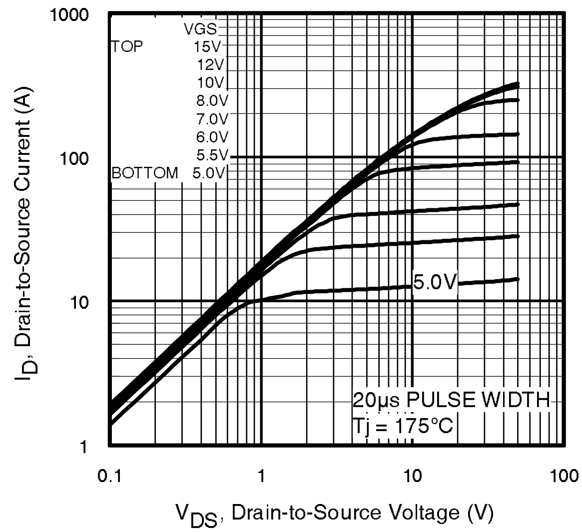


Fig 2. Typical Output Characteristics

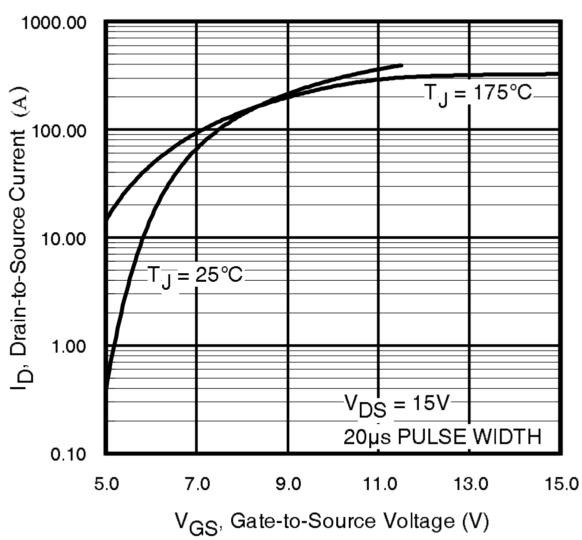


Fig 3. Typical Transfer Characteristics

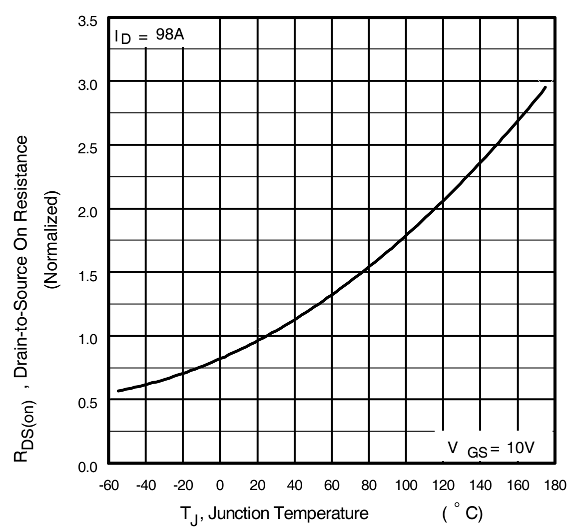


Fig 4. Normalized On-Resistance
Vs. Temperature

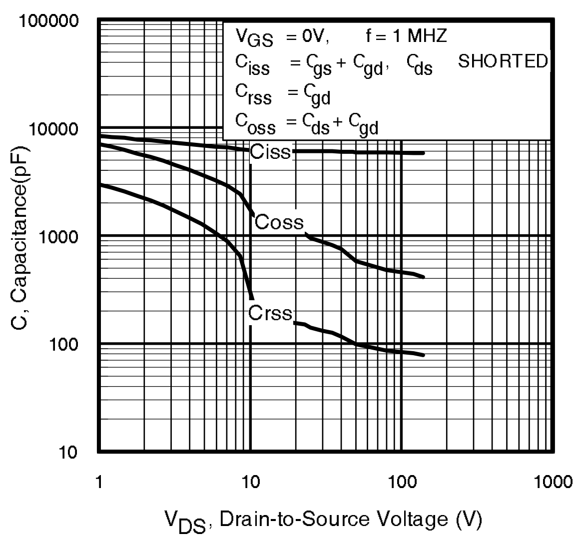


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

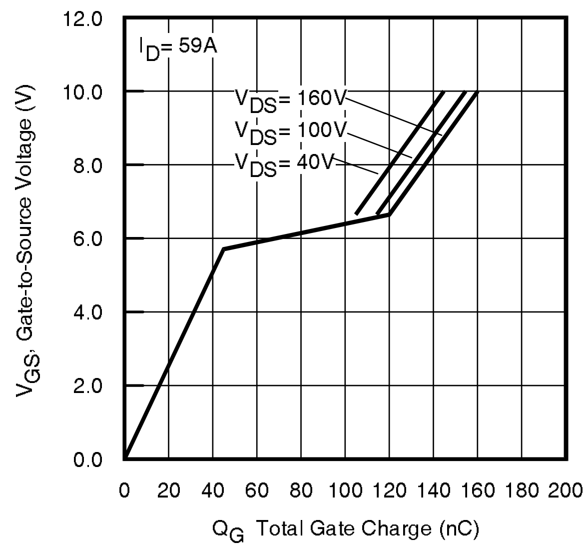


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

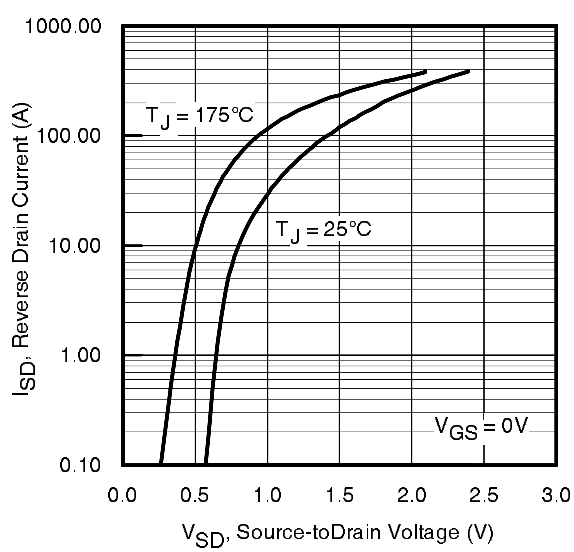


Fig 7. Typical Source-Drain Diode Forward Voltage

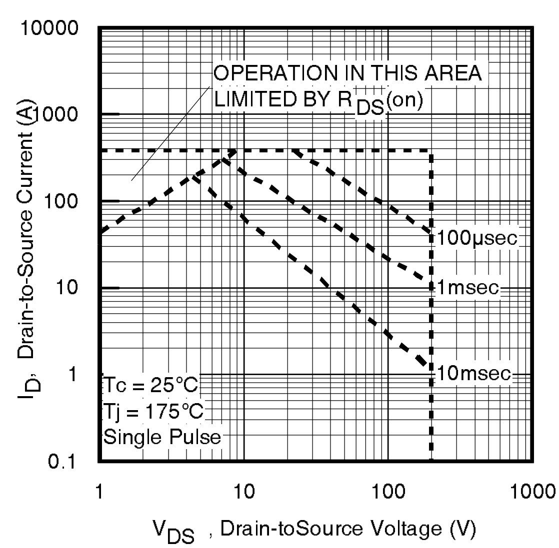


Fig 8. Maximum Safe Operating Area

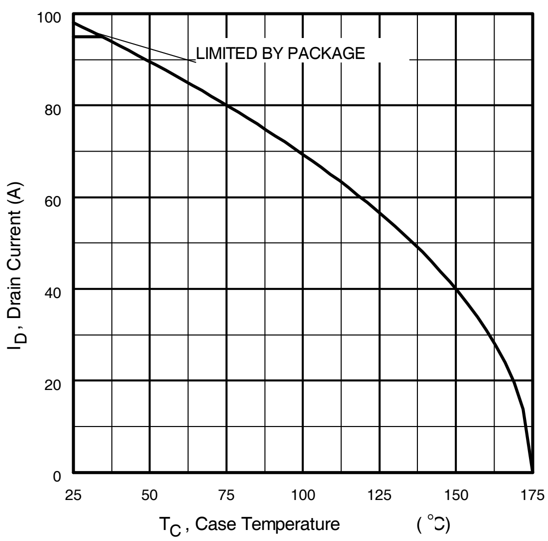


Fig 9. Maximum Drain Current Vs. Case Temperature

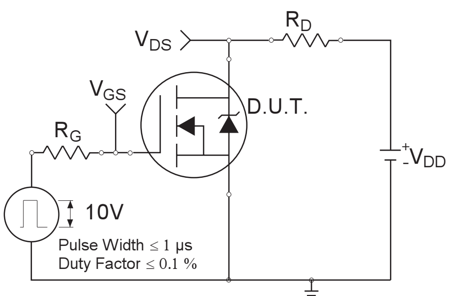


Fig 10a. Switching Time Test Circuit

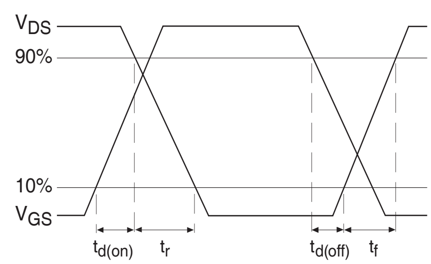


Fig 10b. Switching Time Waveforms

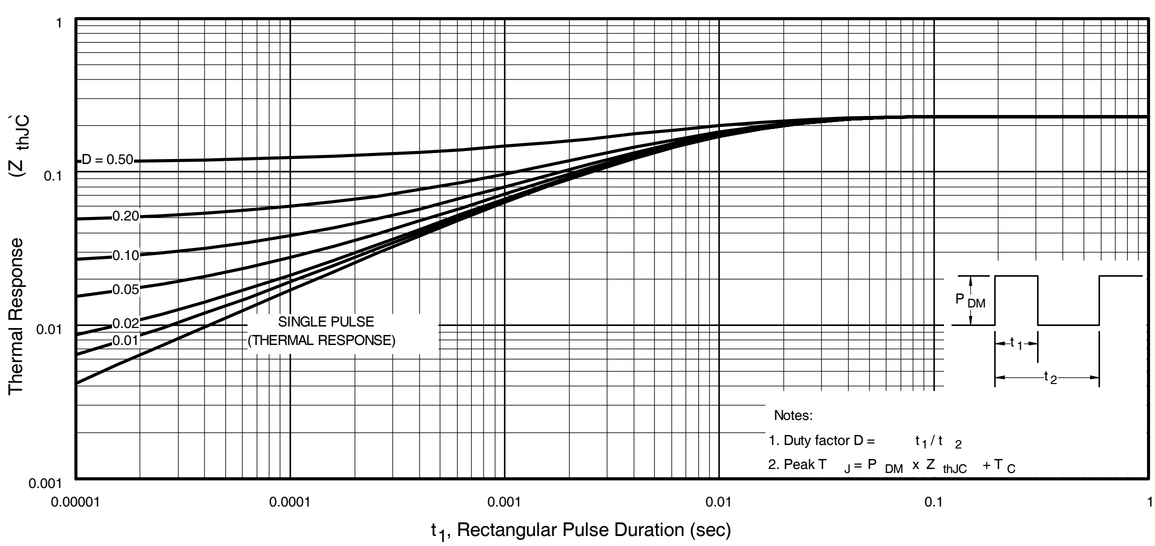


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

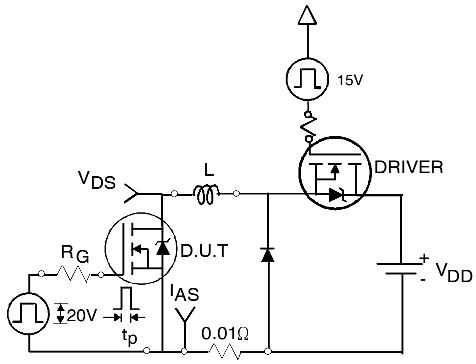


Fig 12a. Unclamped Inductive Test Circuit

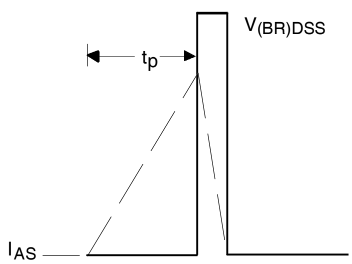


Fig 12b. Unclamped Inductive Waveforms

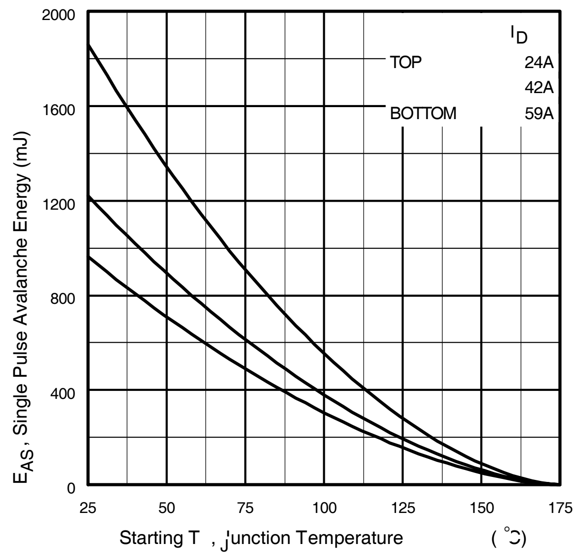


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

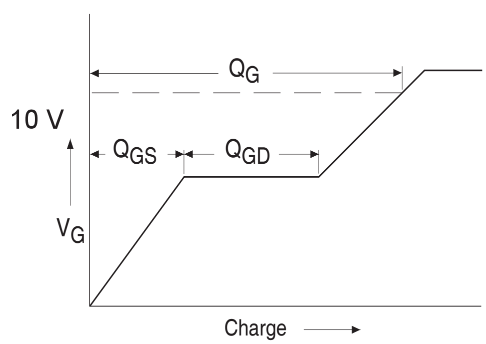


Fig 13a. Basic Gate Charge Waveform

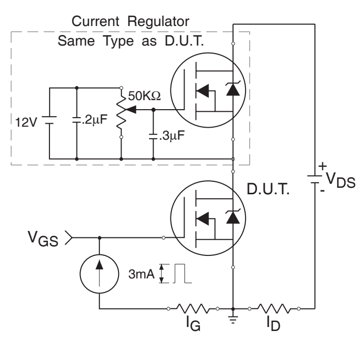
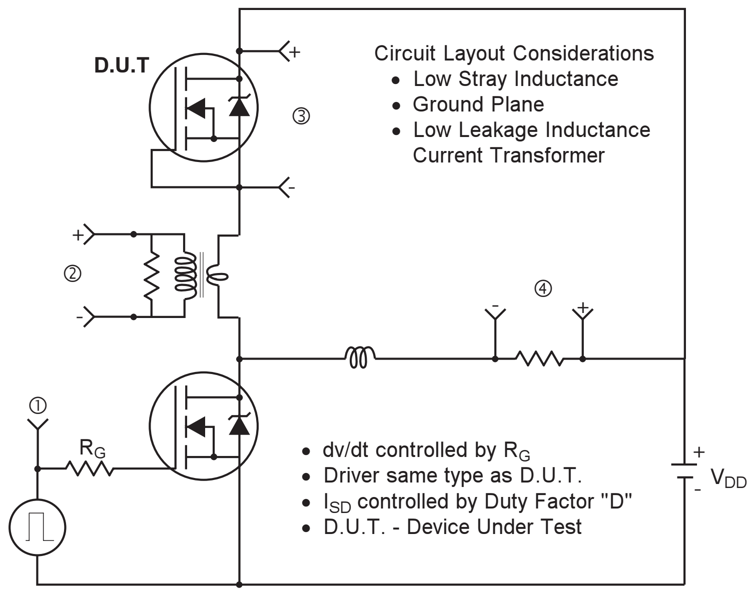
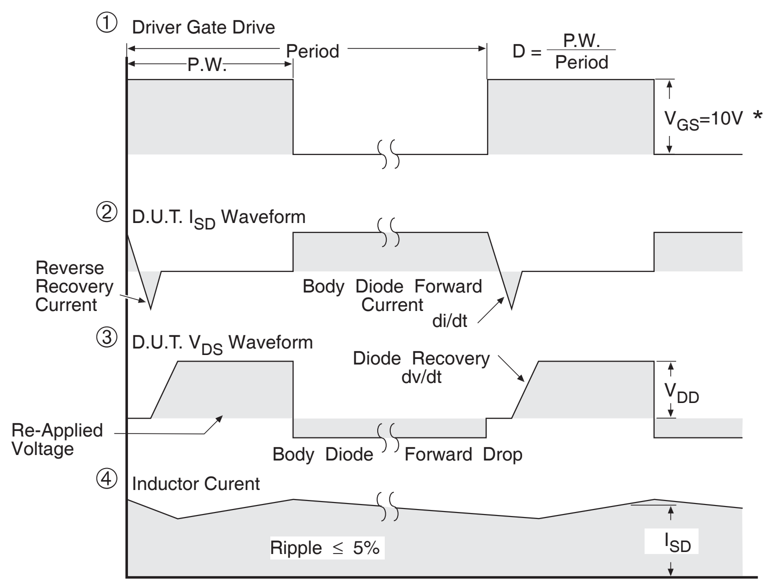


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

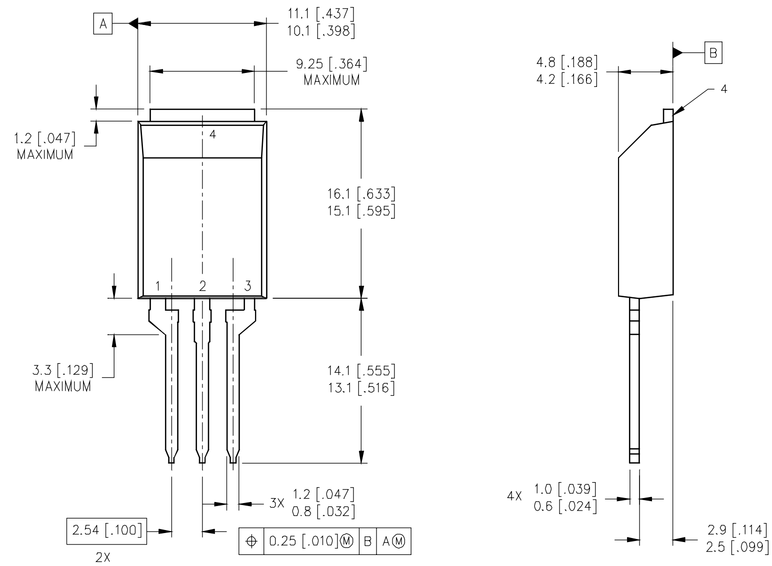




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

Super-220™ Package Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-273AA.

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, L = 0.55mH $R_G = 25\Omega$, $I_{AS} = 59A$.

③ $I_{SD} \leq 59A$, $di/dt \leq 170A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 95A.

Super-220™ not recommended for surface mount application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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