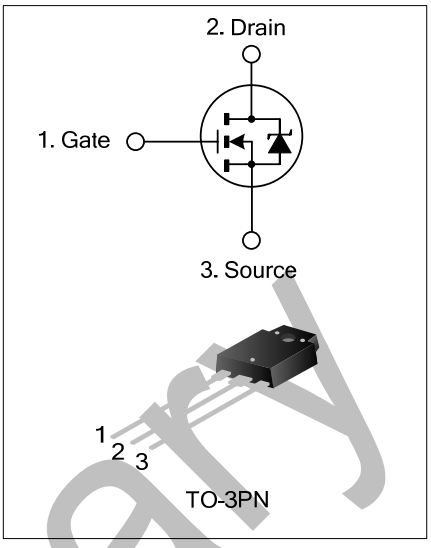
9A, 900V N-CHANNEL MOSFET

DESCRIPTION

SVF9N90PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

* 9A, 900V, $R_{DS(on)\ (typ.)}$=1.10Ω@V_{GS}=10V
* Low gate charge
* Low Crss
* Fast switching
* Improved dv/dt capability

NOMENCLATURE

S V F X N E X X X

Silan VDMOS Code of F-Cell process

Nominal current, using 1 or 2 digits:
Example: 4 denotes 4A,
20 denotes 20A,
08 denotes 0.8A

N denotes N Channel

Special Features indication, May be omitted.
Example: E denotes embeded ESD structure

Nominal Voltage,using 2 digits
Example: 50 denotes 500V,
65 denotes 650V.

Package information.
Example:PN:TO-3PN.

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF9N90PN	TO-3PN	9N90	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (unless otherwise noted, T_C=25°C)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	900	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	9.0	A
	T_C=100°C		5.7	
Drain Current Pulsed		I_{DM}	36.0	A
Power Dissipation (T_C=25°C)		P_D	280	W
-Derate above 25°C			2.22	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	890	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.45	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	40	°C/W

ELECTRICAL CHARACTERISTICS (unless otherwise noted, T_C=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V，I_D=250μA	900	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=900V，V_{GS}=0V	--	--	10	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±25V，V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}，I_D=250μA	2.0	--	4.0	V
On State Resistance	$R_{DS(on)}$	V_{GS}=10V，I_D=4.5A	--	1.10	1.4	Ω
Input Capacitance	C_{iss}	V_{DS}=25V，V_{GS}=0V，f=1.0MHz	--	2000	--	pF
Output Capacitance	C_{oss}		--	160	--	
Reverse Transfer Capacitance	C_{rss}		--	12	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=450V， R_G=25Ω，I_D=9.0A (Note2,3)	--	45	--	ns
Turn-on Rise Time	t_r		--	115	--	
Turn-off Delay Time	$t_{d(off)}$		--	80	--	
Turn-off Fall Time	t_f		--	70	--	
Total Gate Charge	Q_g	V_{DD}=720V，V_{GS}=10V，I_D=9.0A (Note 2,3)	--	40	--	nC
Gate-Source Charge	Q_{gs}		--	12	--	
Gate-Drain Charge	Q_{gd}		--	16	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

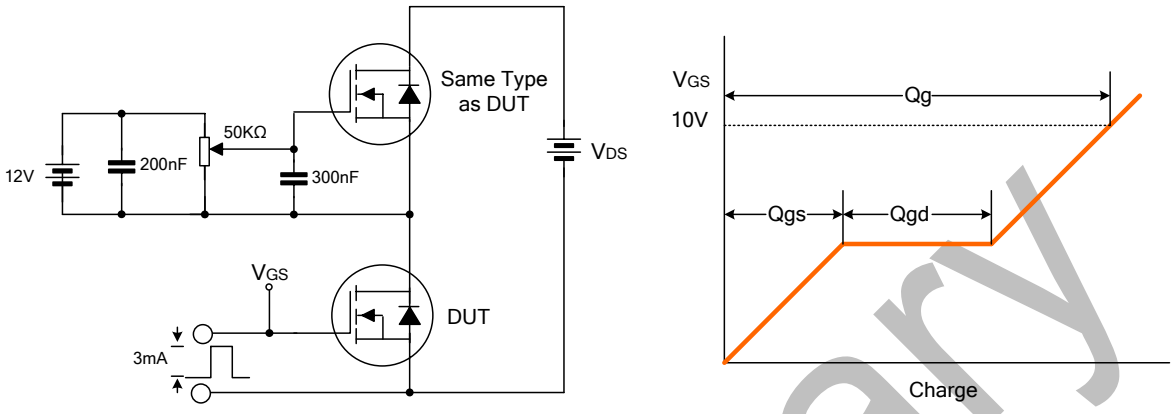
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	9.0	A
Pulsed Source Current	I_{SM}		--	--	36.0	
Diode Forward Voltage	V_{SD}	I_S=9.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=9.0A,V_{GS}=0V, dI_F/dt=100A/μS (Note2)	--	540	--	ns
Reverse Recovery Charge	Q_{rr}		--	6.1	--	μC

Notes:

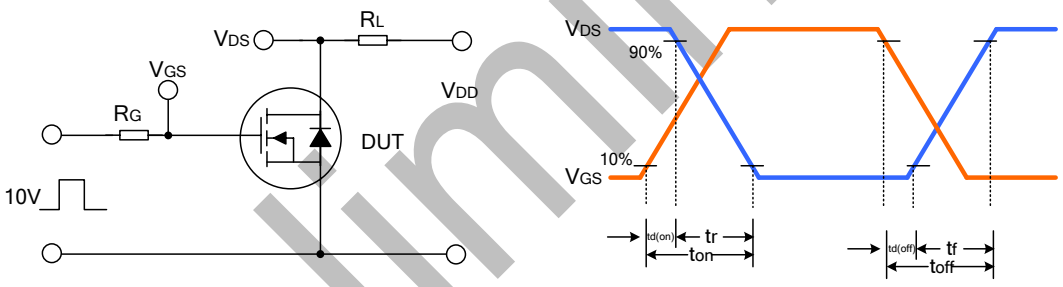
1. L=21mH，I_{AS}=9.0A，V_{DD}=50V，R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL TEST CIRCUIT

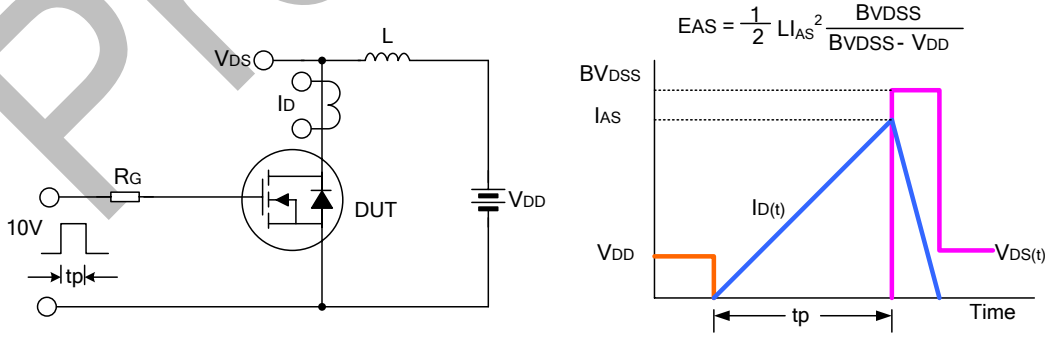
Gate Charge Test Circuit & Waveform



Switching Test Circuit & Waveform

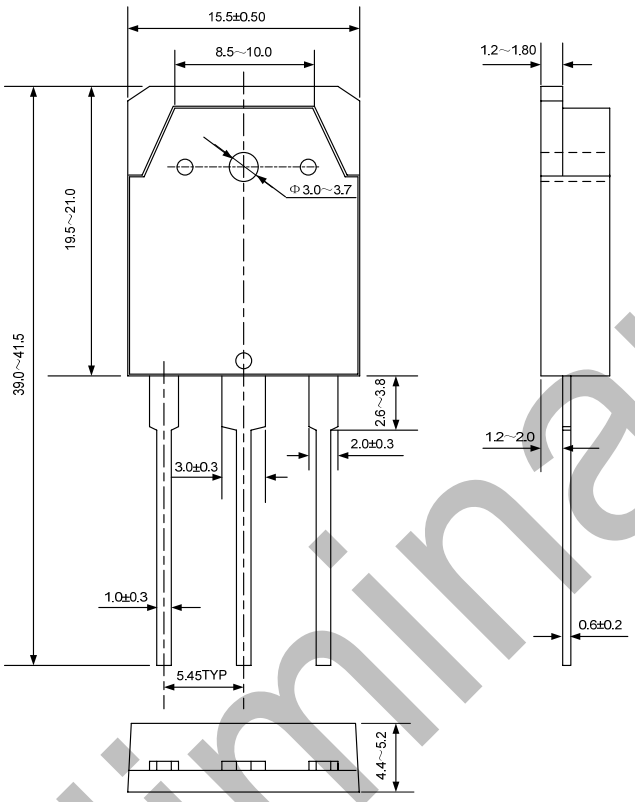


EAS Test Circuit & Waveform



PACKAGE OUTLINE

TO-3PN UNIT：mm



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