

## SWITCHING REGULATOR APPLICATIONS

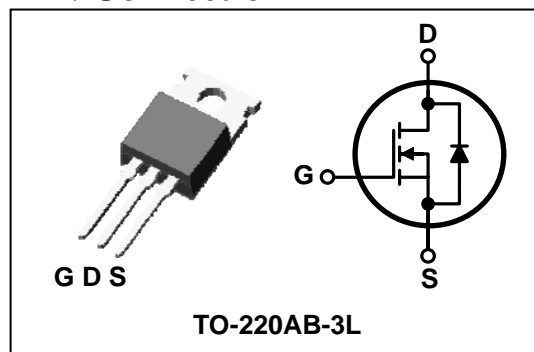
### Features

- High Voltage:  $BV_{DSS}=600V$ (Min.)
- Low  $C_{rss}$  :  $C_{rss}=18pF$ (Typ.)
- Low gate charge :  $Qg=35nc$ (Typ.)
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=0.75\Omega$ (Max.)

### Ordering Information

Type No.	Marking	Package Code
SMK1060P	SMK1060	TO-220AB-3L

### PIN Connection



### Absolute maximum ratings ( $T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	600	V
Gate-source voltage	$V_{GSS}$	$\pm 30$	V
Drain current (DC)*	$I_D$	( $T_C=25^\circ C$ )	10
		( $T_C=100^\circ C$ )	6.32
Drain current (Pulsed)*	$I_{DM}$	40	A
Drain power dissipation	$P_D$	120	W
Avalanche current (Single) ②	$I_{AS}$	10	A
Single pulsed avalanche energy ②	$E_{AS}$	490	mJ
Avalanche current (Repetitive) ①	$I_{AR}$	10	A
Repetitive avalanche energy ①	$E_{AR}$	11.6	mJ
Junction temperature	$T_J$	150	$^\circ C$
Storage temperature range	$T_{stg}$	-55~150	

\* Limited by maximum junction temperature

Characteristic	Symbol	Typ.	Max	Unit
Thermal resistance	Junction-case	$R_{th(J-C)}$	-	1.04
	Junction-ambient	$R_{th(J-a)}$	-	62.5

## Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Drain-source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0	600	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> =V <sub>GS</sub>	2.0	-	4.0	V	
Drain-source cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V	-	-	1	μA	
Gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V	-	-	±100	nA	
Drain-source on-resistance ④	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =5.0A	-	0.60	0.75	Ω	
Forward transfer conductance ④	g <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =5.0A	-	8.0	-	S	
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V f=1MHz	-	2000	2350	pF	
Output capacitance	C <sub>oss</sub>		-	160	215		
Reverse transfer capacitance	C <sub>rss</sub>		-	18	-		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =300V, I <sub>D</sub> =10A R <sub>G</sub> =25Ω	-	23	-	ns	
Rise time	t <sub>r</sub>		-	69	-		
Turn-off delay time	t <sub>d(off)</sub>		③④	-	144		-
Fall time	t <sub>f</sub>		-	77	-		
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =480V, V <sub>GS</sub> =10V I <sub>D</sub> =10A	-	35	57	nC	
Gate-source charge	Q <sub>gs</sub>		③④	-	9.0		-
Gate-drain charge	Q <sub>gd</sub>		-	10	-		

## Source-Drain Diode Ratings and Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

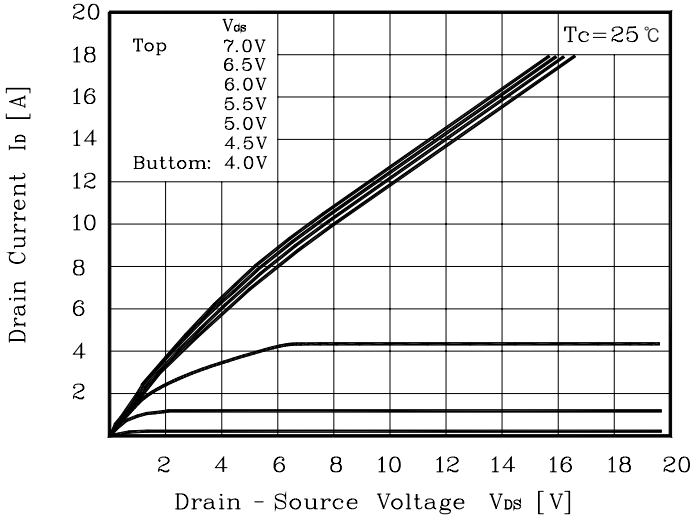
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Source current (DC)	I <sub>S</sub>	Integral reverse diode in the MOSFET	-	-	10	A
Source current (Pulsed) ①	I <sub>SM</sub>		-	-	40	
Forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	-	-	1.4	V
Reverse recovery time	t <sub>rr</sub>	I <sub>S</sub> =10A, V <sub>GS</sub> =0, di <sub>s</sub> /dt=100A/ us	-	470	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	6	-	μC

Note ;

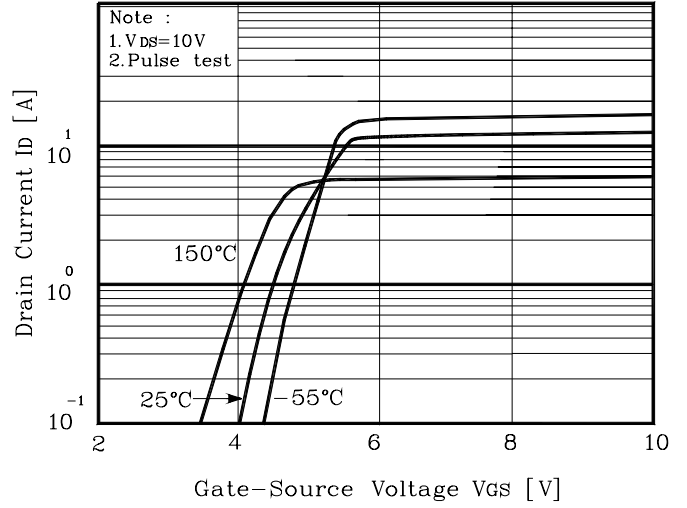
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=10mH, I<sub>AS</sub>=9.5A, V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω , Starting T<sub>J</sub> = 25°C
- ③ Pulse Test : Pulse Width < 300us, Duty cycle ≤ 2%
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

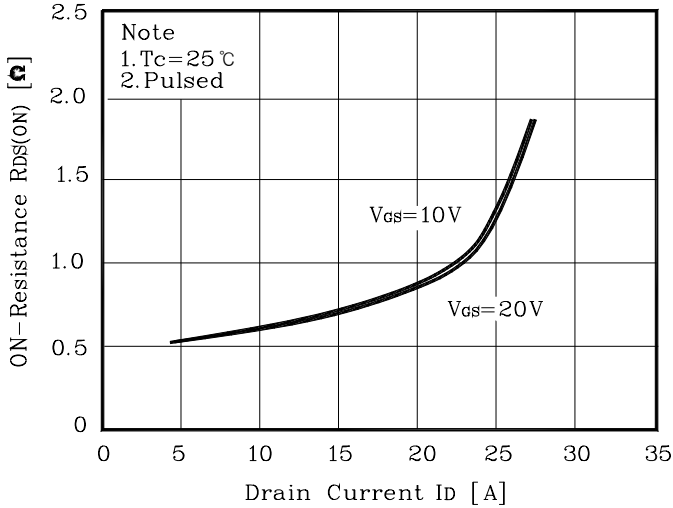
**Fig. 1  $I_D - V_{DS}$**



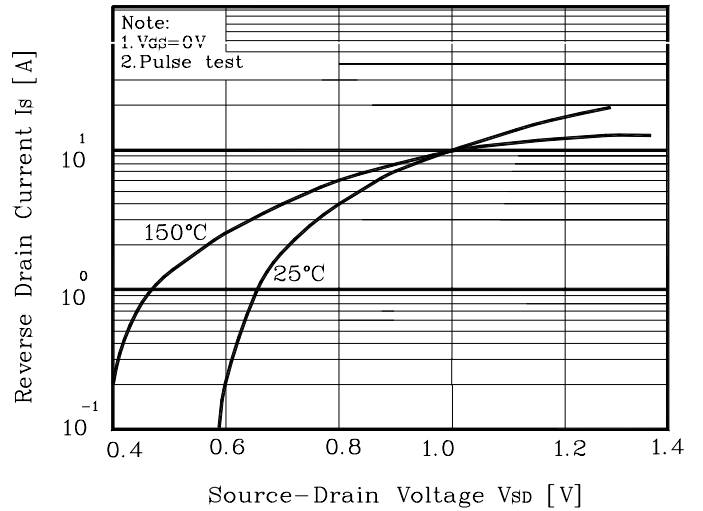
**Fig. 2  $I_D - V_{GS}$**



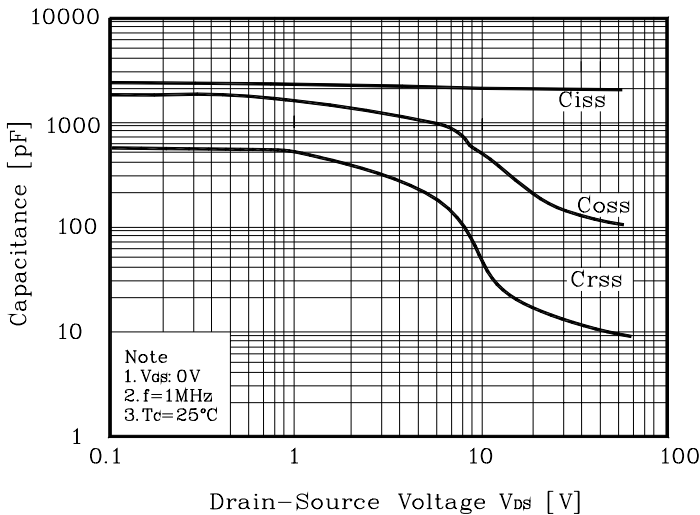
**Fig. 3  $R_{DS(on)} - I_D$**



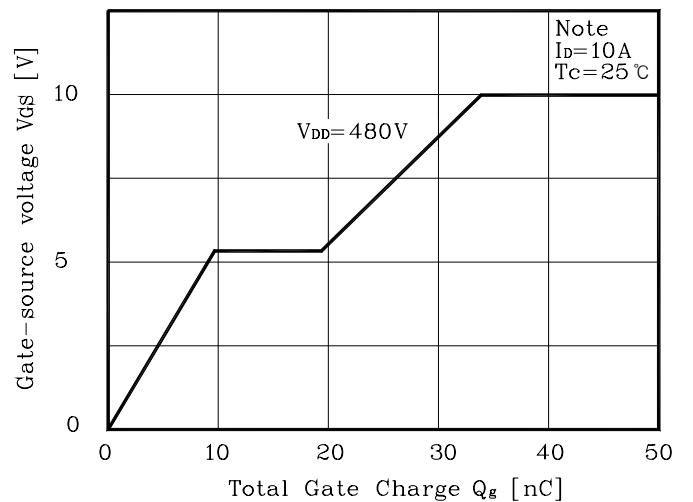
**Fig. 4  $I_S - V_{SD}$**



**Fig. 5 Capacitance -  $V_{DS}$**



**Fig. 6  $V_{GS} - Q_G$**



Electrical Characteristic Curves

Fig. 7  $V_{DSS} - T_J$

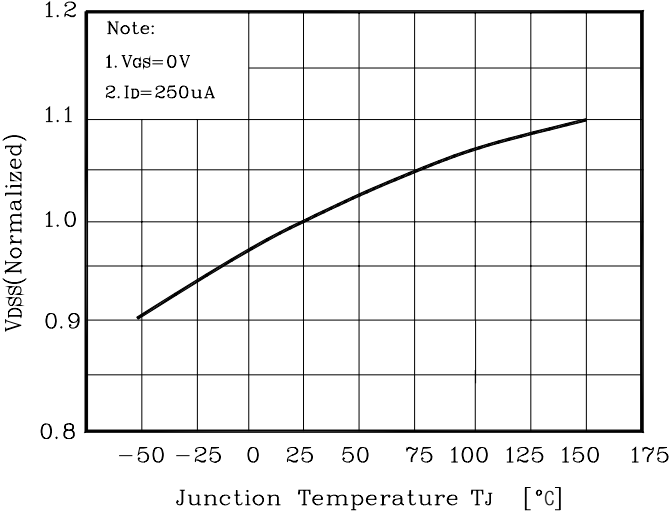


Fig.8  $R_{DS(on)} - T_J$

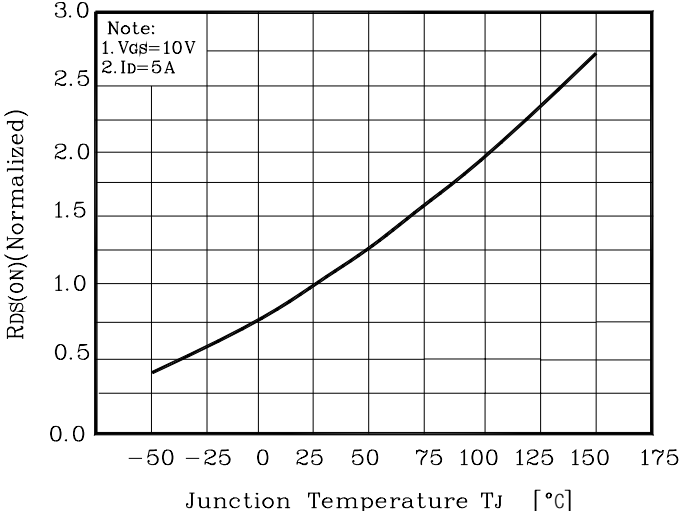


Fig. 9  $I_D - T_C$

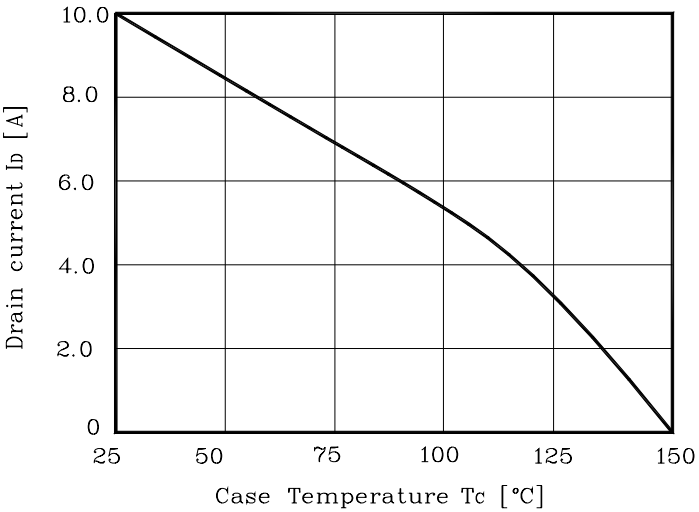


Fig. 10 Safe Operating Area

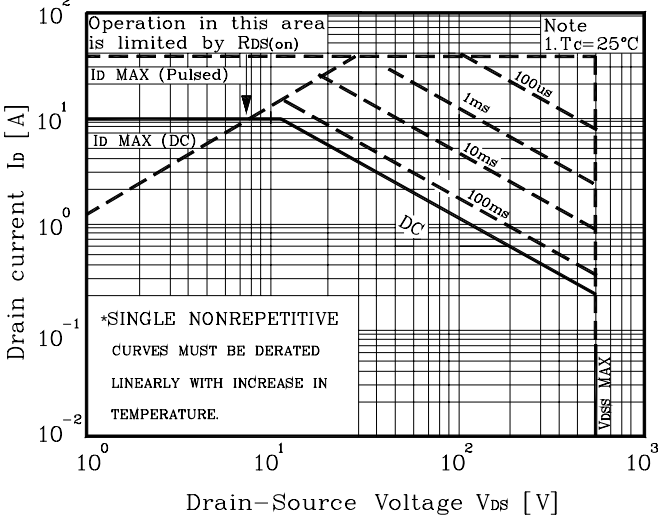


Fig. 10 Gate Charge Test Circuit & Waveform

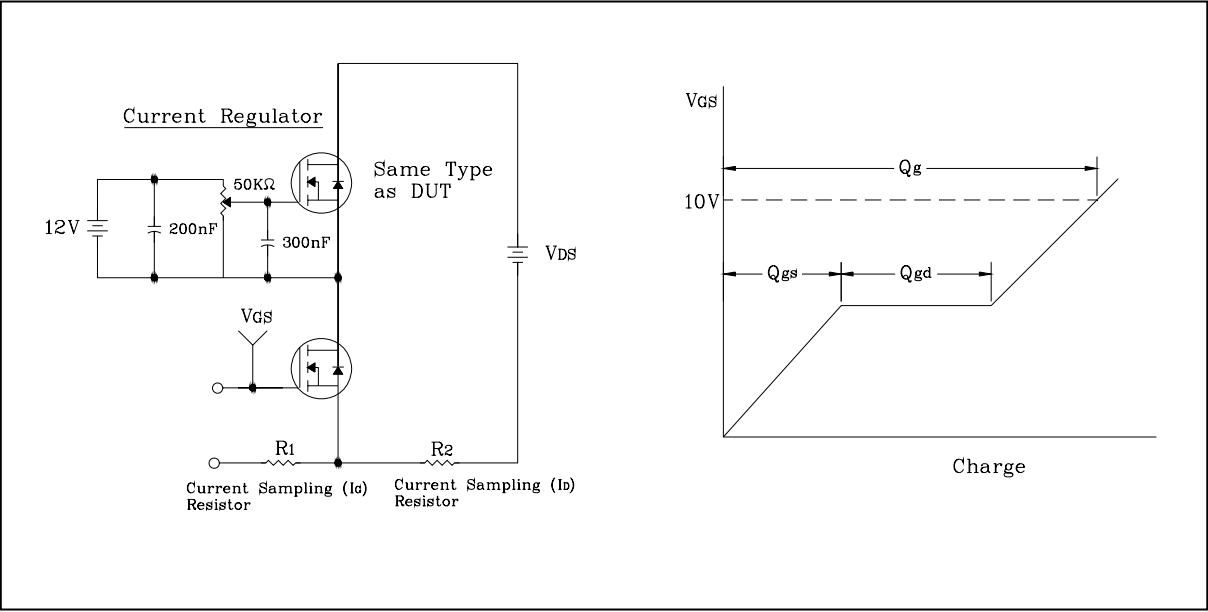


Fig. 11 Resistive Switching Test Circuit & Waveform

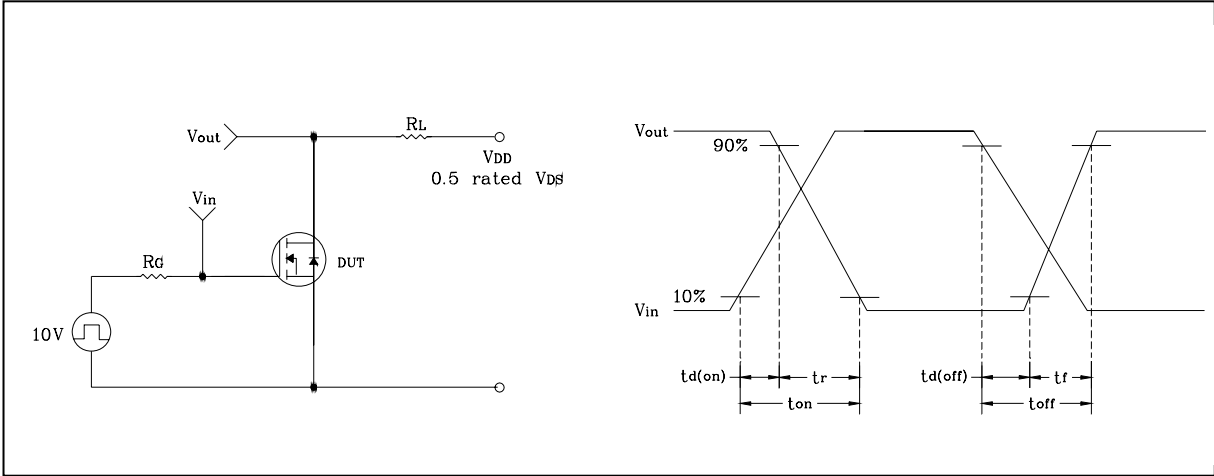


Fig. 12 E<sub>AS</sub> Test Circuit & Waveform

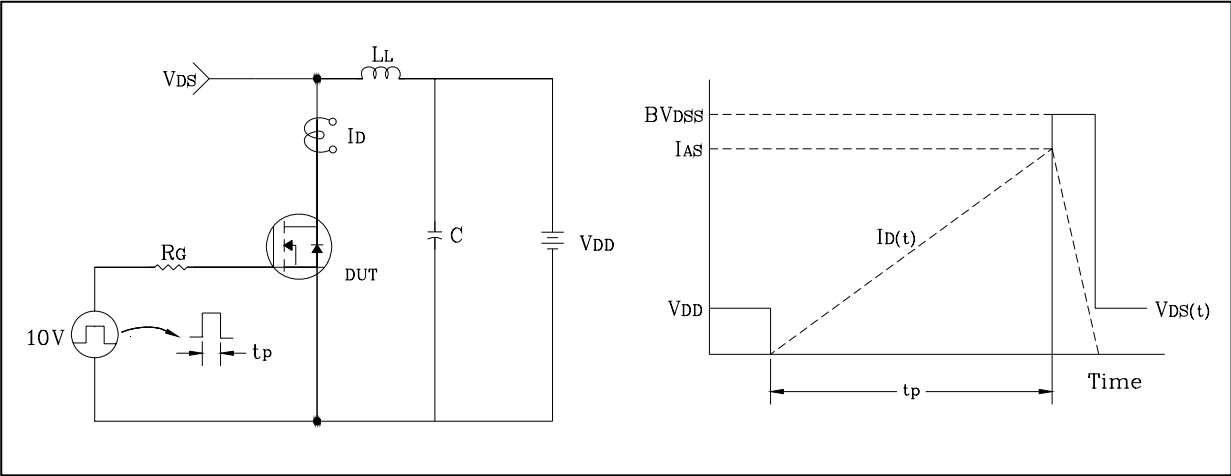
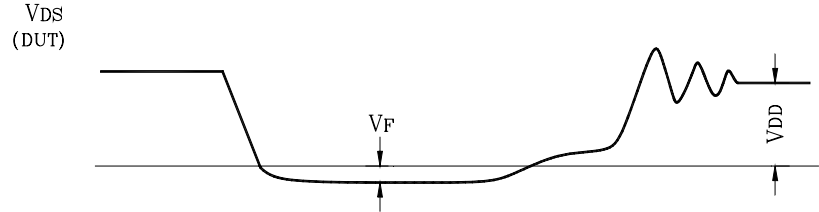
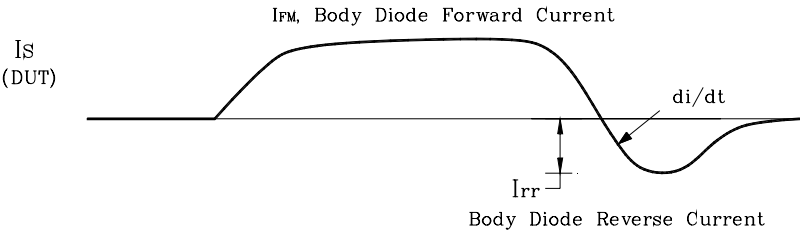
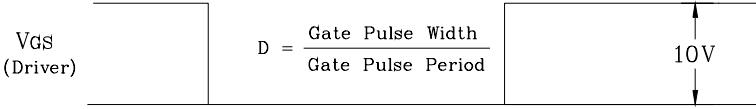
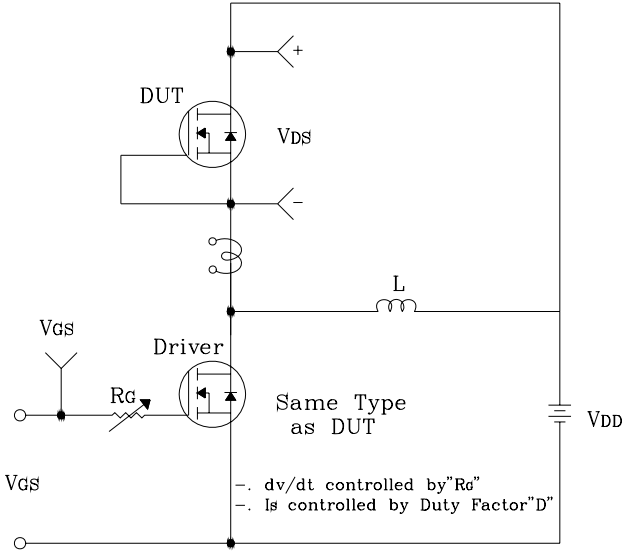
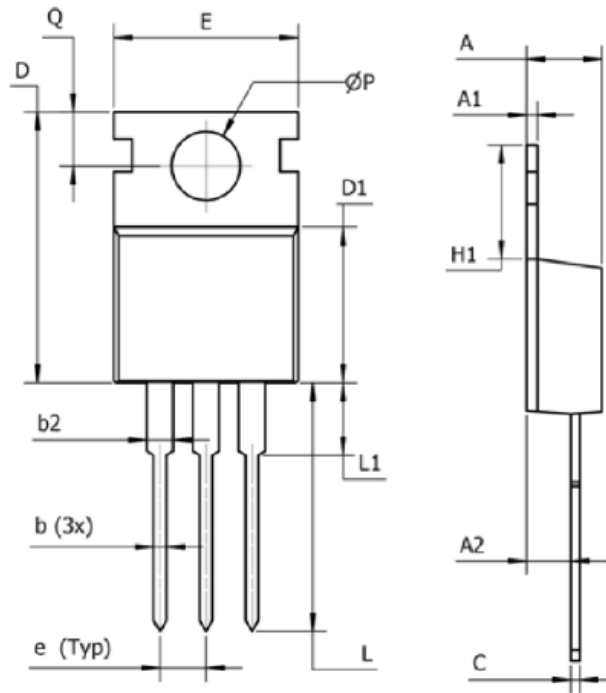


Fig. 13 Diode Reverse Recovery Time Test Circuit & Waveform



Outline Dimension



DIM	MM	INCHES
D	14.22-16.51	0.560-0.650
ØP	Ø3.53-4.09	Ø0.139-0.161
H1	5.84-6.86	0.230-0.270
b	0.38-1.02	0.015-0.040
b2	1.14-1.78	0.045-0.070
D1	8.38-9.02	0.330-0.355
e	2.54	0.100
E	9.65-10.67	0.380-0.420
L1	6.35(MAX)	0.250(MAX)
A	3.56-4.83	0.140-0.190
A1	0.51-0.71	0.020-0.028
L	12.70-14.73	0.500-0.580
A2	2.03-2.92	0.080-0.115
Q	2.54-3.43	0.100-0.135
C	0.36-0.61	0.014-0.024

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