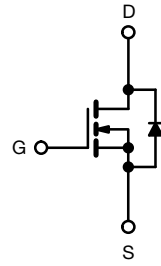
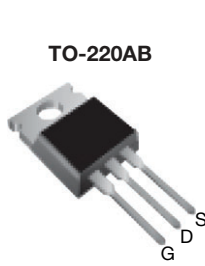


Power MOSFET



N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche, and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


 Available
RoHS*
 Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY	
V_{DS} (V)	650
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.93
Q_g max. (nC)	48
Q_{gs} (nC)	12
Q_{gd} (nC)	19
Configuration	Single

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Single transistor flyback
- Single transistor forward


ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFB9N65APbF
Lead (Pb)-free and halogen-free	IRFB9N65APbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	8.5	A
		$T_C = 100\text{ }^\circ\text{C}$	5.4	
Pulsed drain current ^a	I_{DM}	21		
Linear derating factor		1.3	W/ $^\circ\text{C}$	
Single pulse avalanche energy ^b	E_{AS}	325	mJ	
Repetitive avalanche current ^a	I_{AR}	5.2	A	
Repetitive avalanche energy ^a	E_{AR}	16	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	167	W
Peak diode recovery dV/dt ^c	dV/dt	2.8	V/ns	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) ^d	For 10 s	300		
Mounting torque	6-32 or M3 screw	10	lbf · in	
		1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 24\text{ mH}$, $R_g = 25\text{ }^\circ\Omega$, $I_{AS} = 5.2\text{ A}$ (see fig. 12)
- $I_{SD} \leq 5.2\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.75	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	650	-	-	V	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$	-	670	-	mV/°C	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V	
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 520\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 5.1\text{ A}^b$	-	-	0.93	Ω	
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 3.1\text{ A}$	3.9	-	-	S	
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	1417	-	pF	
Output capacitance	C_{oss}		-	177	-		
Reverse transfer capacitance	C_{rss}		-	7.0	-		
Output capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	1912	-	
Effective output capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 520\text{ V}$, $f = 1.0\text{ MHz}$	-	48	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 5.2\text{ A}$, $V_{DS} = 400\text{ V}$ see fig. 6 and 13 ^b	-	-	48	nC
Gate-source charge	Q_{gs}			-	-	12	
Gate-drain charge	Q_{gd}			-	-	19	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 325\text{ V}$, $I_D = 5.2\text{ A}$ $R_g = 9.1\text{ }\Omega$, $R_D = 62\text{ }\Omega$, see fig. 10 ^b	-	14	-	ns	
Rise time	t_r		-	20	-		
Turn-off delay time	$t_{d(off)}$		-	34	-		
Fall time	t_f		-	18	-		
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain	0.5	-	3.3	Ω	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.2	A	
Pulsed diode forward current ^a	I_{SM}		-	-	21		
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 5.2\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.5	V	
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 5.2\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	493	739	ns	
Body diode reverse recovery charge	Q_{rr}		-	2.1	3.2	μC	
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0% to 80% V_{DS}
- Uses SiHFIB5N65A data and test conditions



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

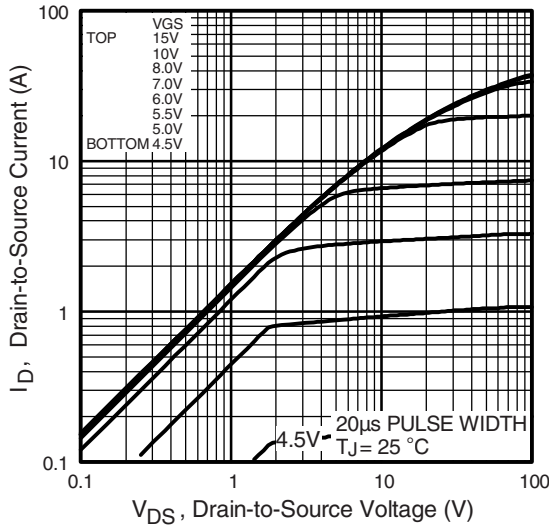


Fig. 1 - Typical Output Characteristics

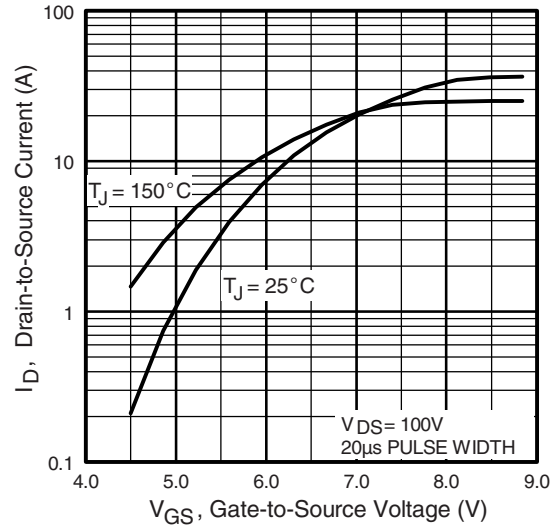


Fig. 3 - Typical Transfer Characteristics

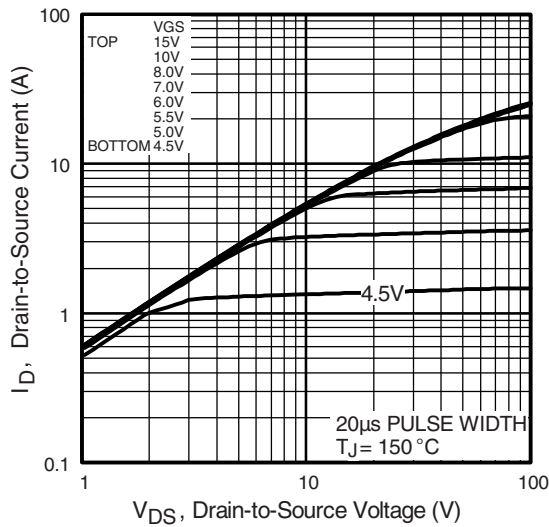


Fig. 2 - Typical Output Characteristics

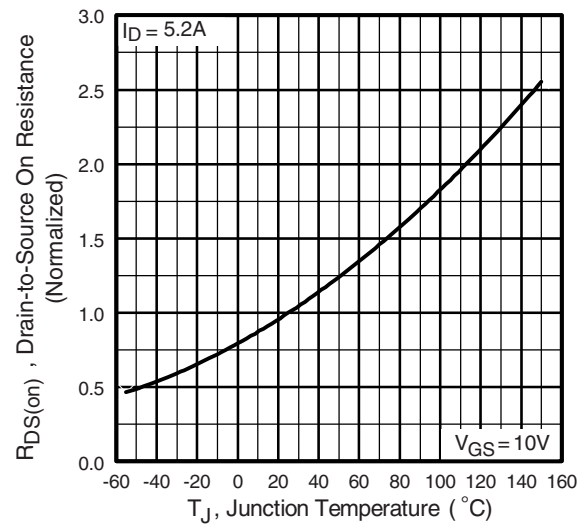


Fig. 4 - Normalized On-Resistance vs. Temperature

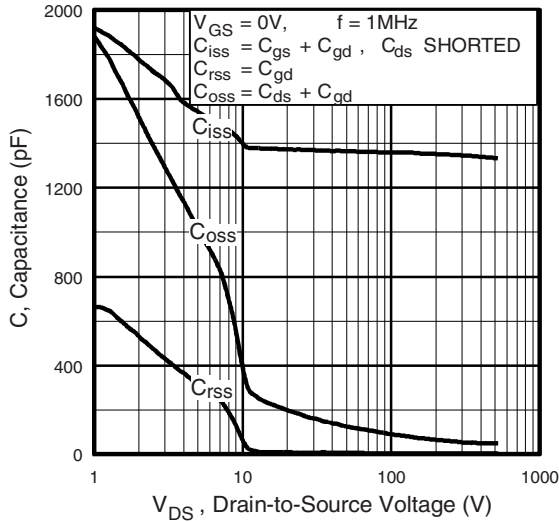


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

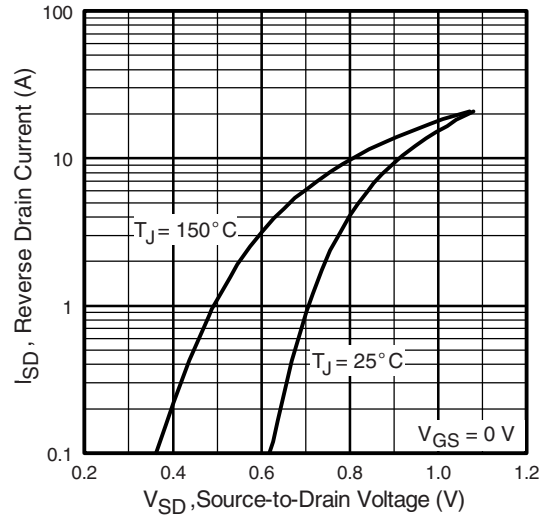


Fig. 7 - Typical Source-Drain Diode Forward Voltage

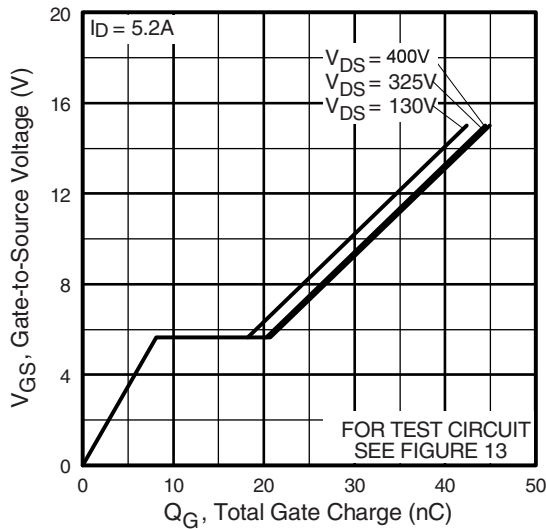


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

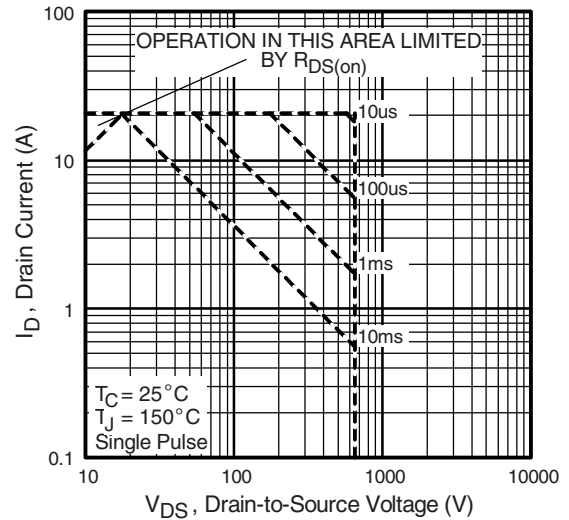


Fig. 8 - Maximum Safe Operating Area

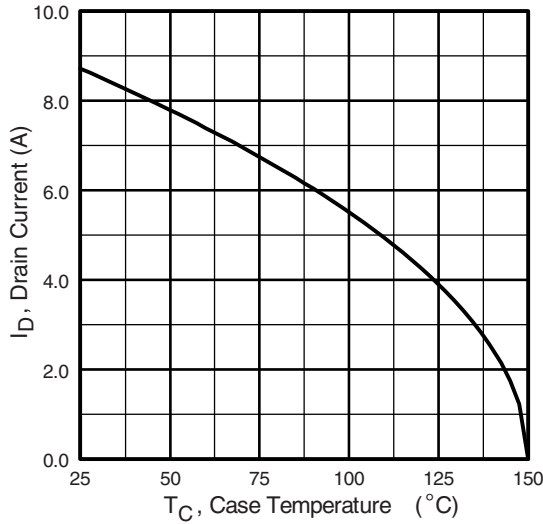


Fig. 9 - Maximum Drain Current vs. Case Temperature

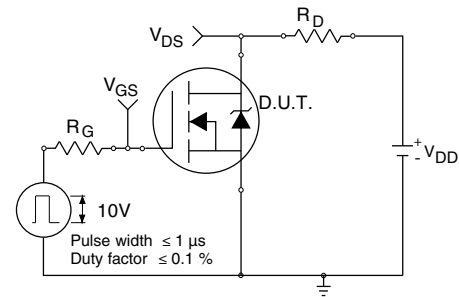


Fig. 10a - Switching Time Test Circuit

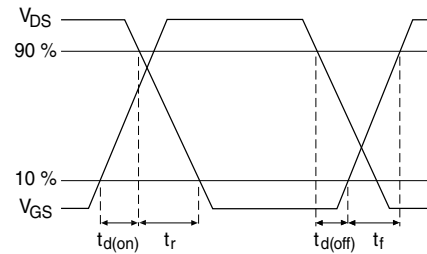


Fig. 10b - Switching Time Waveforms

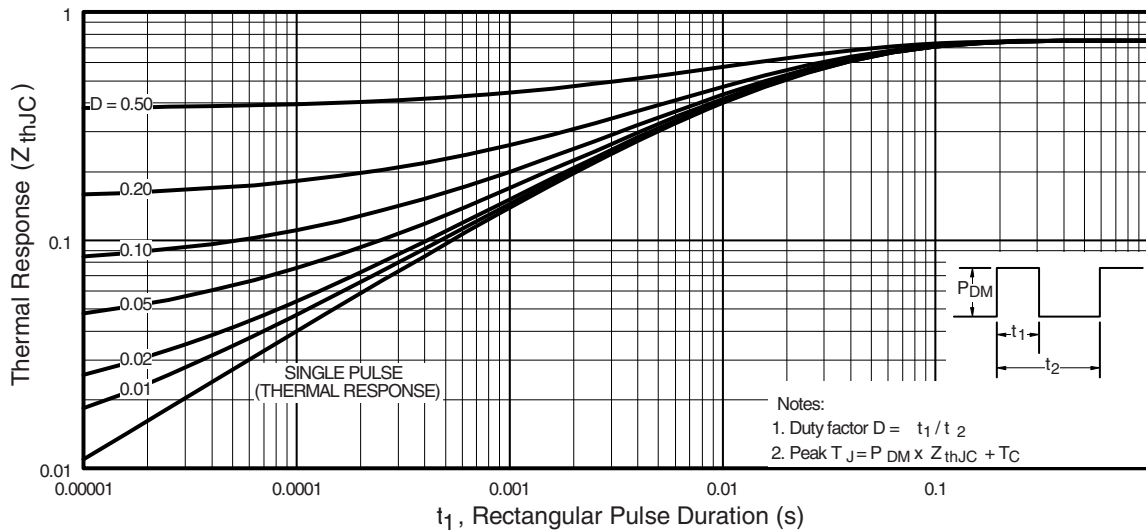


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

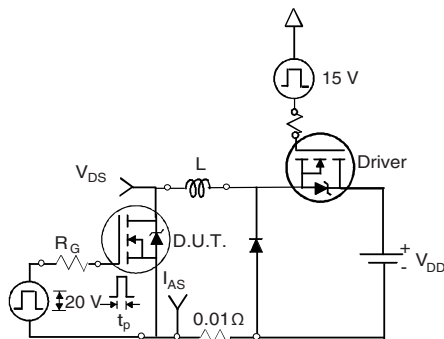


Fig. 12a - Unclamped Inductive Test Circuit

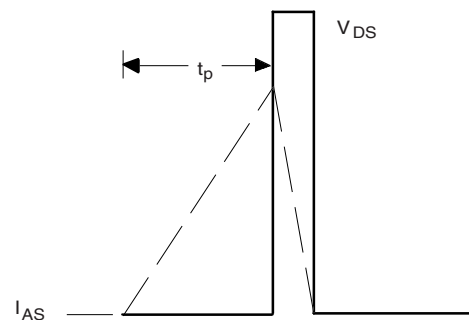


Fig. 12b - Unclamped Inductive Waveforms

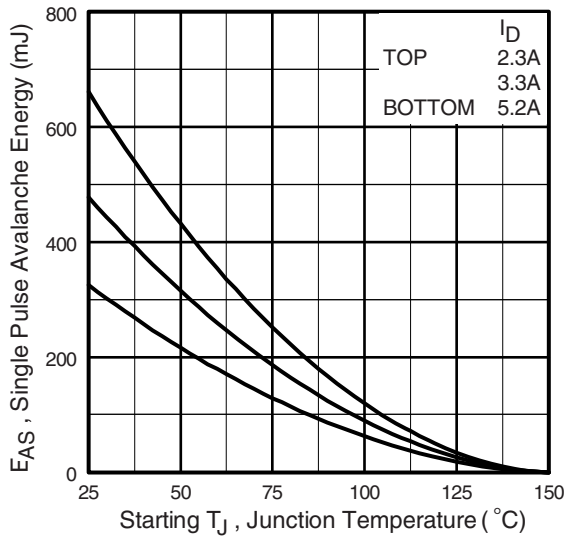


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

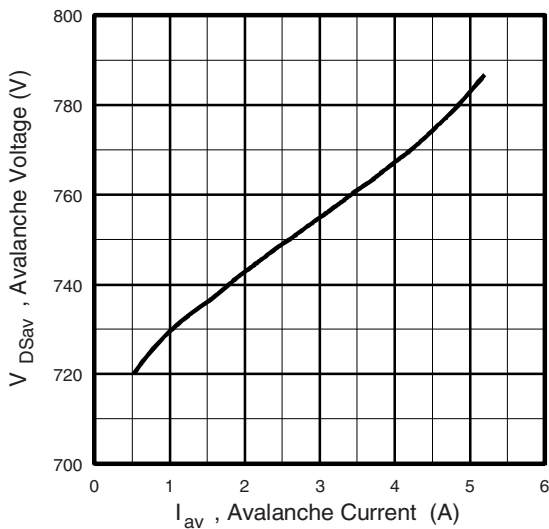


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

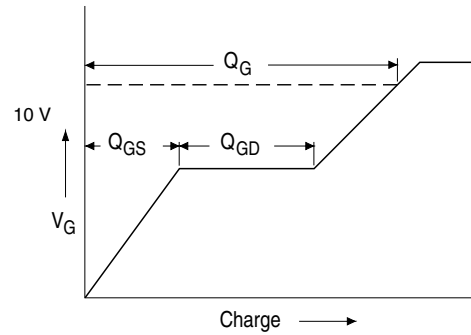


Fig. 13a - Basic Gate Charge Waveform

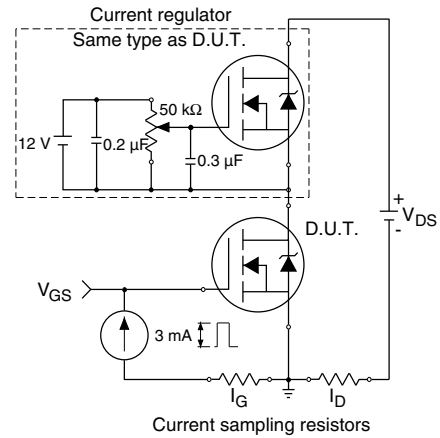
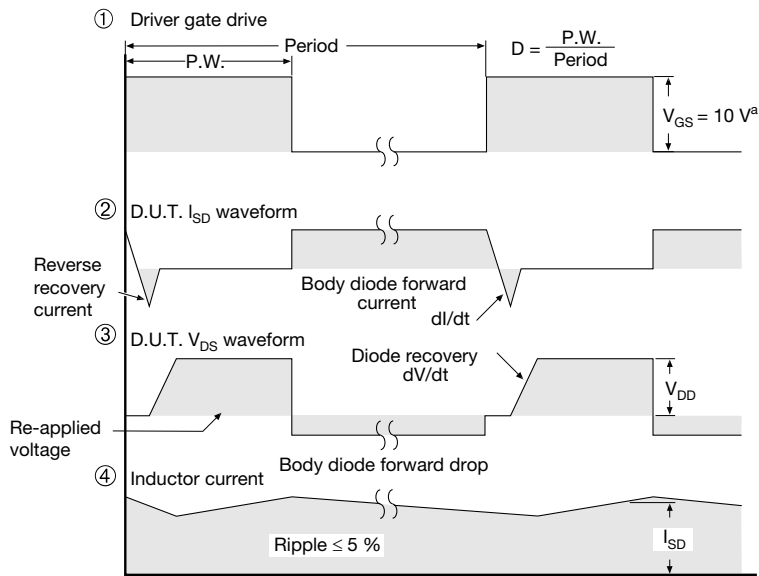
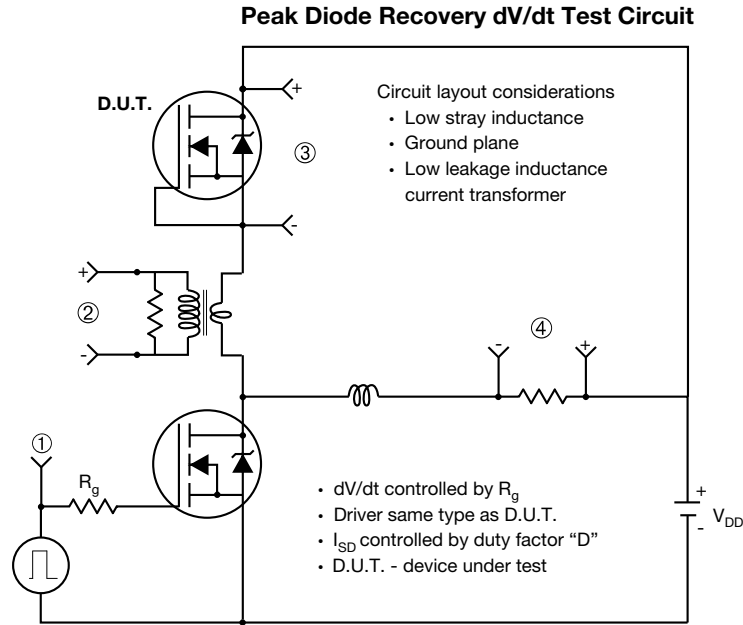


Fig. 13b - Gate Charge Test Circuit



Note

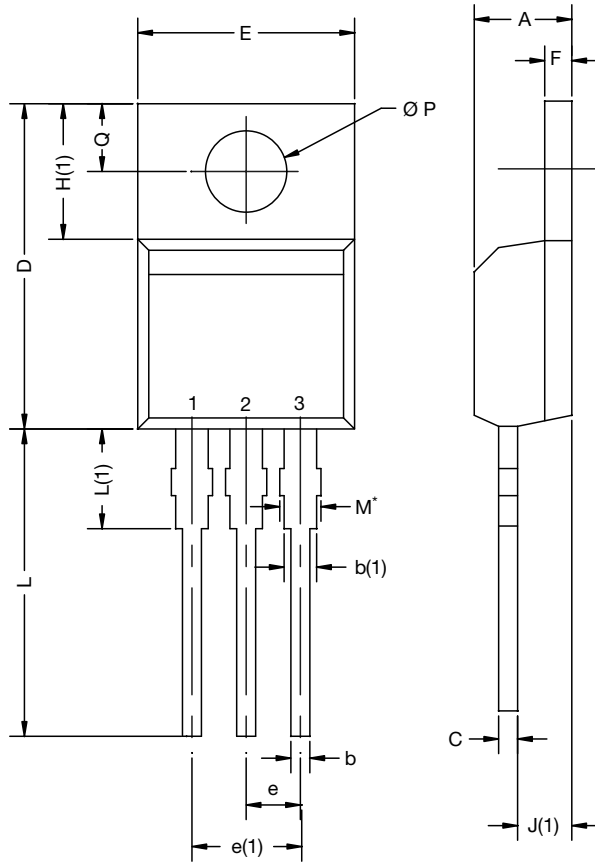
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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