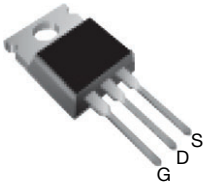
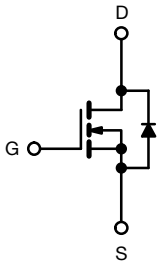
# Power MOSFET

TO-220AB




N-Channel MOSFET

## FEATURES

- Low gate charge $Q_g$ results in simple drive requirement
- Improved gate, avalanche, and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective $C_{oss}$ specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Available

RoHS* Available

**Note**

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 600 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 2.2 |
| $Q_g$ max. (nC) | 23 | |
| $Q_{gs}$ (nC) | 5.4 | |
| $Q_{gd}$ (nC) | 11 | |
| Configuration | Single | |

## APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching

## TYPICAL SMPS TOPOLOGY

- Single Transistor flyback

| ORDERING INFORMATION | |
|---|---|
| Package | TO-220AB |
| Lead (Pb)-free | IRFBC30APbF |
| Lead (Pb)-free and halogen-free | IRFBC30APbF-BE3 |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-source voltage | | | $V_{DS}$ | 600 | V |
| Gate-source voltage | | | $V_{GS}$ | ± 30 | |
| Continuous drain current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 3.6 | A |
| | | $T_C$ = 100 °C | | 2.3 | |
| Pulsed drain current [a] | | | $I_{DM}$ | 14 | |
| Linear derating factor | | | | 0.69 | W/°C |
| Single pulse avalanche energy [b] | | | $E_{AS}$ | 290 | mJ |
| Repetitive avalanche current [a] | | | $I_{AR}$ | 3.6 | A |
| Repetitive avalanche energy [a] | | | $E_{AR}$ | 7.4 | mJ |
| Maximum power dissipation | $T_C$ = 25 °C | | $P_D$ | 74 | W |
| Peak diode recovery dV/dt [c] | | | dV/dt | 7.0 | V/ns |
| Operating junction and storage temperature range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering recommendations (peak temperature) [d] | For 10 s | | | 300 | |
| Mounting torque | 6-32 or M3 screw | | | 10 | lbf · in |
| | | | | 1.1 | N · m |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Starting $T_J$ = 25 °C, L = 41 mH, $R_g$ = 25 Ω, $I_{AS}$ = 3.6 A (see fig. 12)
c. $I_{SD}$ ≤ 3.6 A, dI/dt ≤ 170 A/µs, $V_{DD}$ ≤ $V_{DS}$, $T_J$ ≤ 150 °C
d. 1.6 mm from case

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum junction-to-ambient | $R_{thJA}$ | - | 62 | °C/W |
| Case-to-sink, flat, greased surface | $R_{thCS}$ | 0.50 | - | |
| Maximum junction-to-case (drain) | $R_{thJC}$ | - | 1.7 | |

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | | 600 | - | - | V |
| $V_{DS}$ temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | | - | 0.67 | - | V/°C |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 2.0 | - | 4.5 | V |
| Gate-source leakage | $I_{GSS}$ | $V_{GS}$ = ± 30 V | | - | - | ± 100 | nA |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | | - | - | 25 | µA |
| | | $V_{DS}$ = 480 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | 250 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 2.2 A [b] | - | - | 2.2 | Ω |
| Forward transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 2.2 A [b] | | 2.1 | - | - | S |
| **Dynamic** | | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | | - | 510 | - | pF |
| Output capacitance | $C_{oss}$ | | | - | 70 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | | - | 3.5 | - | |
| Output capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | $V_{DS}$ = 1.0 V, f = 1.0 MHz | - | 730 | - | |
| | | | $V_{DS}$ = 480 V, f = 1.0 MHz | - | 19 | - | |
| Effective output capacitance | $C_{oss}$ eff. | | $V_{DS}$ = 0 V to 480 V [c] | - | 31 | - | |
| Total gate charge | $Q_g$ | $V_{GS}$ = 10 V | $I_D$ = 3.6 A, $V_{DS}$ = 480 V see fig. 6 and 13 [b] | - | - | 23 | nC |
| Gate-source charge | $Q_{gs}$ | | | - | - | 5.4 | |
| Gate-drain charge | $Q_{gd}$ | | | - | - | 11 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = 300 V, $I_D$ = 3.6 A, $R_g$ = 12 Ω, $R_D$ = 82 Ω, see fig. 10 [b] | | - | 9.8 | - | ns |
| Rise time | $t_r$ | | | - | 13 | - | |
| Turn-off delay time | $t_{d(off)}$ | | | - | 19 | - | |
| Fall time | $t_f$ | | | - | 12 | - | |
| Gate input resistance | $R_g$ | f = 1 MHz, open drain | | 0.8 | - | 4.6 | Ω |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous source-drain diode current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 3.6 | A |
| Pulsed diode forward current [a] | $I_{SM}$ | | | - | - | 14 | |
| Body diode voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 3.6 A, $V_{GS}$ = 0 V [b] | | - | - | 1.6 | V |
| Body diode reverse recovery time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 3.6 A, dI/dt = 100 A/µs [b] | | - | 400 | 600 | ns |
| Body diode reverse recovery charge | $Q_{rr}$ | | | - | 1.1 | 1.7 | µC |
| Forward turn-on time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

c. $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

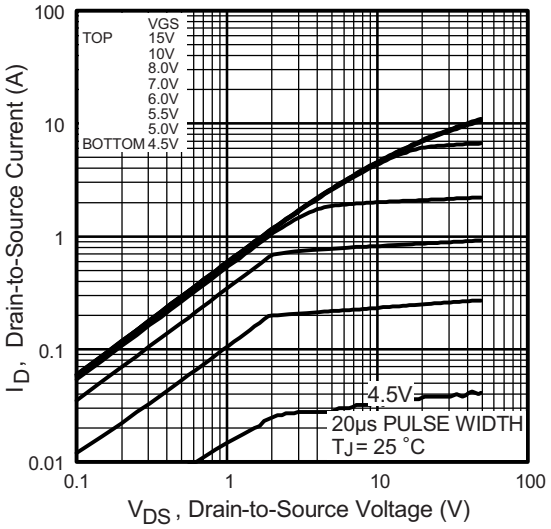



**Fig. 1 - Typical Output Characteristics**

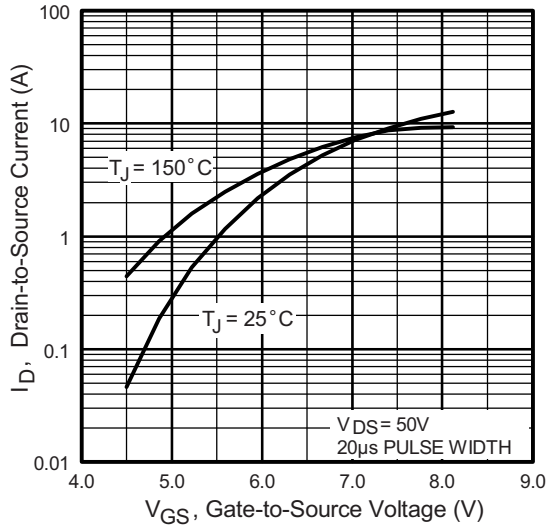



**Fig. 3 - Typical Transfer Characteristics**

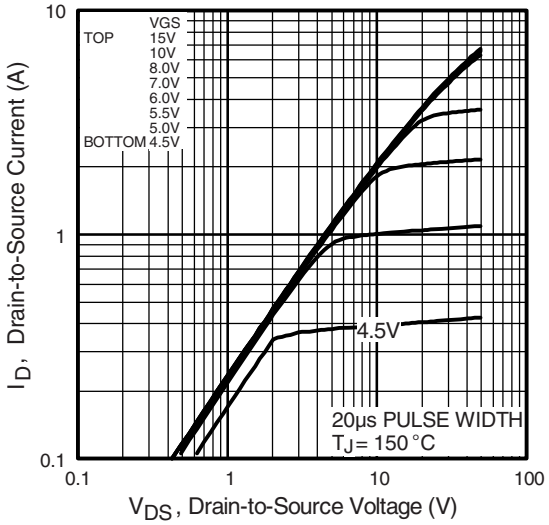



**Fig. 2 - Typical Output Characteristics**

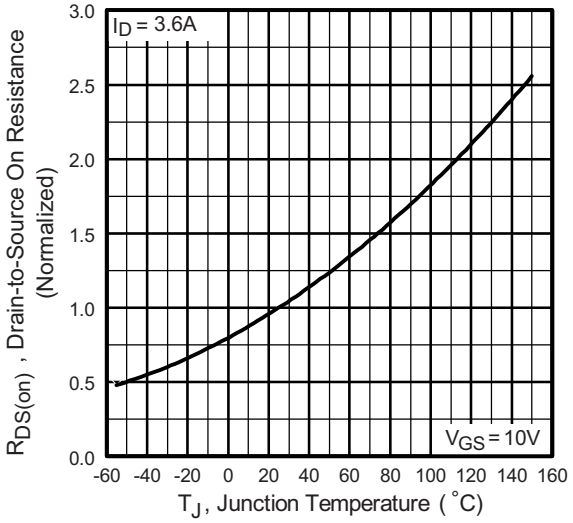



**Fig. 4 - Normalized On-Resistance vs. Temperature**

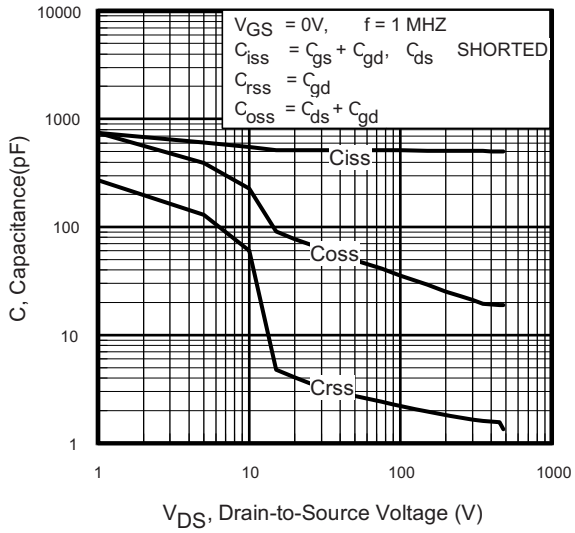



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

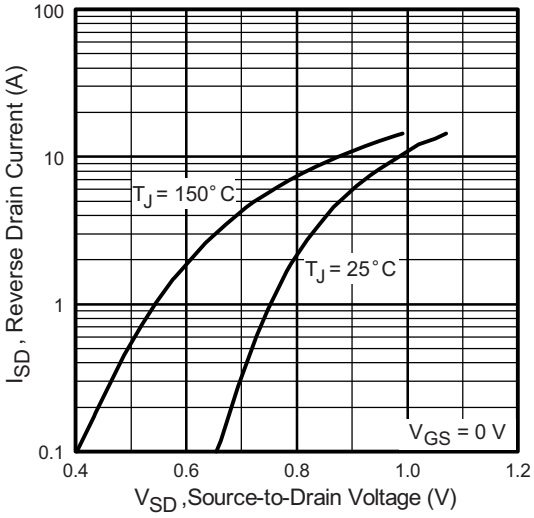



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

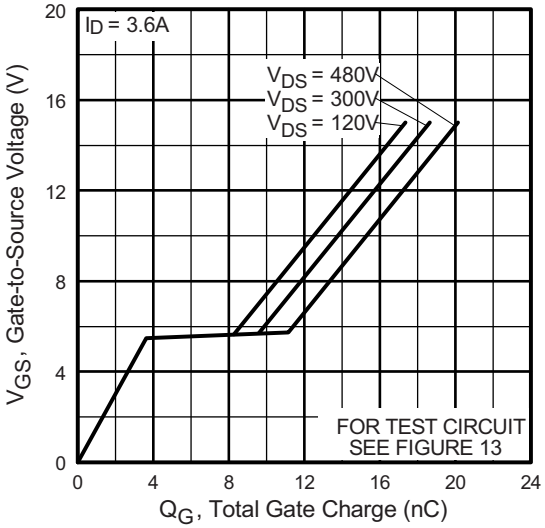



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

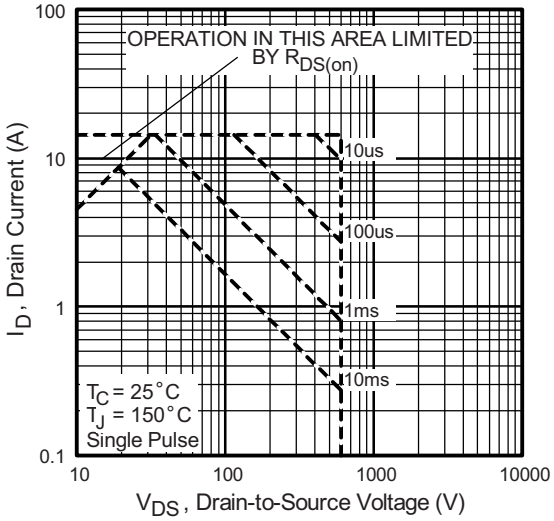



**Fig. 8 - Maximum Safe Operating Area**

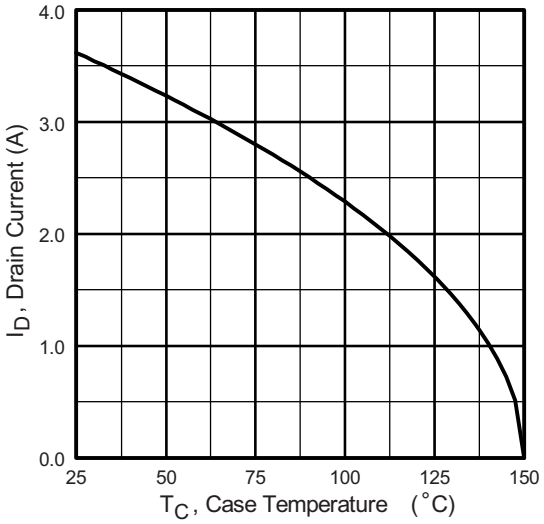



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

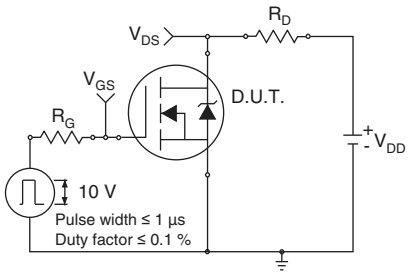



**Fig. 10a - Switching Time Test Circuit**

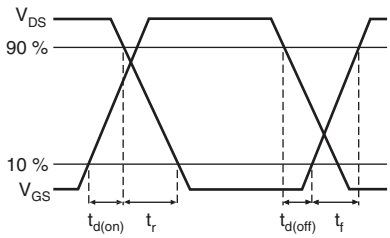



**Fig. 10b - Switching Time Waveforms**

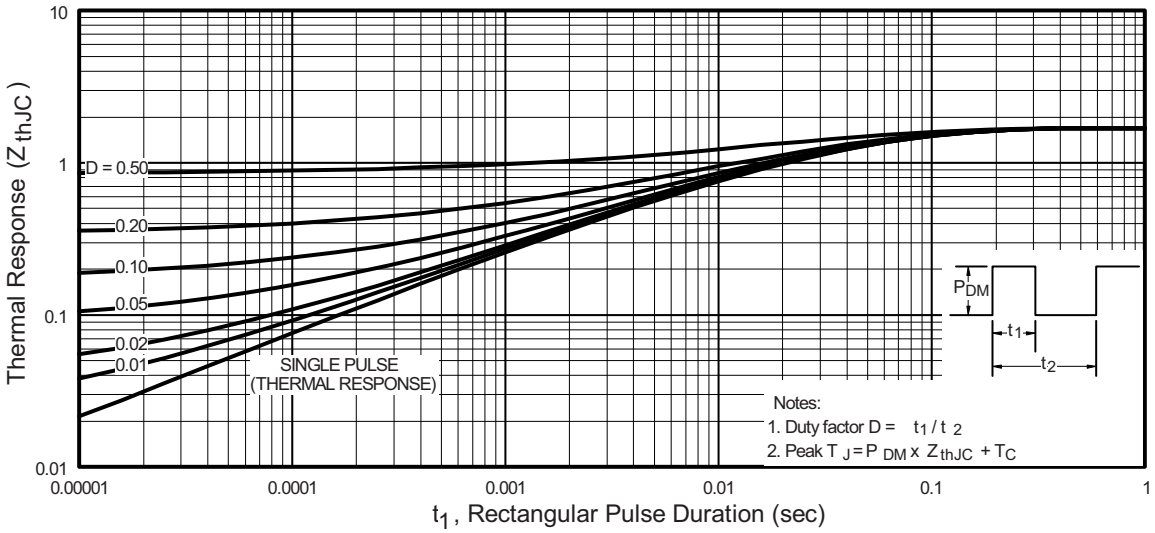



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

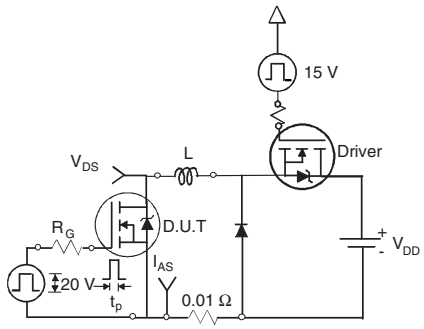



**Fig. 12a - Unclamped Inductive Test Circuit**

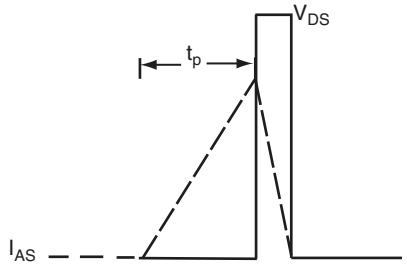



**Fig. 12b - Unclamped Inductive Waveforms**

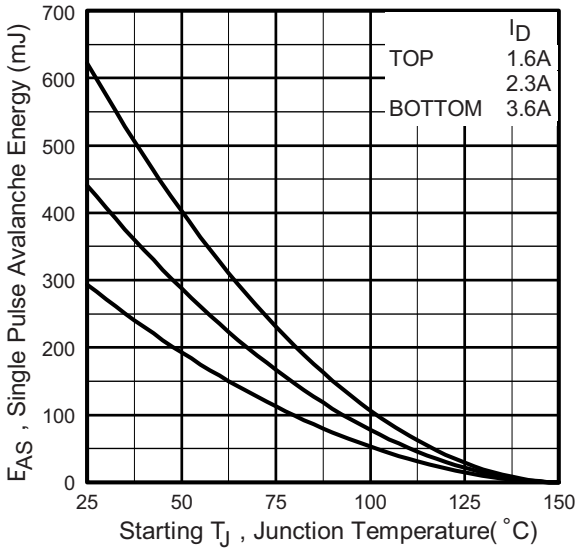



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

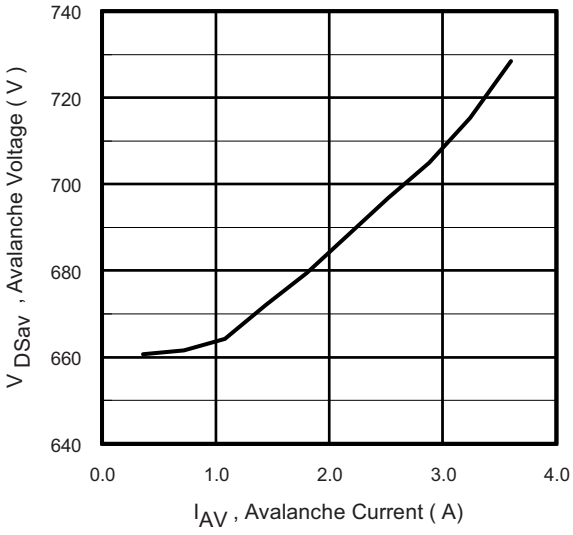



**Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current**

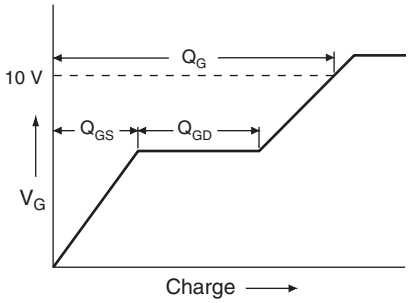



**Fig. 13a - Basic Gate Charge Waveform**

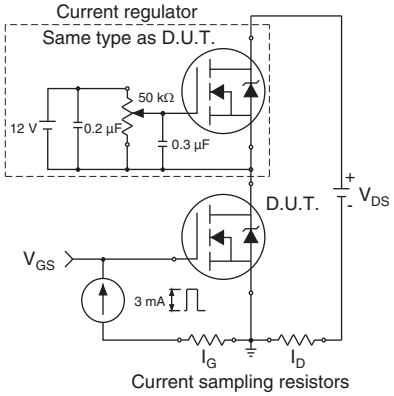
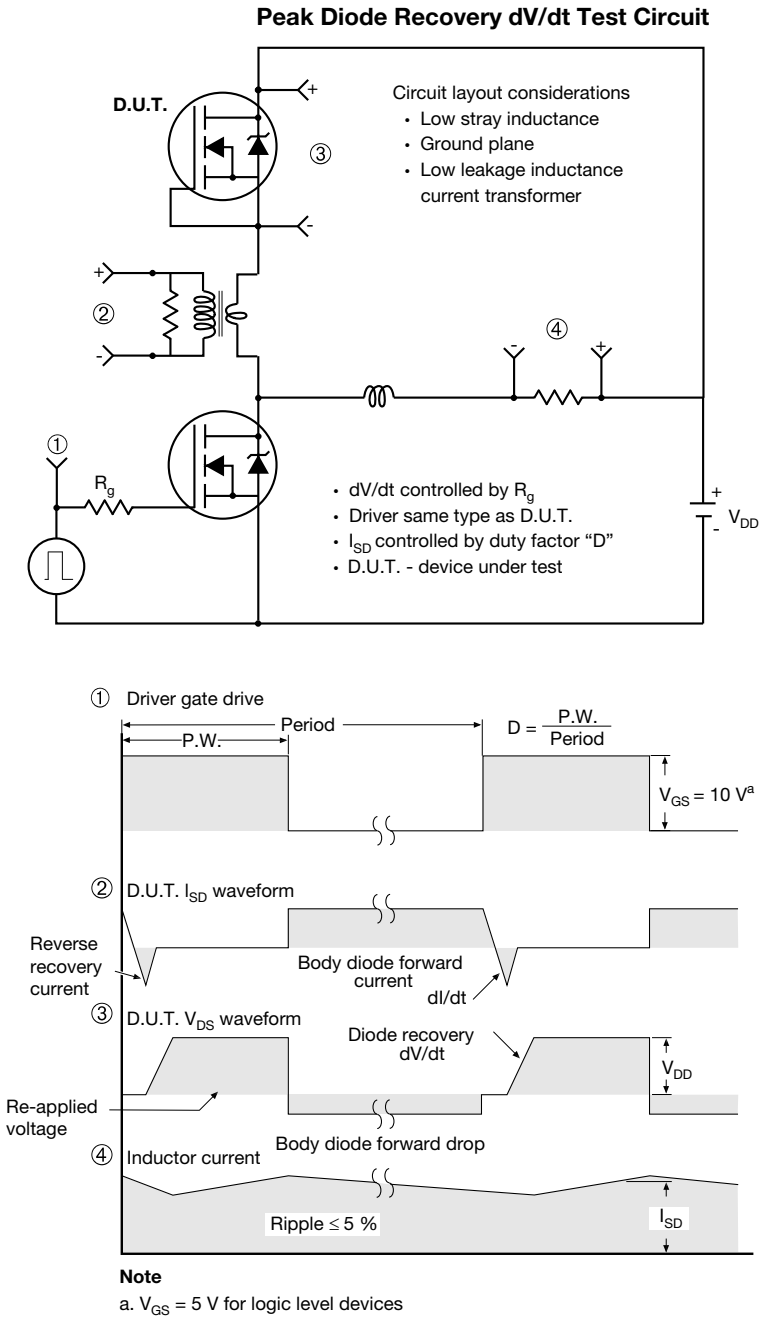



**Fig. 13b - Gate Charge Test Circuit**

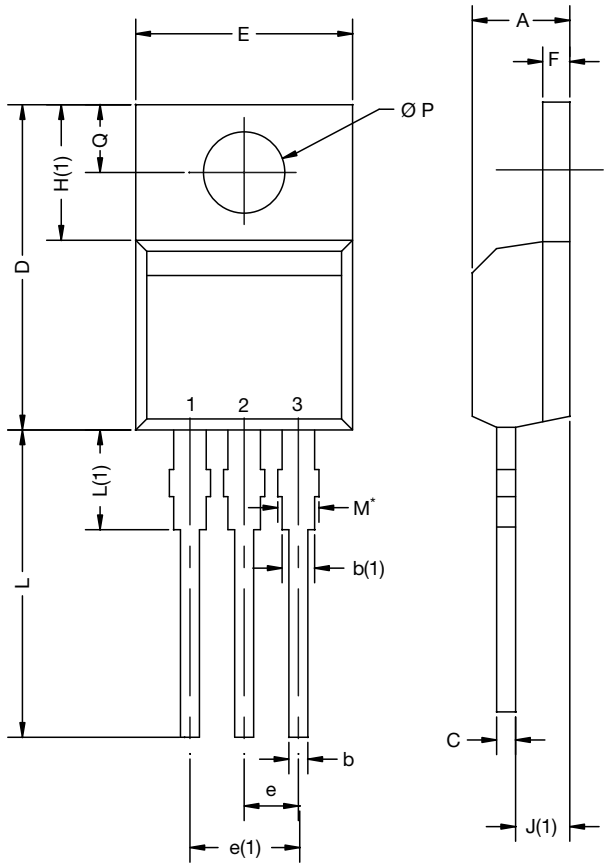



**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

# TO-220-1




| DIM. | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.24 | 4.65 | 0.167 | 0.183 |
| b | 0.69 | 1.02 | 0.027 | 0.040 |
| b(1) | 1.14 | 1.78 | 0.045 | 0.070 |
| c | 0.36 | 0.61 | 0.014 | 0.024 |
| D | 14.33 | 15.85 | 0.564 | 0.624 |
| E | 9.96 | 10.52 | 0.392 | 0.414 |
| e | 2.41 | 2.67 | 0.095 | 0.105 |
| e(1) | 4.88 | 5.28 | 0.192 | 0.208 |
| F | 1.14 | 1.40 | 0.045 | 0.055 |
| H(1) | 6.10 | 6.71 | 0.240 | 0.264 |
| J(1) | 2.41 | 2.92 | 0.095 | 0.115 |
| L | 13.36 | 14.40 | 0.526 | 0.567 |
| L(1) | 3.33 | 4.04 | 0.131 | 0.159 |
| Ø P | 3.53 | 3.94 | 0.139 | 0.155 |
| Q | 2.54 | 3.00 | 0.100 | 0.118 |
| ECN: E21-0621-Rev. D, 04-Nov-2021<br>DWG: 6031 | | | | |

**Note**

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

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