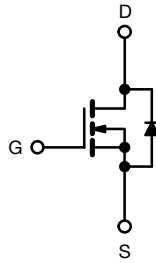
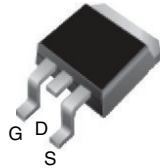


## Power MOSFET

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	600
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V   1.2
Q <sub>g</sub> max. (nC)	42
Q <sub>gs</sub> (nC)	10
Q <sub>gd</sub> (nC)	20
Configuration	Single

### FEATURES

- Low gate charge Q<sub>g</sub> results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C<sub>oss</sub> specified
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

### TYPICAL SMPS TOPOLOGIES

- Single transistor forward

ORDERING INFORMATION			
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHFBC40AS-GE3	SiHFBC40ASTRL-GE3 <sup>a</sup>	SiHFBC40ASTRR-GE3 <sup>a</sup>
Lead (Pb)-free	IRFBC40ASPbF	IRFBC40ASTRLPbF <sup>a</sup>	IRFBC40ASTRRPbF <sup>a</sup>

### Note

a. See device orientation.

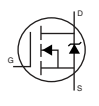
ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-source voltage	V <sub>DS</sub>		600	V	
Gate-source voltage	V <sub>GS</sub>		± 30		
Continuous drain current <sup>e</sup>	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	6.2	A	
		T <sub>C</sub> = 100 °C	3.9		
Pulsed drain current <sup>a, e</sup>	I <sub>DM</sub>		25		
Linear derating factor			1.0	W/°C	
Single pulse avalanche energy <sup>b</sup>	E <sub>AS</sub>		570	mJ	
Repetitive avalanche current <sup>a</sup>	I <sub>AR</sub>		6.2	A	
Repetitive avalanche energy <sup>a</sup>	E <sub>AR</sub>		13	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	125	W
Peak diode recovery dV/dt <sup>c, e</sup>	dV/dt		6.0	V/ns	
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>		-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	for 10 s		300		

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting T<sub>J</sub> = 25 °C, L = 29.6 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 6.2 A (see fig. 12)
- I<sub>SD</sub> ≤ 6.2 A, dI/dt ≤ 88 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C
- 1.6 mm from case
- Uses IRFBC40A, SiHFBC40A data and test conditions



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	40	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$	-	0.66	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3.7\text{ A}^b$	-	-	1.2	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 3.7\text{ A}$	3.4	-	-	S
<b>Dynamic</b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	1036	-	pF
Output capacitance	$C_{oss}$		-	136	-	
Reverse transfer capacitance	$C_{rss}$		-	7.0	-	
Output capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	1487	-
			$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	36	-
Output capacitance effective	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	48	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 6.2\text{ A}, V_{DS} = 480\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	42	nC
Gate-source charge	$Q_{gs}$		-	-	10	
Gate-drain charge	$Q_{gd}$		-	-	20	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 6.2\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 47\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	13	-	ns
Rise time	$t_r$		-	23	-	
Turn-off delay time	$t_{d(off)}$		-	31	-	
Fall time	$t_f$		-	18	-	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$ , open drain	0.6	-	3.9	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	6.2	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$		-	-	25	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 6.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 6.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	431	647	ns
Body diode reverse recovery charge	$Q_{rr}$		-	1.8	2.8	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$
- c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$
- d. Uses IRHFBC40A, SiHFBC40A data and test conditions



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

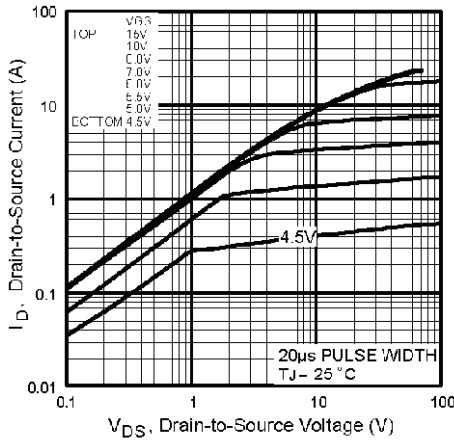


Fig. 1 - Typical Output Characteristics

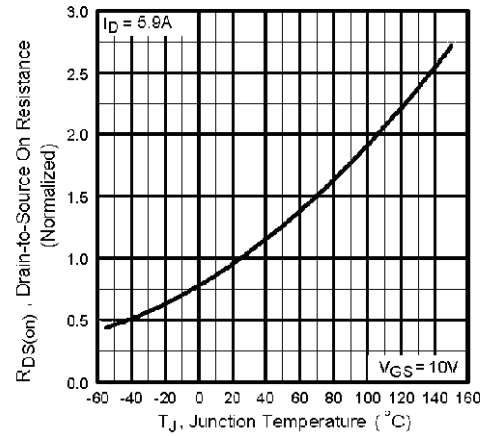


Fig. 4 - Normalized On-Resistance vs. Temperature

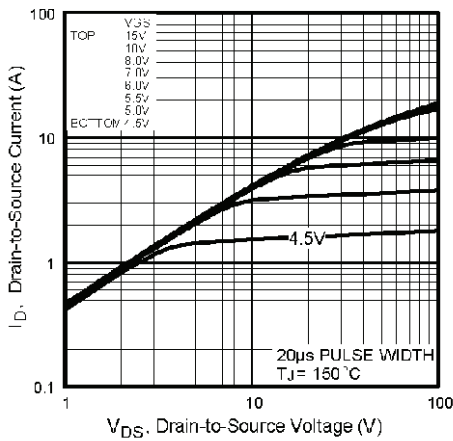


Fig. 2 - Typical Output Characteristics

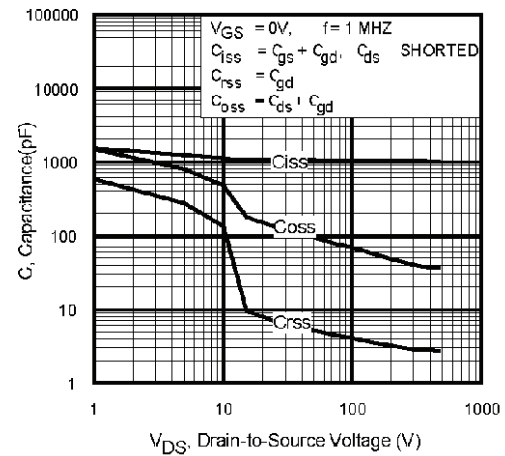


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

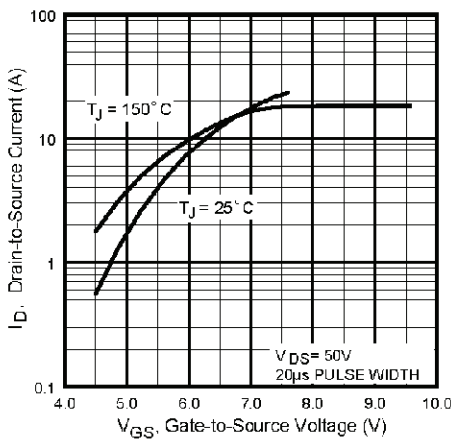


Fig. 3 - Typical Transfer Characteristics

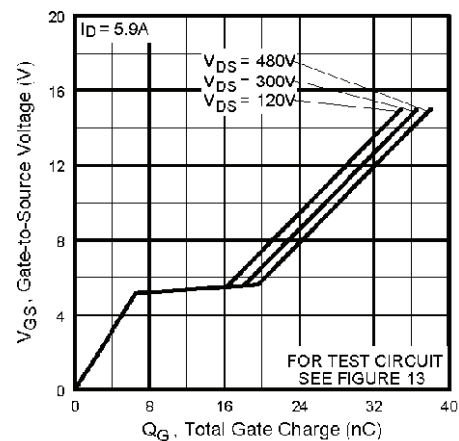


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

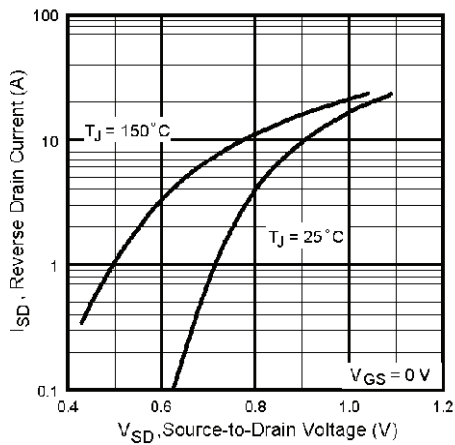


Fig. 7 - Typical Source-Drain Diode Forward Voltage

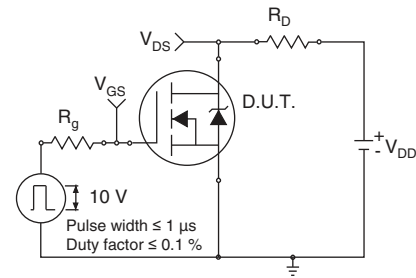


Fig. 10a - Switching Time Test Circuit

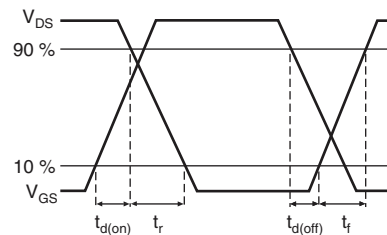


Fig. 10b - Switching Time Waveforms

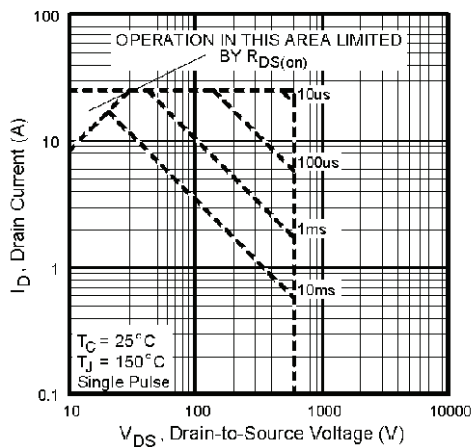


Fig. 8 - Maximum Safe Operating Area

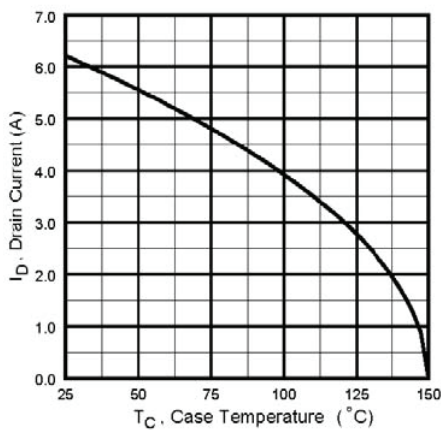


Fig. 9 - Maximum Drain Current vs. Case Temperature

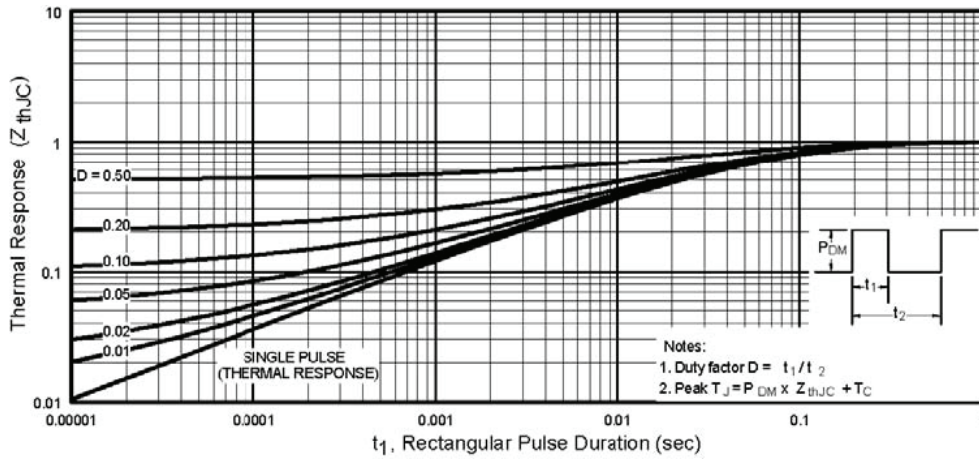


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

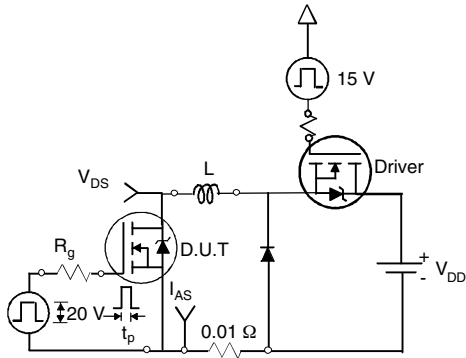


Fig. 12a - Unclamped Inductive Test Circuit

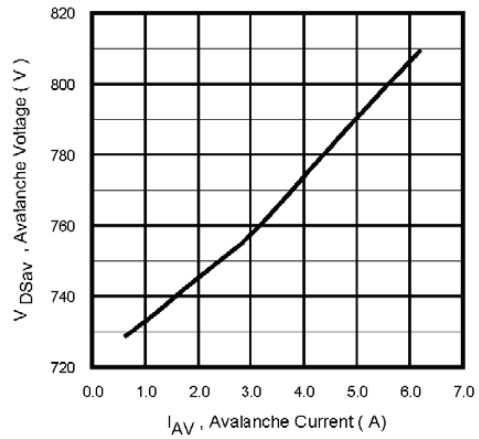


Fig. 12d - Maximum Avalanche Energy vs. Drain Current

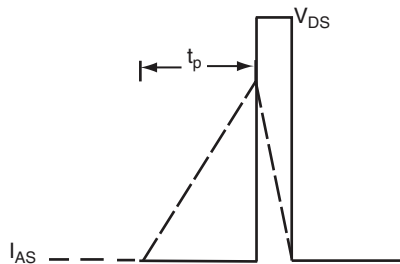


Fig. 12b - Unclamped Inductive Waveforms

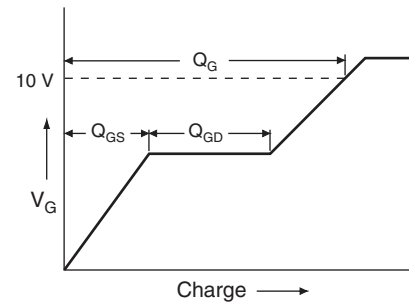


Fig. 13a - Basic Gate Charge Waveform

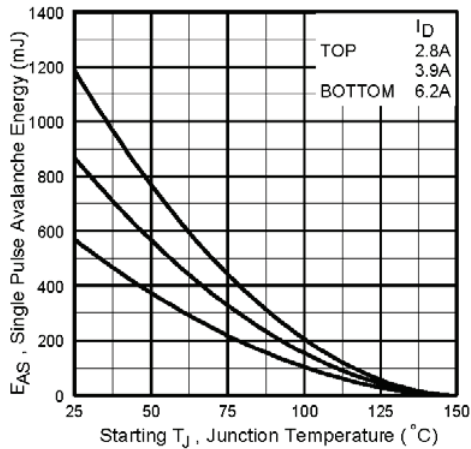


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

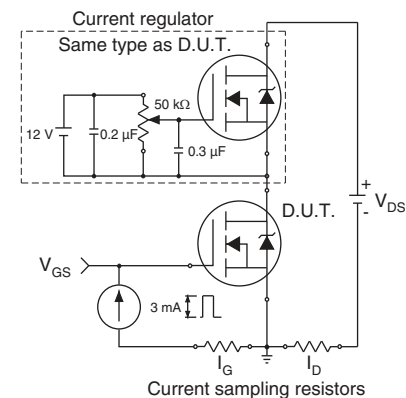
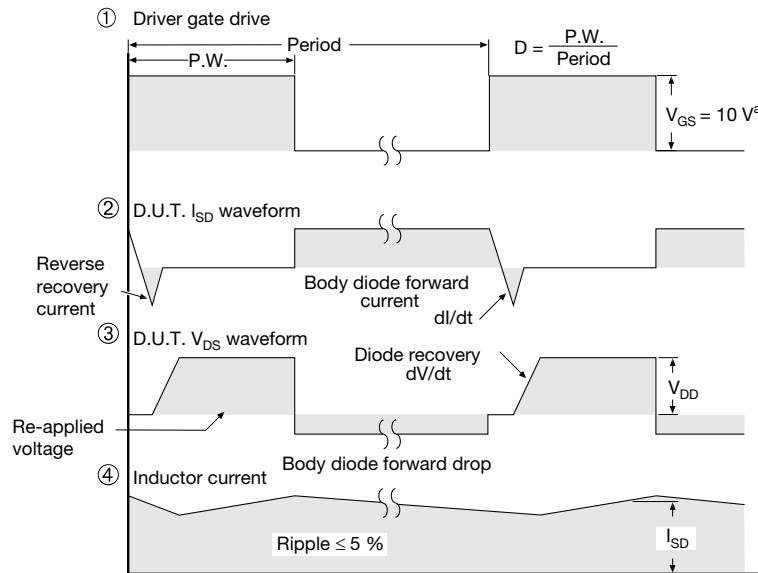
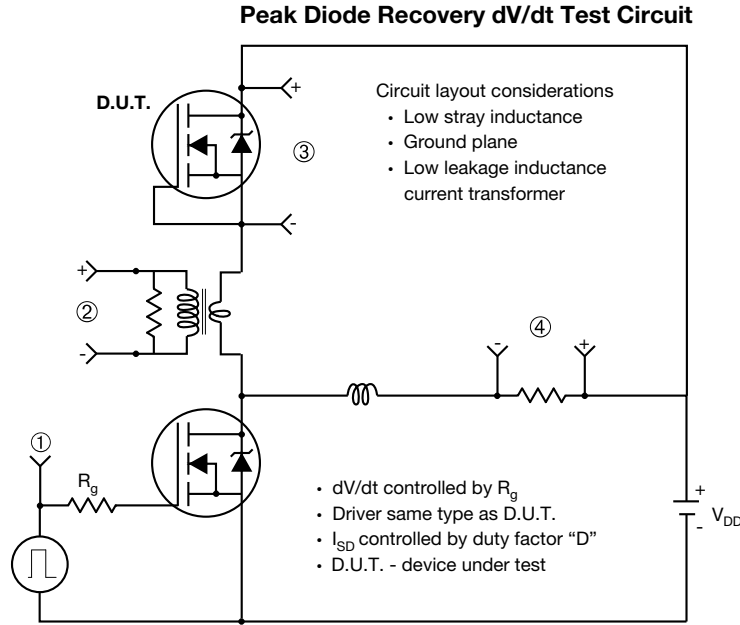


Fig. 13b - Gate Charge Test Circuit



**Note**  
 a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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### TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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