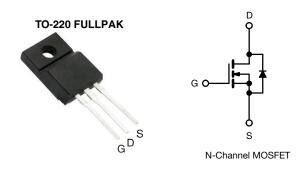
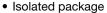
Vishay Siliconix

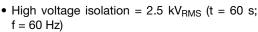
Power MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	100				
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V 0.27				
Q _g max. (nC)	16				
Q _{gs} (nC)	4.4				
Q _{gd} (nC)	7.7				
Configuration	Single				

FEATURES







• Sink to lead creepage distance = 4.8 mm

- 175 °C operating temperature
- Dynamic dV/dt rating
- Low thermal resistance
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI520GPbF

ABSOLUTE MAXIMUM RATINGS (T _C	•				
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	100	V
Gate-source voltage			V_{GS}	± 20	V
Continuous drain current	V at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	I-	7.2	
Continuous drain current $V_{GS} \text{ at 10 V} \frac{T_C = 200 \text{ °C}}{T_C = 100 \text{ °C}}$			ID	5.1	Α
Pulsed drain current ^a			I _{DM}	29	
Linear derating factor				0.24	W/°C
Single pulse avalanche energy b			E _{AS}	36	mJ
Repetitive avalanche current ^a			I _{AR}	7.2	А
Repetitive avalanche energy ^a			E _{AR}	3.7	mJ
Maximum power dissipation $T_C = 25 ^{\circ}C$			P _D	37	W
Peak diode recovery dV/dt ^c			dV/dt	5.5	V/ns
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +175	
Soldering recommendations (peak temperature) ^d	For	10 s		300	°C
Mounting torque	M3 s	screw		0.6	Nm

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 25 V, starting T_J = 25 °C, L = 1.0 mH, R_q = 25 Ω , I_{AS} = 7.2 A (see fig. 12)
- c. $I_{SD} \le 9.2 \text{ A}$, $dI/dt \le 110 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_{J} \le 175 \text{ °C}$
- d. 1.6 mm from case



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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	4.1	C/ VV

PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT
Static							
Drain-ssource breakdown voltage	V_{DS}	V _{GS} =	= 0 V, I _D = 250 μA	100	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = 1 mA	-	0.13	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	,	V _{GS} = ± 20 V	-	-	± 100	nA
Zoro goto voltago droin ourrent	1	V _{DS} =	= 100 V, V _{GS} = 0 V	-	-	25	
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 80 \text{ V}$	V _{GS} = 0 V, T _J = 150 °C	-	-	250	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.3 A ^b	-	-	0.27	Ω
Forward transconductance	9 _{fs}	V _{DS} =	50 V, I _D = 4.3 A ^b	2.3	-	-	S
Dynamic							
Input capacitance	C _{iss}		$V_{GS} = 0 V$	-	360	-	
Output capacitance	C _{oss}		$V_{DS} = 25 \text{ V},$	-	150	-	рF
Reverse transfer capacitance	C _{rss}	f = 1.	.0 MHz, see fig. 5	-	34	-	PΓ
Drain to sink capacitance	С		f = 1.0 MHz	-	12	-	
Total gate charge	Qg			-	-	16	
Gate-source charge	Q_{gs}	$V_{GS} = 10 \text{ V}$	$I_D = 9.2 \text{ A}, V_{DS} = 80 \text{ V},$ see fig. 6 and 13 b	-	-	4.4	nC
Gate-drain charge	Q_{gd}		occ lig. o and ro	-	-	7.7	
Turn-on delay time	t _{d(on)}			-	8.8	-	
Rise time	t _r		, 5	-	30	-	
Turn-off delay time	t _{d(off)}	$R_g =$		-	19	-	ns
Fall time	t _f	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		-			
Gate input resistance	R _g	f = 1	MHz, open drain	0.4	-	2.1	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from		-	4.5	-	
Internal source inductance	L _S	package and die cont		-	7.5	-	nH
Drain-Source Body Diode Characteristic	cs					•	,
Continuous source-drain diode current	I _S	MOSFET sym showing the		-	=	7.2	Α
Pulsed diode forward current ^a	I _{SM}	integral reverse p - n junction diode		-	-	29	
Body diode voltage	V _{SD}	T _J = 25 °C	$I_{S} = 7.2 \text{ A}, V_{GS} = 0 \text{ V}^{\text{ b}}$	-	-	2.5	V
Body diode reverse recovery time	t _{rr}	T. = 25 °C 1	- 0.2 A dl/dt - 100 A/vob	=	130	260	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 9.2 \text{A}, dI/dt = 100 \text{A/}\mu\text{s}^{\text{b}}$		-	0.65	1.3	μC
Forward turn-on time	t _{on}	Intrinsic tu	rn-on time is negligible (turn	-on is dor	ninated b	y L _S and	L _D)

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%$



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

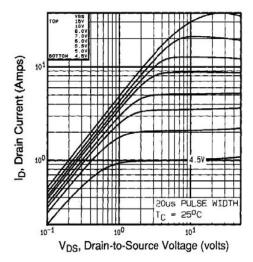


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

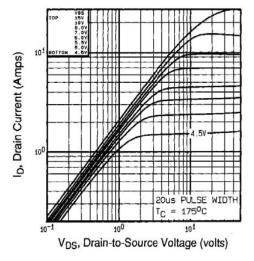


Fig. 2 - Typical Output Characteristics, $T_C = 175$ °C

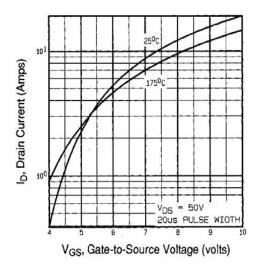


Fig. 3 - Typical Transfer Characteristics

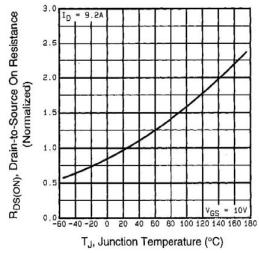


Fig. 4 - Normalized On-Resistance vs. Temperature



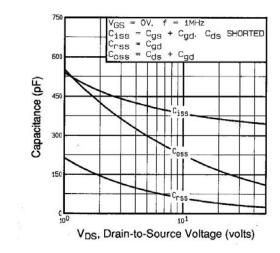


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

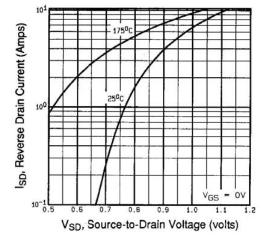


Fig. 7 - Typical Source-Drain Diode Forward Voltage

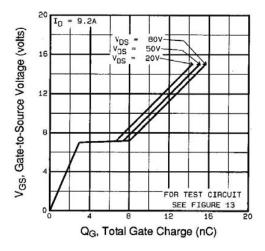


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

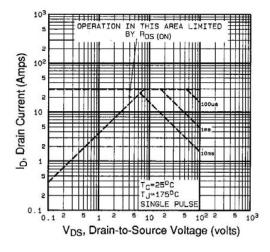


Fig. 8 - Maximum Safe Operating Area



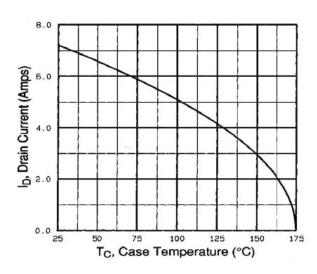


Fig. 9 - Maximum Drain Current vs. Case Temperature

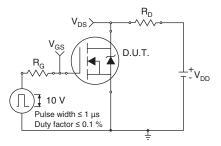


Fig. 10a - Switching Time Test Circuit

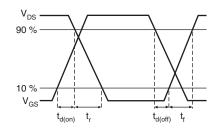


Fig. 10b - Switching Time Waveforms

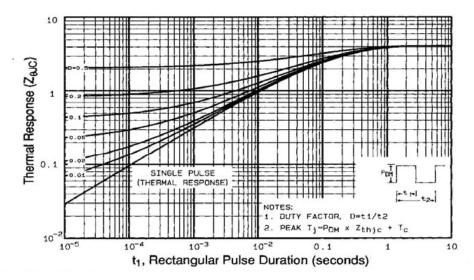


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

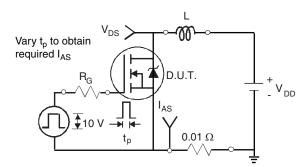


Fig. 12a - Unclamped Inductive Test Circuit

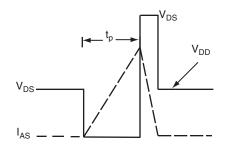


Fig. 12b - Unclamped Inductive Waveforms



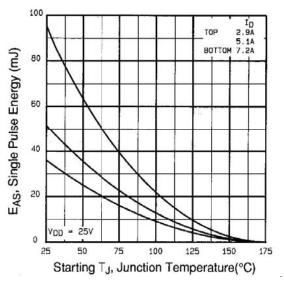


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

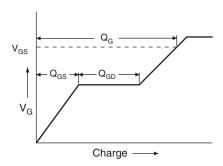


Fig. 13a - Basic Gate Charge Waveform

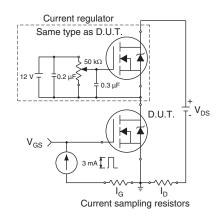
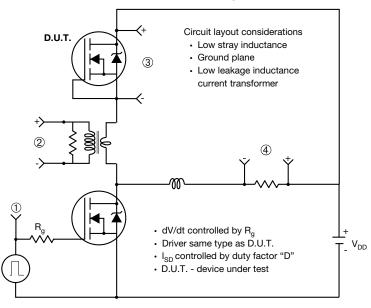


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



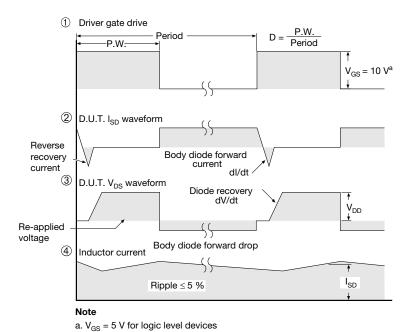


Fig. 14 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



	MILLIMETERS		
DIM.	MIN.	NOM.	MAX.
Α	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
С	0.45	0.50	0.63
D	15.80	15.87	15.97
е		2.54 BSC	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
ØR	3.08	3.18	3.28

- 1. To be used only for process drawing
- 2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
- 3. All critical dimensions should C meet $C_{pk} > 1.33$
- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
- 6. Facility code will be the 1st character located at the 2nd row of the unit marking



OPTION 2: FACILITY CODE = Y



	MILLIMETERS		INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.570	4.830	0.180	0.190	
A1	2.570	2.830	0.101	0.111	
A2	2.510	2.850	0.099	0.112	
b	0.622	0.890	0.024	0.035	
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
С	0.440	0.629	0.017	0.025	
D	8.650	9.800	0.341	0.386	
d1	15.88	16.120	0.622	0.635	
d3	12.300	12.920	0.484	0.509	
Е	10.360	10.630	0.408	0.419	
е	2.54	BSC	0.100 BSC		
L	13.200	13.730	0.520	0.541	
L1	3.100	3.500	0.122	0.138	
n	6.050	6.150	0.238	0.242	
ØΡ	3.050	3.450	0.120	0.136	
u	2.400	2.500	0.094	0.098	
V	0.400	0.500	0.016	0.020	

ECN: E19-0180-Rev. D, 08-Apr-2019

DWG: 5972

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- 2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
- 3. All critical dimensions should C meet $C_{pk} > 1.33$
- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
- 6. Facility code will be the 1st character located at the 2nd row of the unit marking



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Vishay

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