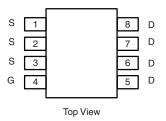


P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)			
	0.00875 at V <sub>GS</sub> = - 4.5 V	- 14			
- 20	0.01075 at V <sub>GS</sub> = - 2.5 V	- 12			
	0.0135 at V <sub>GS</sub> = - 1.8 V	- 11			





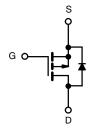


- Halogen-free Option Available
- TrenchFET<sup>®</sup> Power MOSFET

#### **APPLICATIONS**

Game Station
Load Switch





P-Channel MOSFET

Ordering Information: Si4421DY-T1-E3 (Lead (Pb)-free) Si4421DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_A = 25 \text{ °C}$ , unless otherwise noted						
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	- 20		V	
Gate-Source Voltage		V <sub>GS</sub>	± 8			
Continuous Drain Current (T <sub>.I</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	– I <sub>D</sub>	- 14	- 10		
Continuous Drain Current $(T_j = 150^{\circ} C)$	T <sub>A</sub> = 70 °C		- 11.5	- 8	А	
Pulsed Drain Current		I <sub>DM</sub>	- 40		A	
Continuous Source Current (Diode Conduction) <sup>a</sup>		۱ <sub>S</sub>	- 2.7	- 1.36		
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.0	1.5	W	
Maximum Fower Dissipation	T <sub>A</sub> = 70 °C		1.9	0.95	vv	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mauinum lunction to Anchienta	t ≤ 10 s	R <sub>thJA</sub>	33	42	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		70	85	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	16	21	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•			
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -850 \ \mu A$	- 0.4		- 0.8	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 8 V$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70 \text{ °C}$			- 1	μΑ	
					- 10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 V, V_{GS} = -4.5 V$	- 30			Α	
		$V_{GS}$ = - 4.5 V, $I_D$ = - 14 A		0.007	0.00875		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 12 A		0.0085	0.01075	Ω	
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 11 A		0.011	0.0135		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = -10 \text{ V}, \text{ I}_{D} = -14 \text{ A}$		55		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{\rm S}$ = - 2.7 A, $V_{\rm GS}$ = 0 V		- 0.6	- 1.1	V	
Dynamic <sup>b</sup>					•		
Total Gate Charge	Qg			82	125		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = - 10 V, $V_{GS}$ = - 4.5 V, $I_{D}$ = - 14 A		10		nC	
Gate-Drain Charge	Q <sub>gd</sub>			27			
Gate Resistance	Rg			3		Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			45	70		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 10 $\Omega$		90	140	ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_{\text{D}}\cong$ - 1 A, $\text{V}_{\text{GEN}}$ = - 4.5 V, $\text{R}_{\text{G}}$ = 6 $\Omega$		350	550		
Fall Time	t <sub>f</sub>			170	260	113	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 2.1 A, dl/dt = 100 A/μs		135	210		

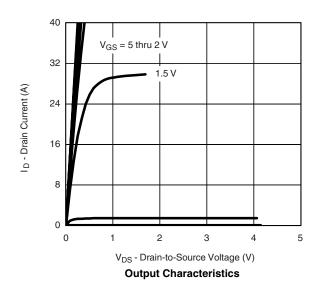
Notes:

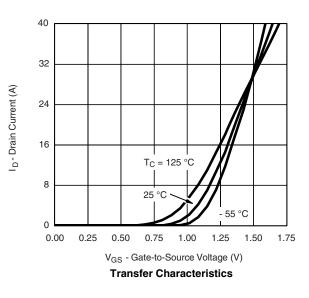
a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



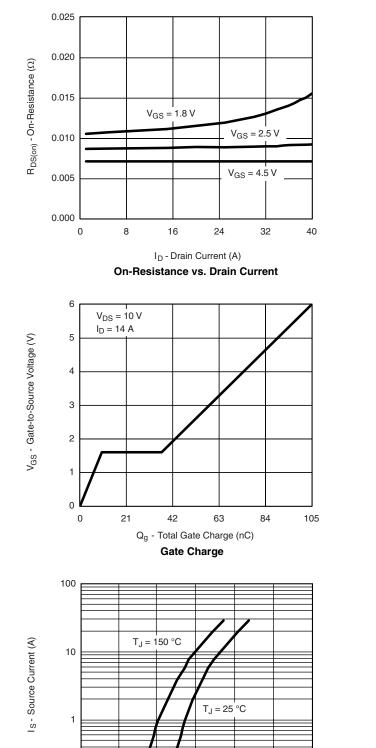


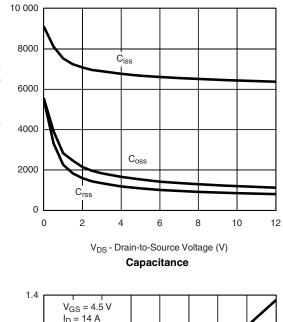
Si4421DY

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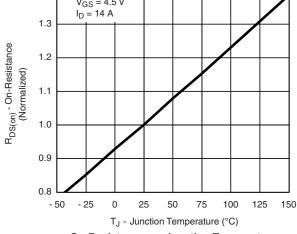
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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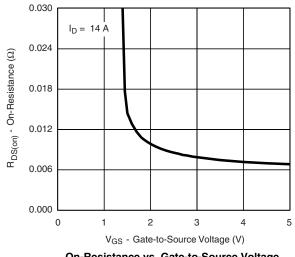




C - Capacitance (pF)



**On-Resistance vs. Junction Temperature** 



On-Resistance vs. Gate-to-Source Voltage

0.1

0.0

0.2

0.4

0.6

V<sub>SD</sub> - Source-to-Drain Voltage (V) Source-Drain Diode Forward Voltage

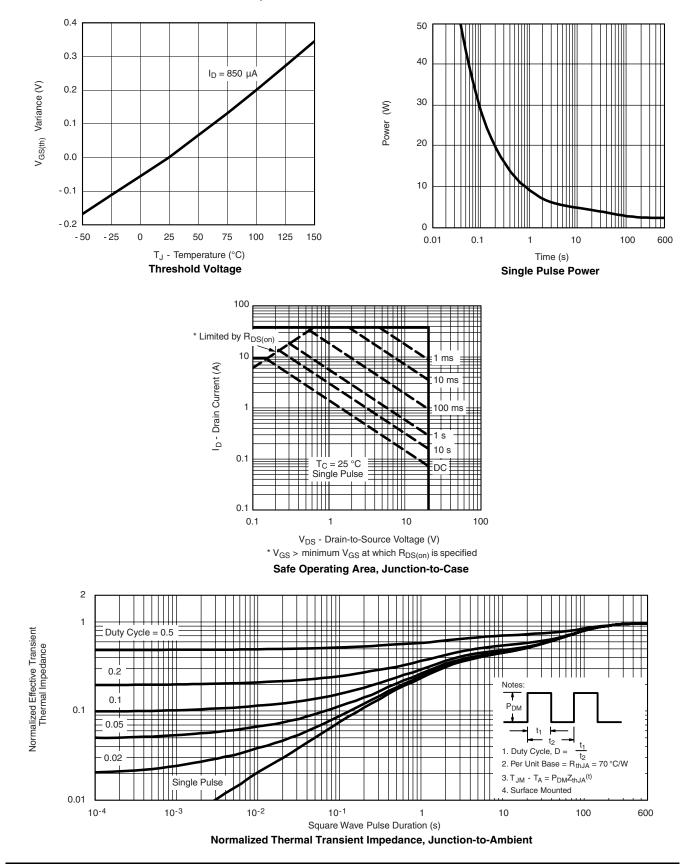
0.8

1.0

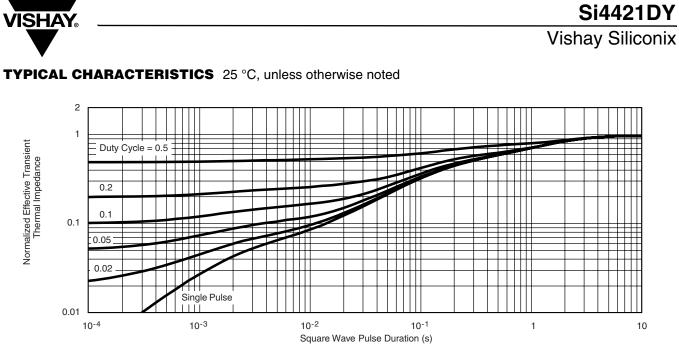
1.2

### Vishay Siliconix





VISHA`



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72114.



# Package Information

Vishay Siliconix

# SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES			
DIM	Min	Мах	Min	Max		
A	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						

## **Application Note 826**

Vishay Siliconix



**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)

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