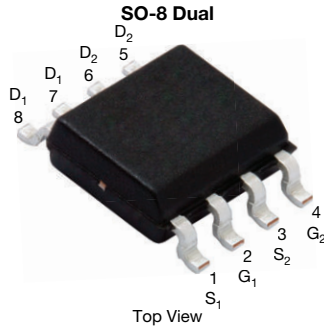


N- and P-Channel 60 V (D-S) MOSFET



FEATURES

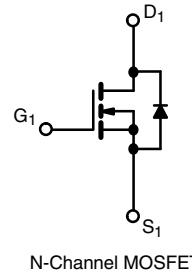
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



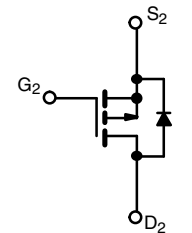
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- CCFL Inverter



N-Channel MOSFET



P-Channel MOSFET

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V _{DS} (V)	60	-60
R _{DS(on)} (Ω) at V _{GS} = ± 10 V	0.058	0.120
R _{DS(on)} (Ω) at V _{GS} = ± 4.5 V	0.072	0.150
Q _g typ. (nC)	6	8
I _D (A) ^a	5.3	-3.9
Configuration	N- and p-pair	

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free	Si4559ADY-T1-E3
Lead (Pb)-free and halogen-free	Si4559ADY-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT	
Drain-source voltage	V _{DS}	60	-60	V	
Gate-source voltage	V _{GS}	± 20	± 20		
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	5.3	-3.9	A
		T _C = 70 °C	4.3	-3.2	
		T _A = 25 °C	4.3 ^{b, c}	-3 ^{b, c}	
		T _A = 70 °C	3.4 ^{b, c}	-2.4 ^{b, c}	
Pulsed drain current (10 μs pulse width)	I _{DM}	20	-25	A	
Source drain current diode current	I _S	T _C = 25 °C	2.6		-2.8
		T _A = 25 °C	1.7 ^{b, c}	-1.7 ^{b, c}	
Pulsed source-drain current	I _{SM}	20	-25	mJ	
Single pulse avalanche current	I _{AS}	11	15		
Single pulse avalanche energy	E _{AS}	6.1	11	W	
Maximum power dissipation	P _D	T _C = 25 °C	3.1		3.4
		T _C = 70 °C	2		2.2
		T _A = 25 °C	2 ^{b, c}		2 ^{b, c}
		T _A = 70 °C	1.3 ^{b, c}	1.3 ^{b, c}	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150		°C	

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient ^{b, d}	t ≤ 10 s	R _{thJA}	55	62.5	53	62.5	°C/W
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	33	40	30	37	

Notes

- Based on T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- Maximum under steady state conditions is 110 °C/W for N-channel and P-channel



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT			
Static									
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	60	-	-	V		
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-60	-	-			
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch	-	55	-	mV		
		I _D = -250 μA	P-Ch	-	-50	-			
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch	-	-6	-			
		I _D = -250 μA	P-Ch	-	4	-			
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1	-	3	V		
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1	-	-3			
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch	-	-	100	nA		
			P-Ch	-	-	-100			
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	N-Ch	-	-	1	μA		
			P-Ch	-	-	-1			
			N-Ch	-	-	10			
			P-Ch	-	-	-10			
On-state drain current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	20	-	-	A		
		V _{DS} ≤ -5 V, V _{GS} = -10 V	P-Ch	-25	-	-			
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.3 A	N-Ch	-	0.046	0.058	Ω		
			P-Ch	-	0.100	0.120			
			N-Ch	-	0.059	0.072			
			P-Ch	-	0.126	0.150			
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 4.3 A	N-Ch	-	15	-	S		
		V _{DS} = -15 V, I _D = -3.1 A	P-Ch	-	8.5	-			
Dynamic^a									
Input capacitance	C _{iss}	N-Channel V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	-	665	-	pF		
			P-Ch	-	650	-			
Output capacitance	C _{oss}		N-Ch	-	75	-			
			P-Ch	-	95	-			
Reverse transfer capacitance	C _{rss}		N-Ch	-	40	-			
			P-Ch	-	60	-			
Total gate charge	Q _g		V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.3 A V _{DS} = -30 V, V _{GS} = -10 V, I _D = -3.1 A	N-Ch	-	13		20	nC
				P-Ch	-	14.5		22	
		N-Ch		-	6	9			
		P-Ch		-	8	12			
Gate-source charge	Q _{gs}	N-Channel V _{DS} = 30 V, V _{GS} = 4.5 V, I _D = 4.3 A P-Channel V _{DS} = -30 V, V _{GS} = -4.5 V, I _D = -3.1 A	N-Ch	-	2.3	-			
			P-Ch	-	2.2	-			
Gate-drain charge	Q _{gd}		N-Ch	-	2.6	-			
			P-Ch	-	3.7	-			
Gate resistance	R _g	f = 1 MHz	N-Ch	-	2	3	Ω		
			P-Ch	-	14	20			



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT	
Dynamic ^a							
Turn-on delay time	$t_{d(on)}$	N-Channel $V_{DD} = 30\text{ V}$, $R_L = 8.8\ \Omega$ $I_D \cong 3.4\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch	-	15	25	ns
			P-Ch	-	30	45	
Rise time	t_r	P-Channel $V_{DD} = -30\text{ V}$, $R_L = 12.5\ \Omega$ $I_D \cong -2.4\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch	-	65	100	
			P-Ch	-	70	105	
Turn-off delay time	$t_{d(off)}$	N-Channel $V_{DD} = 30\text{ V}$, $R_L = 8.8\ \Omega$ $I_D \cong 3.4\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	N-Ch	-	15	25	
			P-Ch	-	40	60	
Fall time	t_f	P-Channel $V_{DD} = -30\text{ V}$, $R_L = 12.5\ \Omega$ $I_D \cong -2.4\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\ \Omega$	N-Ch	-	10	15	
			P-Ch	-	30	45	
Turn-on delay time	$t_{d(on)}$	N-Channel $V_{DD} = 30\text{ V}$, $R_L = 8.8\ \Omega$ $I_D \cong 3.4\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	N-Ch	-	10	15	
			P-Ch	-	10	15	
Rise time	t_r	P-Channel $V_{DD} = -30\text{ V}$, $R_L = 12.5\ \Omega$ $I_D \cong -2.4\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\ \Omega$	N-Ch	-	15	25	
			P-Ch	-	13	20	
Turn-off delay time	$t_{d(off)}$	N-Channel $V_{DD} = 30\text{ V}$, $R_L = 8.8\ \Omega$ $I_D \cong 3.4\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	N-Ch	-	20	30	
			P-Ch	-	35	55	
Fall time	t_f	P-Channel $V_{DD} = -30\text{ V}$, $R_L = 12.5\ \Omega$ $I_D \cong -2.4\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\ \Omega$	N-Ch	-	10	15	
			P-Ch	-	30	45	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch	-	-	2.6	A
			P-Ch	-	-	-2.8	
Pulse diode forward current ^a	I_{SM}		N-Ch	-	-	20	A
			P-Ch	-	-	-25	
Body diode voltage	V_{SD}	$I_S = 1.7\text{ A}$	N-Ch	-	0.8	1.2	V
		$I_S = -2\text{ A}$	P-Ch	-	-0.8	-1.2	
Body diode reverse recovery time	t_{rr}	N-Channel $I_F = 1.7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch	-	30	60	ns
			P-Ch	-	30	50	
Body diode reverse recovery charge	Q_{rr}	P-Channel $I_F = -2\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch	-	32	50	nC
			P-Ch	-	35	60	
Reverse recovery fall time	t_a	N-Channel $I_F = 1.7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch	-	25	-	ns
			P-Ch	-	16	-	
Reverse recovery rise time	t_b	P-Channel $I_F = -2\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch	-	5	-	
			P-Ch	-	14	-	

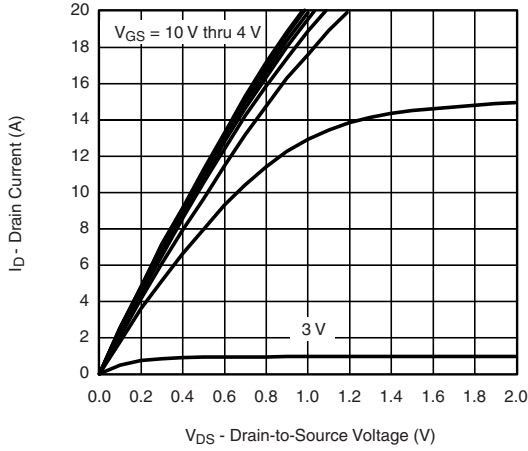
Notes

- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

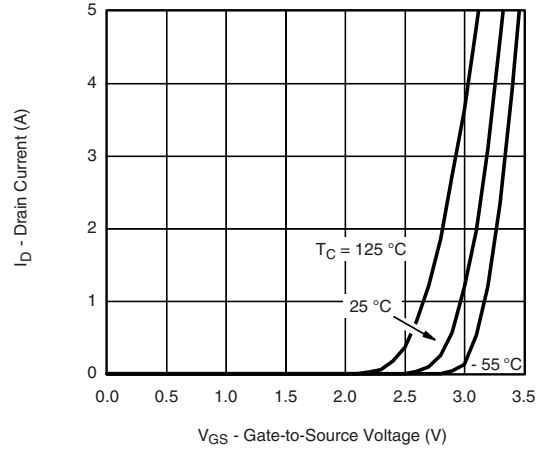
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



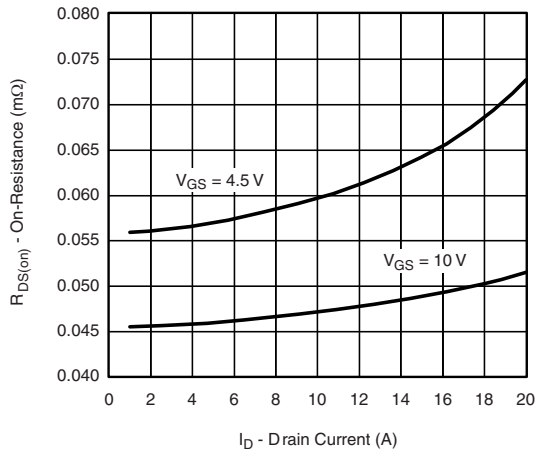
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



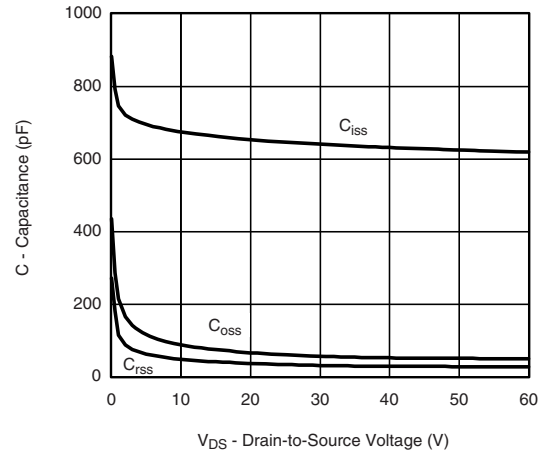
Output Characteristics



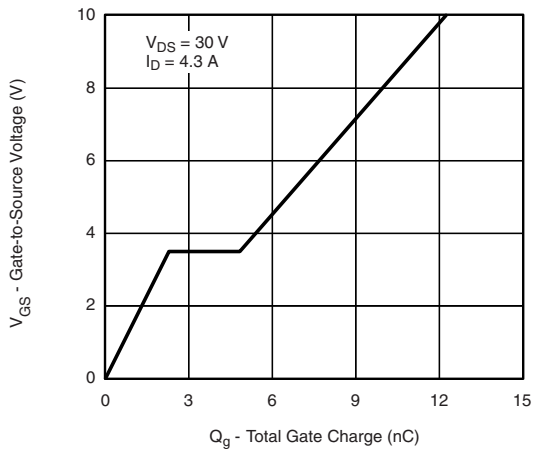
Transfer Characteristics



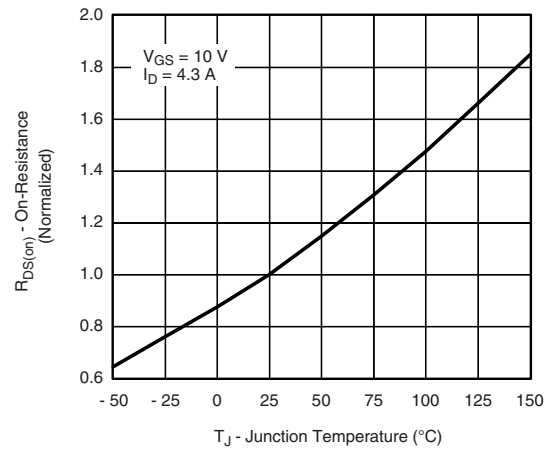
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



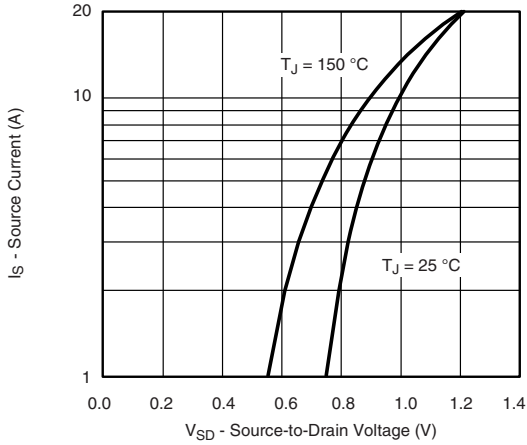
Gate Charge



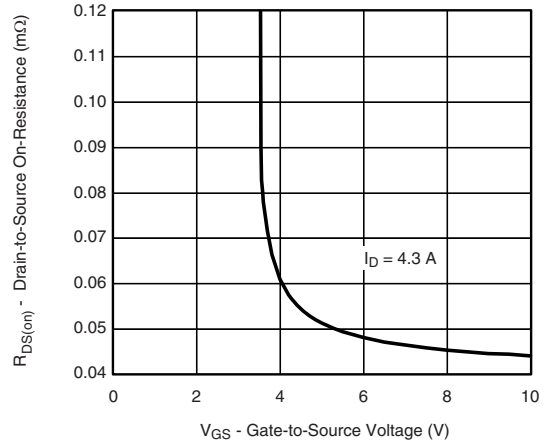
On-Resistance vs. Junction Temperature



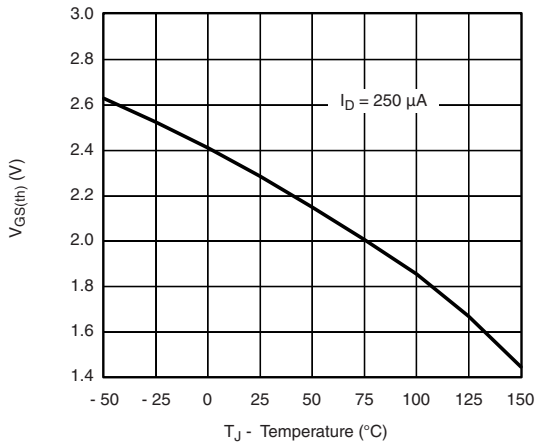
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



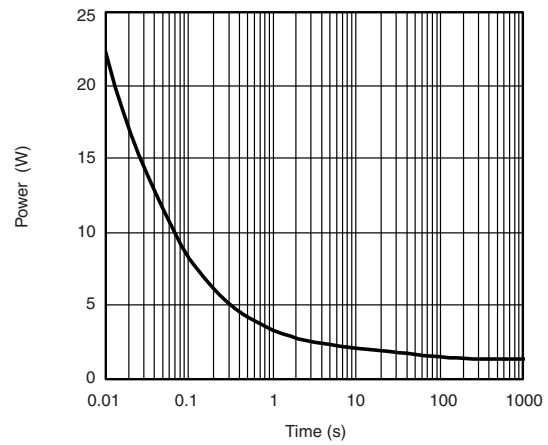
Source-Drain Diode Forward Voltage



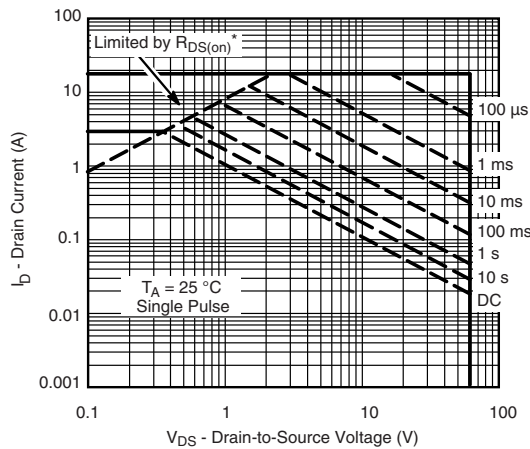
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

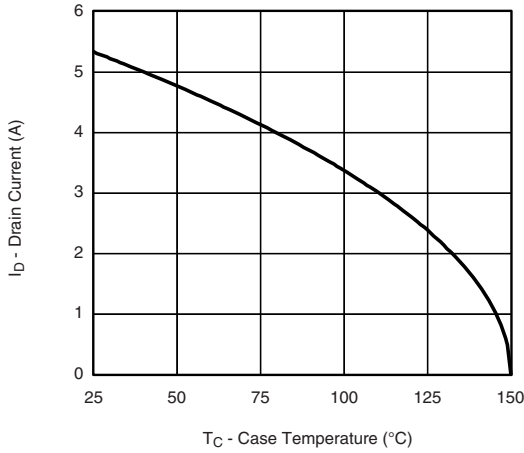


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

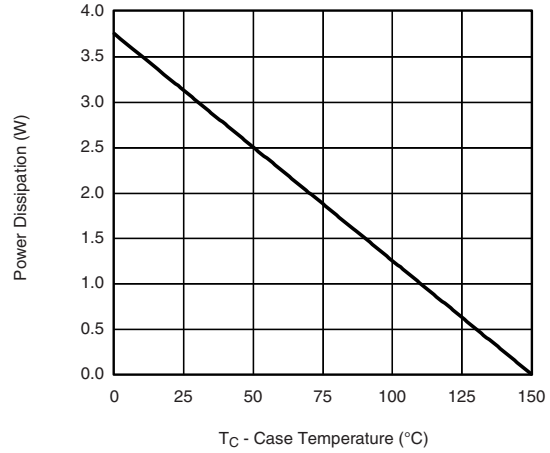
Safe Operating Area



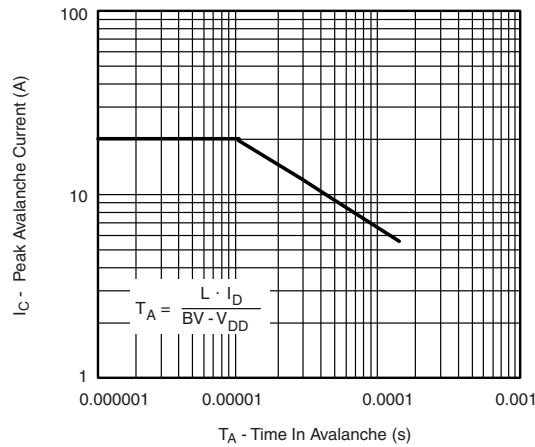
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power Derating



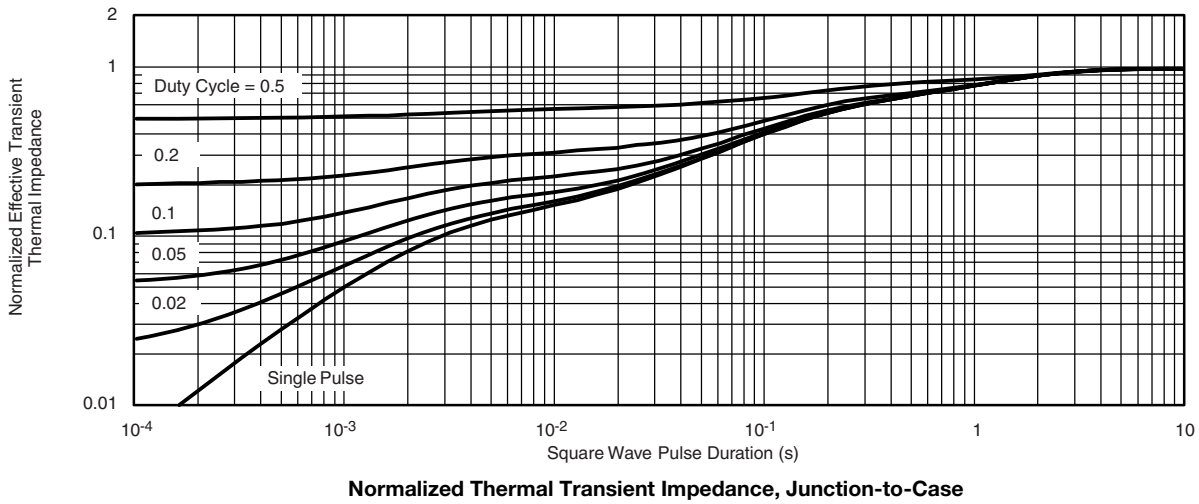
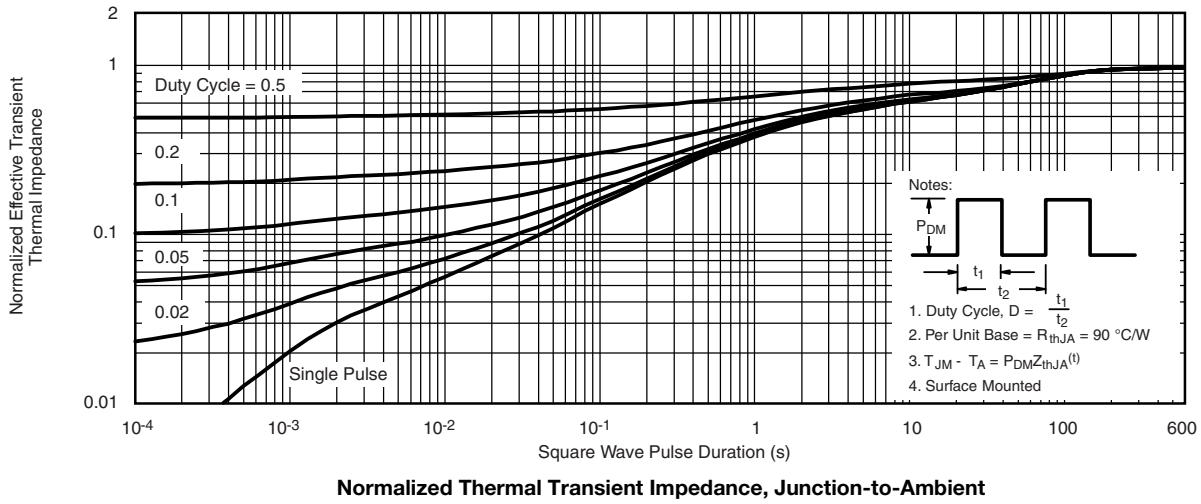
Single Pulse Avalanche Capability

Note

- a. The power dissipation P_D is based on T_J max = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

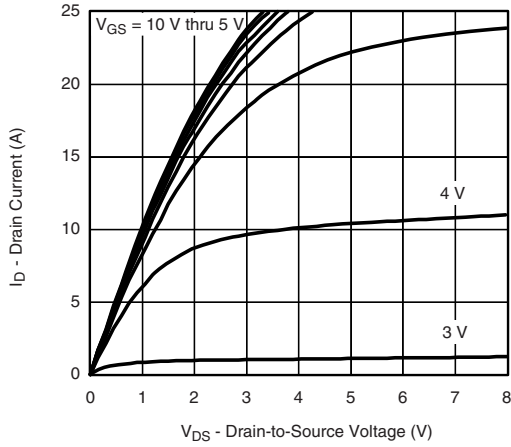


N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

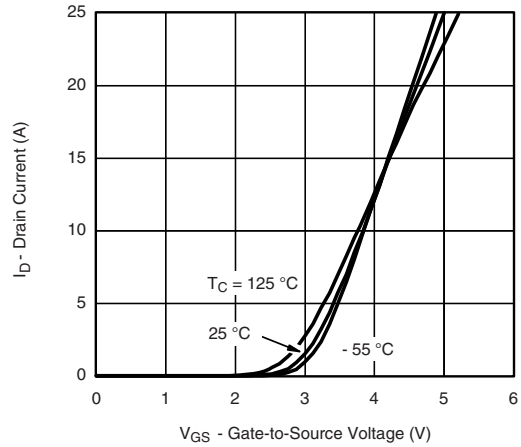




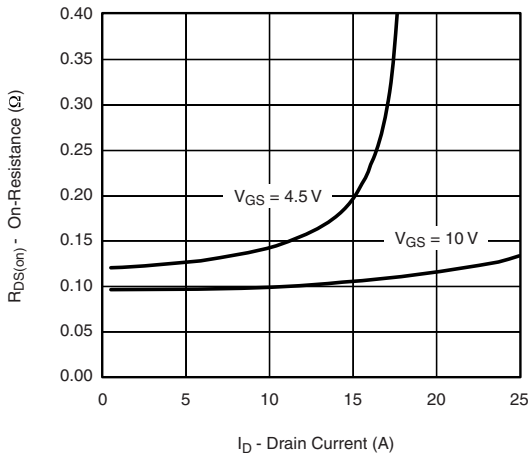
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



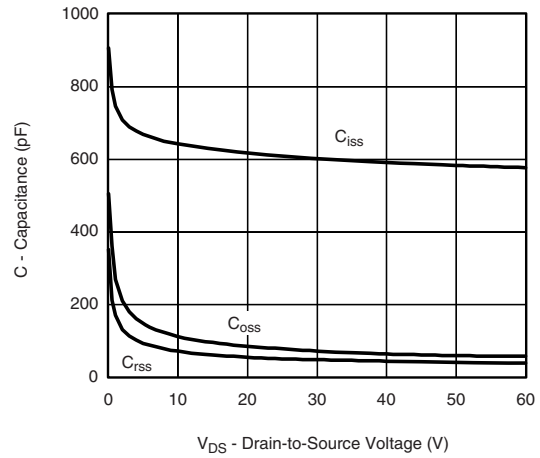
Output Characteristics



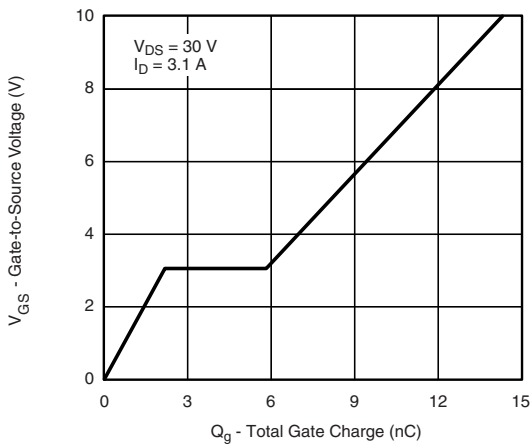
Transfer Characteristics



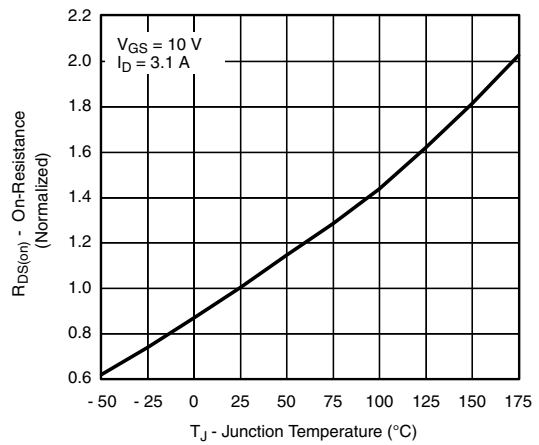
On-Resistance vs. Drain Current



Capacitance



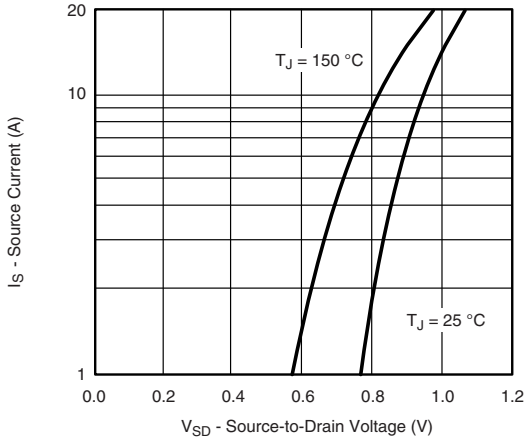
Gate Charge



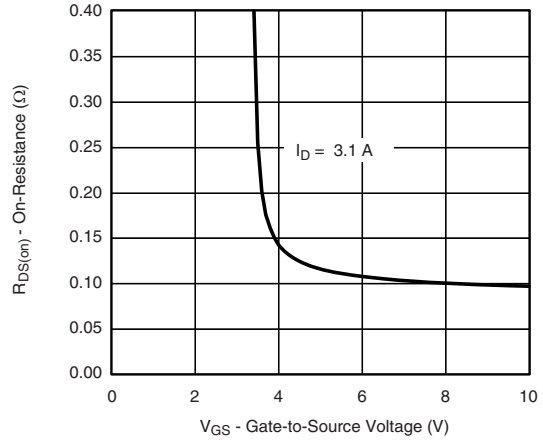
On-Resistance vs. Junction Temperature



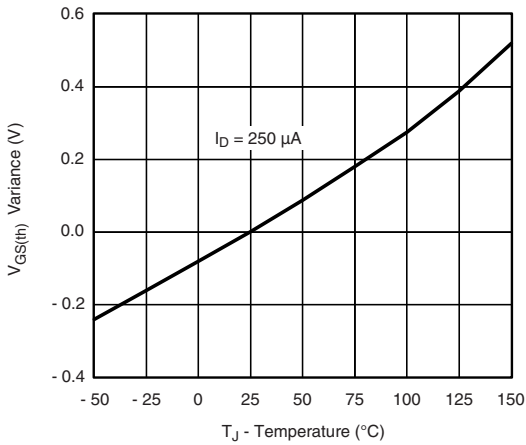
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



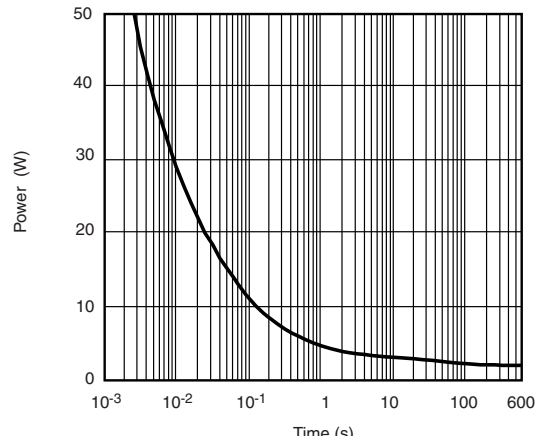
Source-Drain Diode Forward Voltage



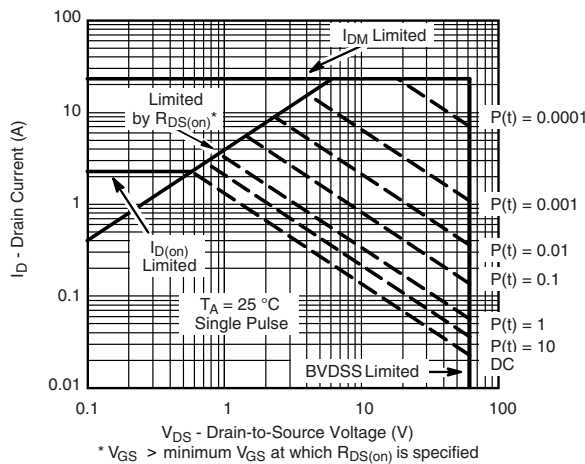
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



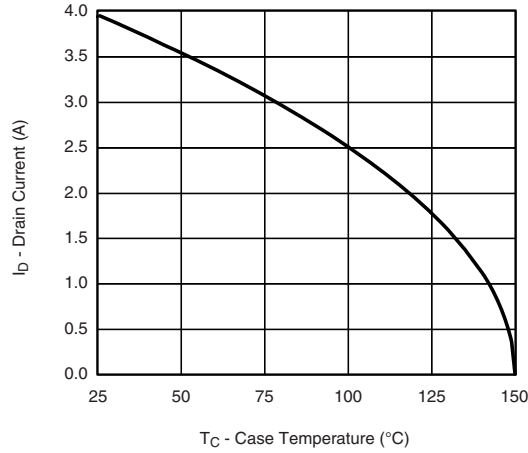
Single Pulse Power



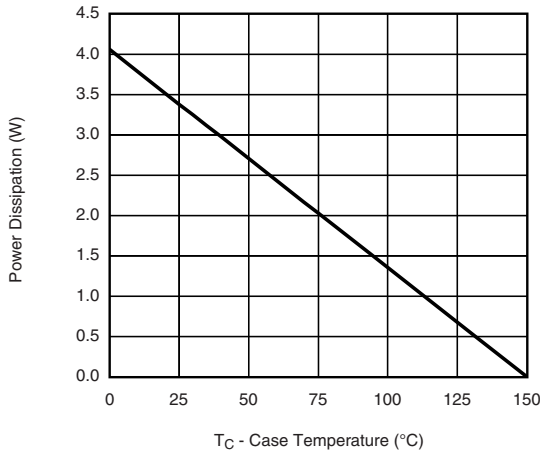
Safe Operating Area, Junction-to-Case



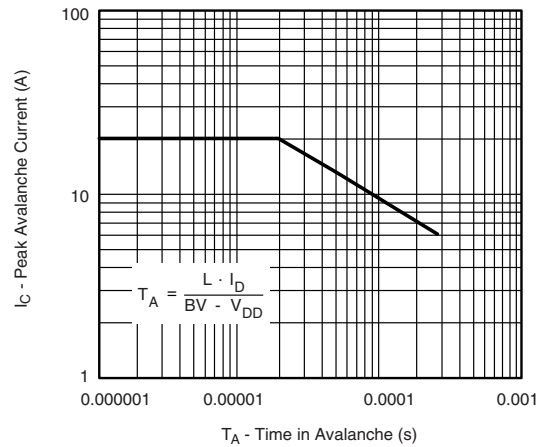
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power Derating, Junction-to-Foot



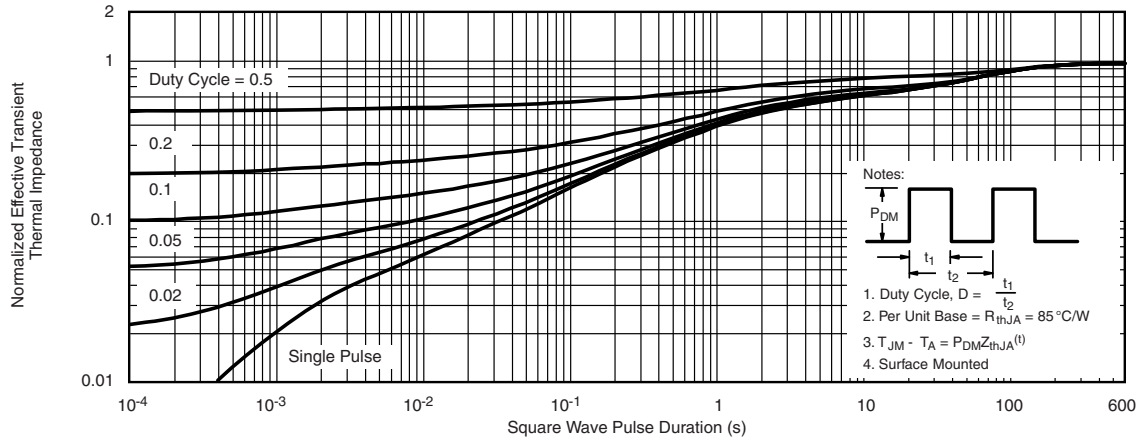
Single Pulse Avalanche Capability

Note

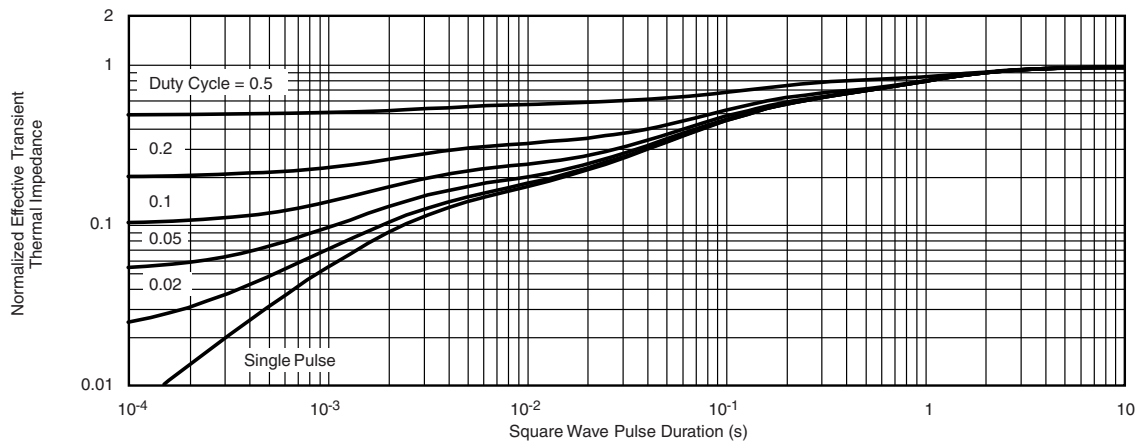
- a. The power dissipation P_D is based on T_J max = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



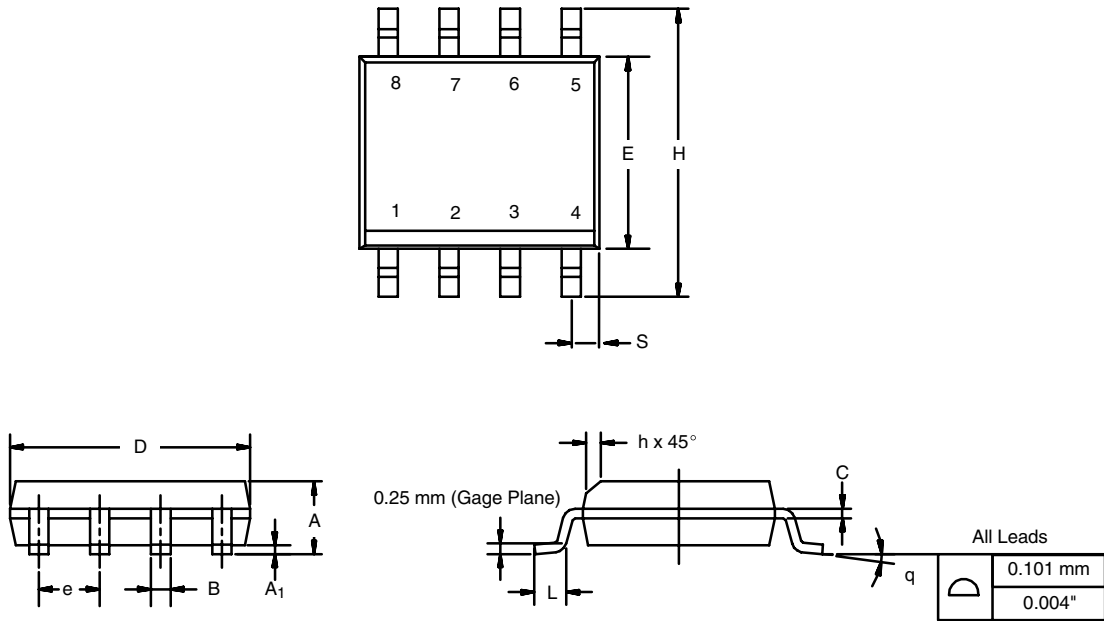
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73624.



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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