

## Dual N-Channel 30-V (D-S) MOSFET

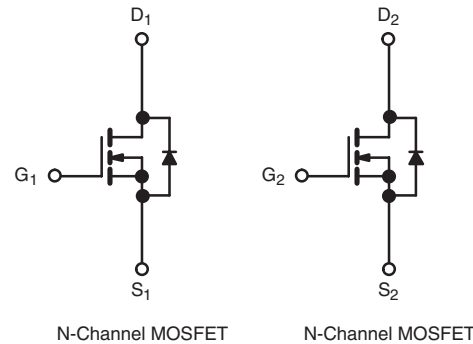
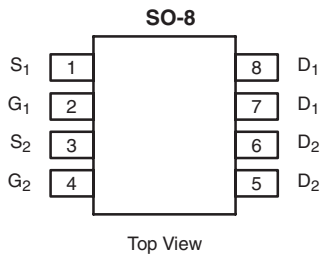
PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a, e</sup>	Q <sub>g</sub> (Typ.)
30	0.016 at V <sub>GS</sub> = 10 V	8	19
	0.018 at V <sub>GS</sub> = 4.5 V	8	
	0.024 at V <sub>GS</sub> = 2.5 V	8	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



**Ordering Information:** Si4922BDY-T1-E3 (Lead (Pb)-free)  
Si4922BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage	V <sub>DS</sub>	30	V			
Gate-Source Voltage	V <sub>GS</sub>	± 12				
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	8 <sup>e</sup>			
		T <sub>C</sub> = 70 °C	8 <sup>e</sup>			
		T <sub>A</sub> = 25 °C	8 <sup>b, c, e</sup>			
		T <sub>A</sub> = 70 °C	6.6 <sup>b, c</sup>			
Pulsed Drain Current (10 μs Pulse Width)	I <sub>DM</sub>	35	A			
Source-Drain Current Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			2.5	
		T <sub>A</sub> = 25 °C			1.7 <sup>b, c</sup>	
Pulsed Source-Drain Current	I <sub>SM</sub>	35				
Single Pulse Avalanche Current	I <sub>AS</sub>	15				
Single-Pulse Avalanche Energy	E <sub>AS</sub>	11.2	mJ			
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	3.1			
		T <sub>C</sub> = 70 °C	2			
		T <sub>A</sub> = 25 °C	2 <sup>b, c</sup>			
		T <sub>A</sub> = 70 °C	1.28 <sup>b, c</sup>			
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 50 to 150	°C			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Limit		Unit
			Typical	Maximum	
Maximum Junction-to-Ambient <sup>b, d</sup>	R <sub>thJA</sub>	50	62.5	°C/W	
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	30	40		

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 110 °C/W.
- Package Limited.

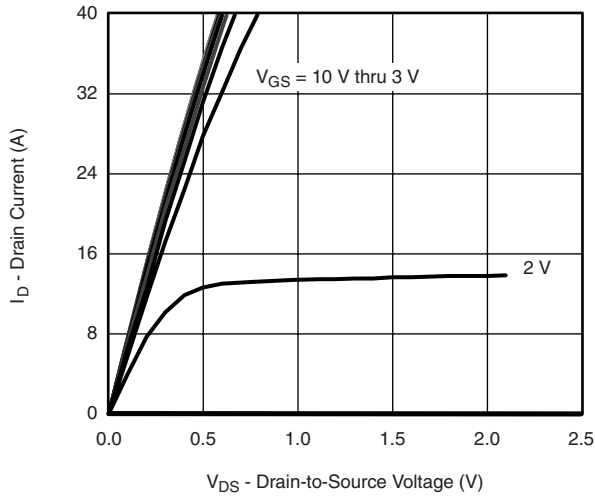
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	30			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4.6		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	0.6		1.8	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 12\text{ V}$			100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}$ , $V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 5\text{ A}$		0.0135	0.016	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 5\text{ A}$		0.0145	0.018	
		$V_{GS} = 2.5\text{ V}$ , $I_D = 5\text{ A}$		0.018	0.024	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 5\text{ A}$		30		S
<b>Dynamic<sup>a</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		2070		pF
Output Capacitance	$C_{oss}$			255		
Reverse Transfer Capacitance	$C_{rss}$			135		
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 5\text{ A}$		41	62	nC
		$V_{DS} = 15\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 5\text{ A}$		19	29	
Gate-Source Charge	$Q_{gs}$			3.5		
Gate-Drain Charge	$Q_{gd}$		3.7			
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		1.8	3	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$ , $R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$		7	14	ns
Rise Time	$t_r$			27	41	
Turn-Off Delay Time	$t_{d(off)}$			31	47	
Fall Time	$t_f$			8	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$ , $R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\text{ }\Omega$		13	25	
Rise Time	$t_r$			53	80	
Turn-Off Delay Time	$t_{d(off)}$			68	102	
Fall Time	$t_f$			54	81	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			2.5	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				35	
Body Diode Voltage	$V_{SD}$	$I_S = 1.7\text{ A}$		0.77	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 1.7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$		32	48	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			21	32	nC
Reverse Recovery Fall Time	$t_a$			13		ns
Reverse Recovery Rise Time	$t_b$			19		

## Notes:

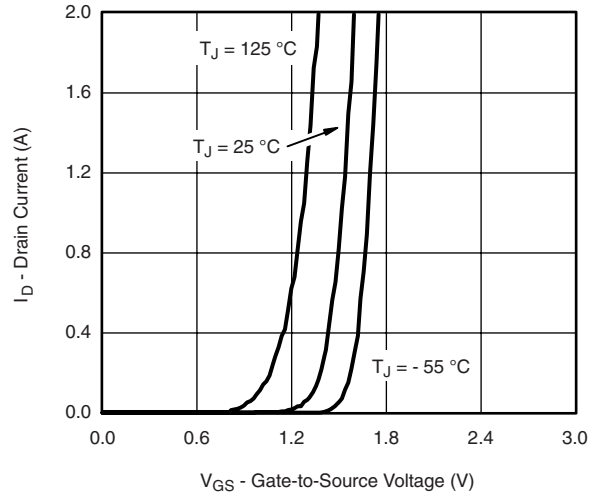
- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

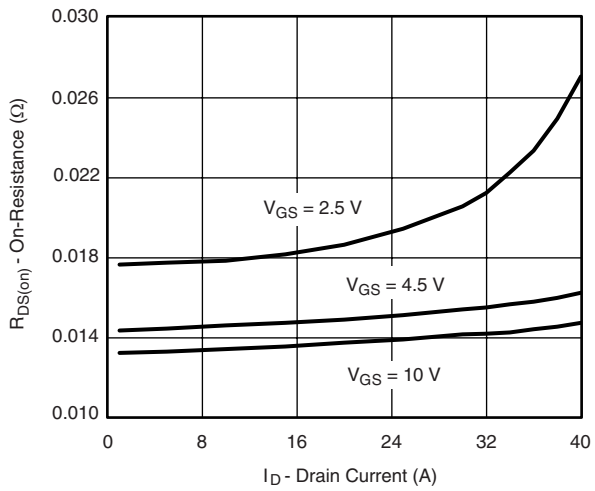
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



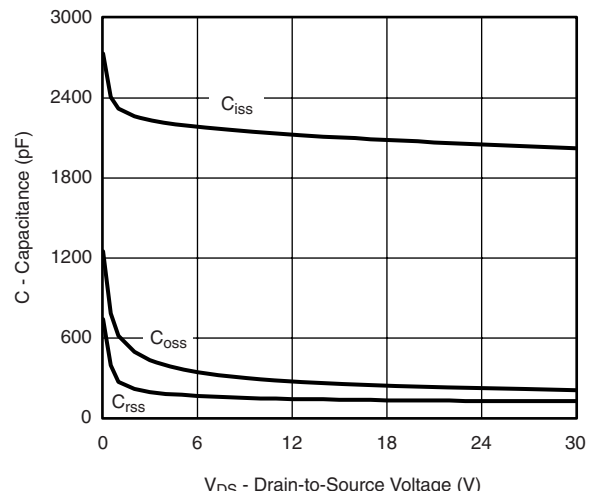
**Output Characteristics**



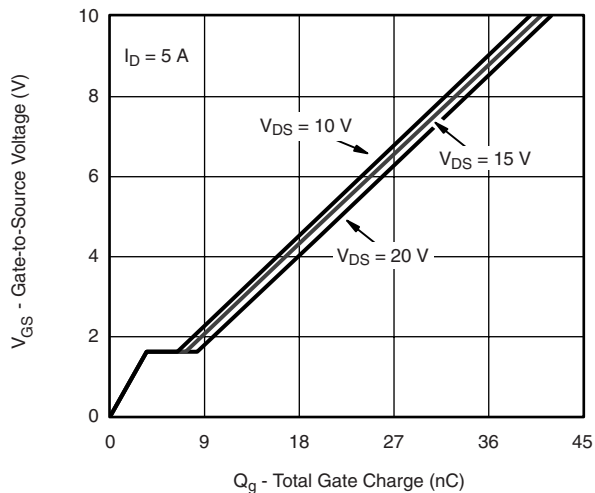
**Transfer Characteristics**



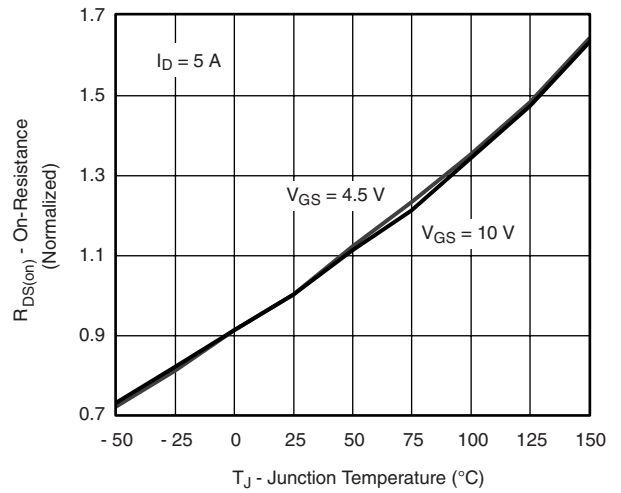
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

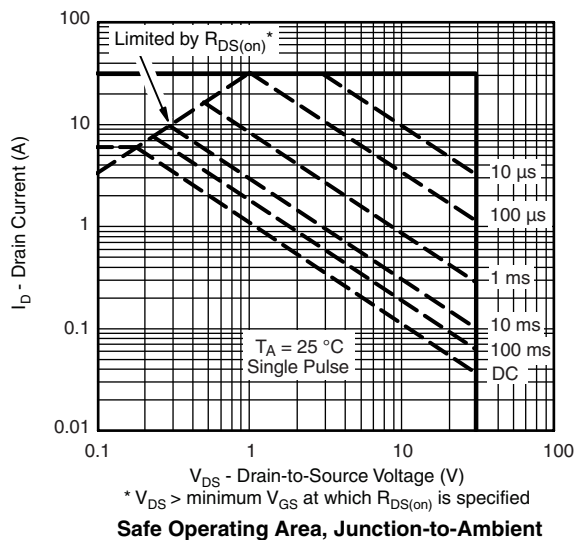
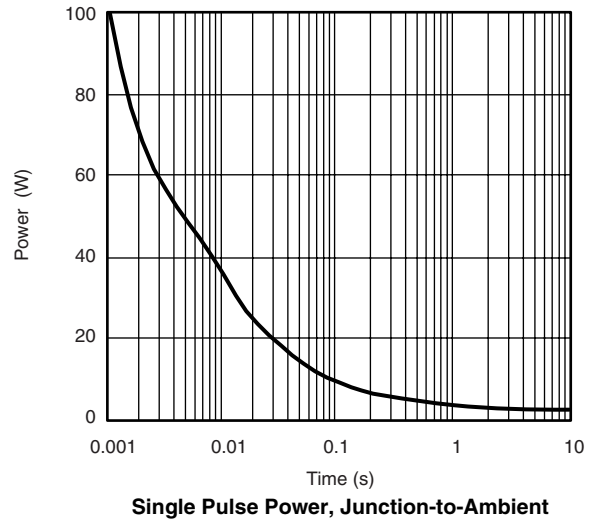
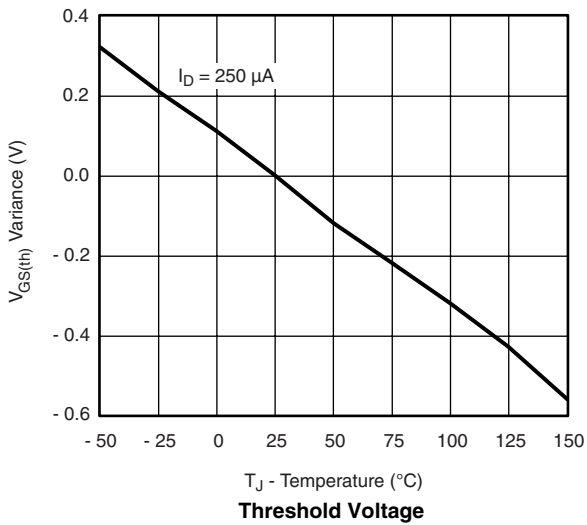
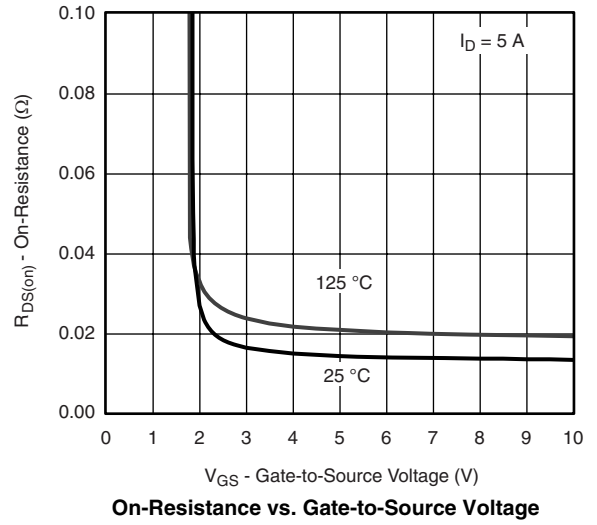
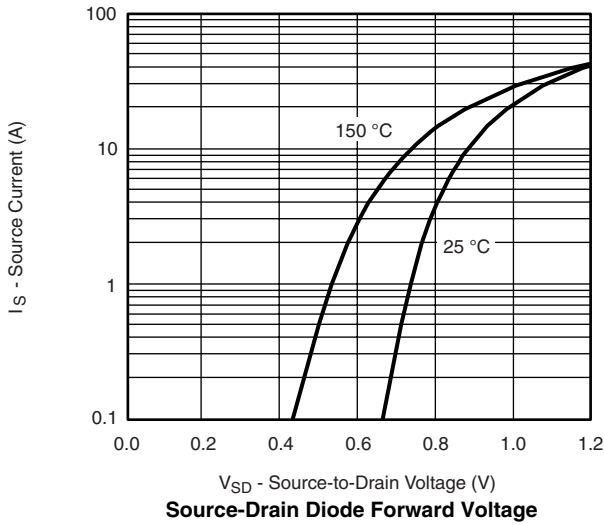


**Gate Charge**

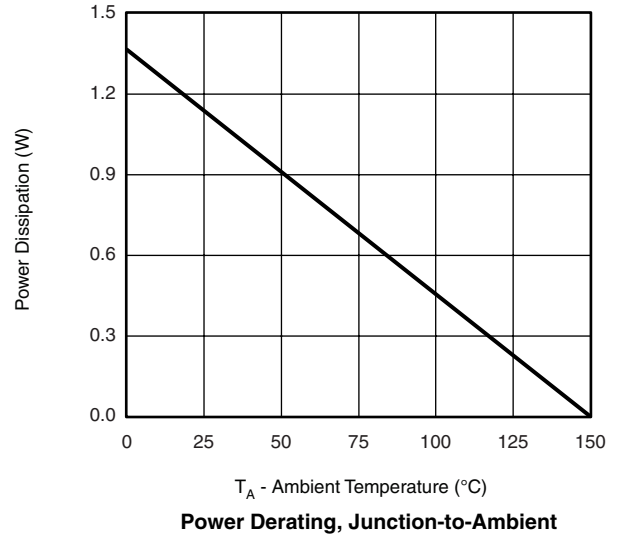
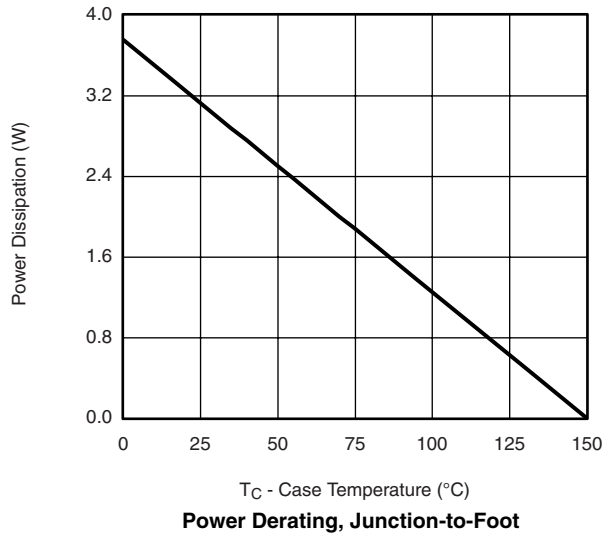
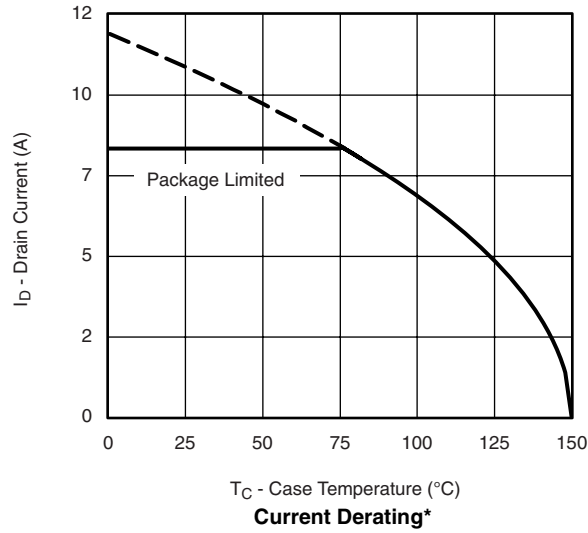


**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

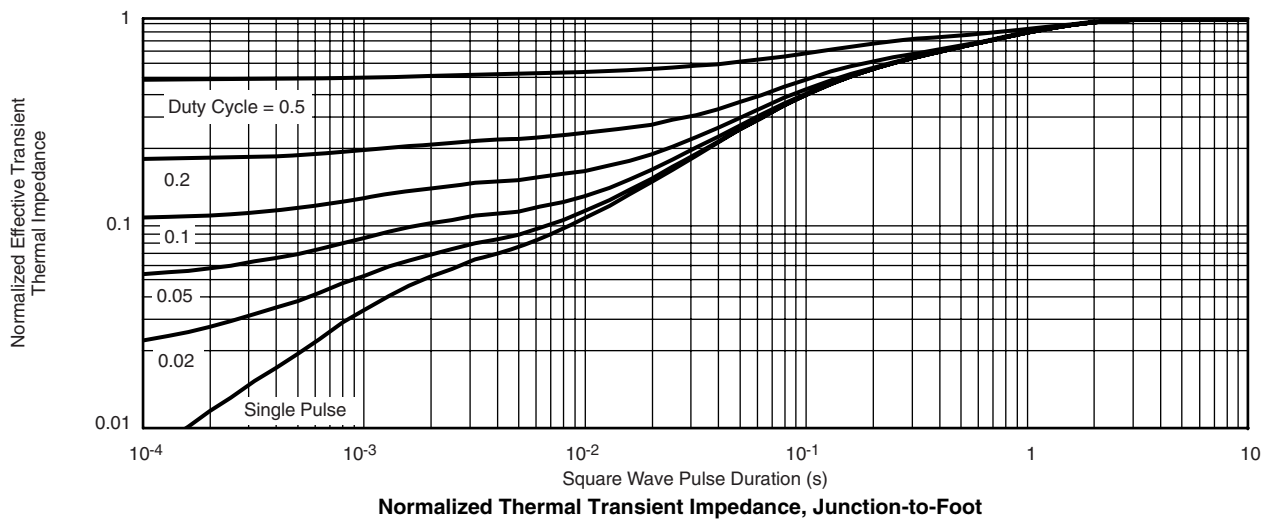
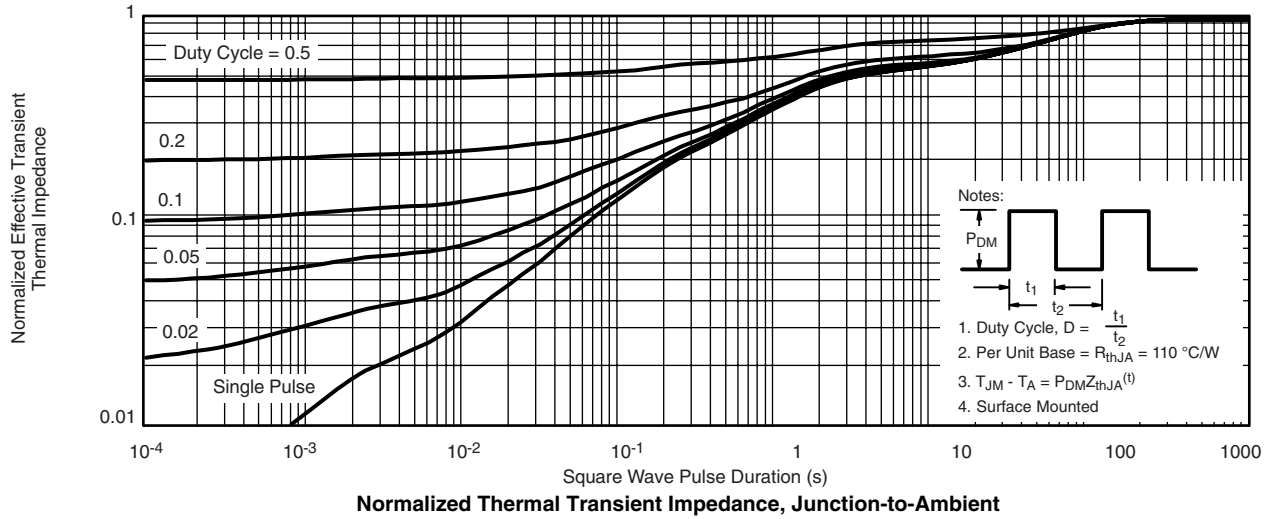


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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