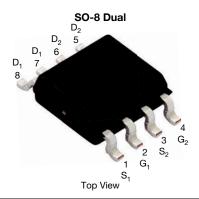


www.vishay.com

Vishay Siliconix

Dual N-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	30				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.040				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.050				
Q _g typ. (nC)	2.8				
I _D (A) ^d	5.8				
Configuration	Dual				

FEATURES

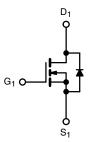
- TrenchFET® power MOSFET
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

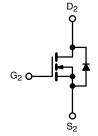


ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Low current DC/DC conversion
- Notebook system power





N-Channel MOSFET

N-Channel MOSFET

ORDERING INFORMATION			
Package	SO-8		
Lead (Pb)-free and halogen-free	Si4936CDY-T1-GE3		

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	30	V	
Gate-source voltage		V _{GS}	± 20	v	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		5.8		
	T _C = 70 °C	1 .	4.6		
	T _A = 25 °C	- I _D	5 a, b		
	T _A = 70 °C		4 a, b	A	
Pulsed drain current		I _{DM}	20		
Continuous source-drain diode current	T _C = 25 °C	I _S	1.9		
	T _A = 25 °C		1.4 ^{a, b}		
Maximum power dissipation	T _C = 25 °C	P _D	2.3		
	T _C = 70 °C		1.5	14/	
	T _A = 25 °C		1.7 ^{a, b}	W	
	T _A = 70 °C		1.1 ^{a, b}		
Operating junction and storage temperature	range	T _J , T _{stq}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient a, c	t ≤ 10 s	R_{thJA}	58	75	°C/W	
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	42	55	C/VV	

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. t = 10 s
- c. Maximum under steady state conditions is 110 °C/W
- d. Based on T_C = 25 °C

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static				•			
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	J In = 250 µA		32	-	mV/°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$			-5	-		
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.2	-	3	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
		V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	μА	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10		
On-state drain current a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	15	-	-	Α	
Duning and an adult and a state and a	Б	V _{GS} = 10 V, I _D = 5 A	-	0.033	0.040	Ω	
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.7 A	-	0.041	0.050		
Forward transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 5 \text{ A}$	-	15	-	S	
Dynamic ^b				•			
Input capacitance	C _{iss}		-	325	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	60	-		
Reverse transfer capacitance	C _{rss}		-	30	-		
-	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 5 A	-	6	9	nC	
Total gate charge			-	2.8	4.2		
Gate-source charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	1.1	-		
Gate-drain charge	Q _{gd}		-	0.8	-		
Gate resistance	R _g	f = 1 MHz	0.6	2.8	5.6	Ω	
Turn-on delay time	t _{d(on)}		-	12	18		
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_L = 3.8 \Omega$	-	13	20		
Turn-off delay time	t _{d(off)}	$I_D\cong 4$ A, $V_{GEN}=4.5$ V, $R_g=1~\Omega$	-	16	25		
Fall time	t _f		-	11	17		
Turn-on delay time	t _{d(on)}		-	4	8	ns	
Rise time	t _r	V_{DD} = 15 V, R_L = 3.8 Ω	-	9	18		
Turn-off delay time	t _{d(off)}	$I_D\cong 4$ A, V_{GEN} = 10 V, R_g = 1 Ω	-	11	20		
Fall time	t _f		-	8	15		
Drain-Source Body Diode Characteristic	es						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	1.9	_	
Pulse diode forward current	I _{SM}		-	-	20	A	
Body diode voltage	V_{SD}	I _S = 4 A, V _{GS} = 0 V	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}		-	11	20	ns	
Body diode reverse recovery charge	Q _{rr}	$I_F = 4 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	4	8	nC	
Reverse recovery fall time	t _a	$T_J = 25 ^{\circ}C$	-	6	-		
Reverse recovery rise time	t _b		_	5	-	ns	

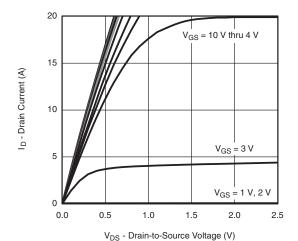
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

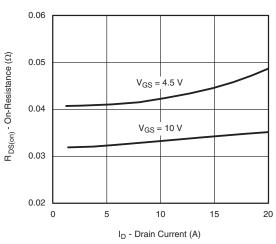
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



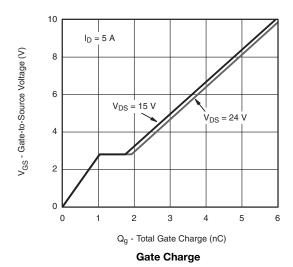
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

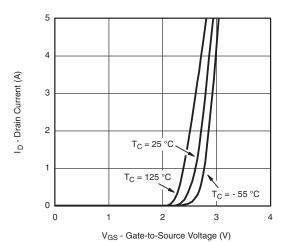


Output Characteristics

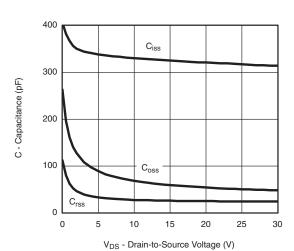


On-Resistance vs. Drain Current

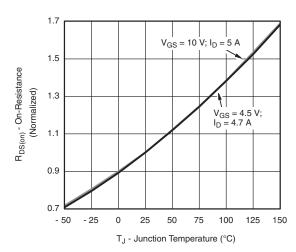




Transfer Characteristics



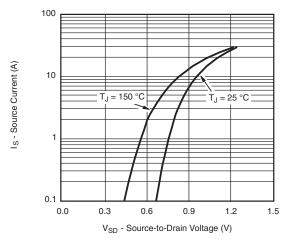
Capacitance



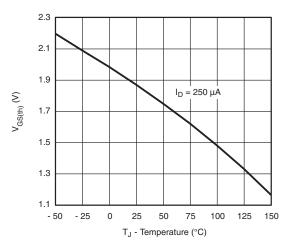
On-Resistance vs. Junction Temperature



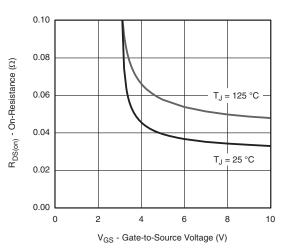
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



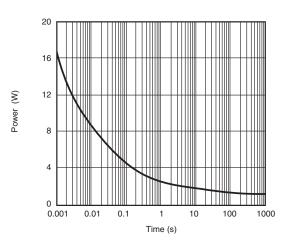
Source-Drain Diode Forward Voltage



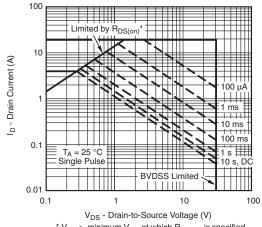
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power

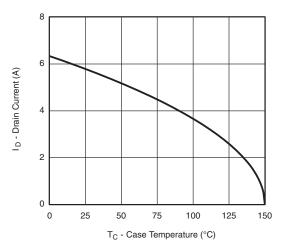


* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

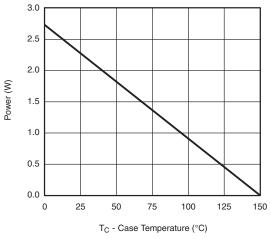
Safe Operating Area, Junction-to-Ambient

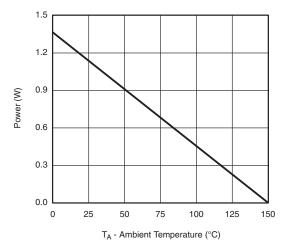
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating a





Power, Junction-to-Case

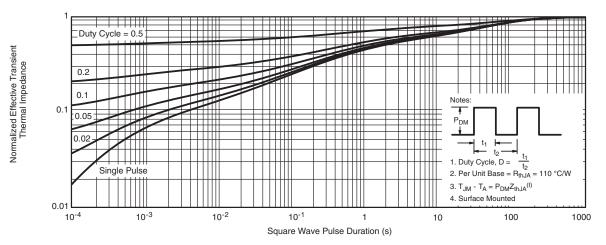
Power, Junction-to-Ambient

Note

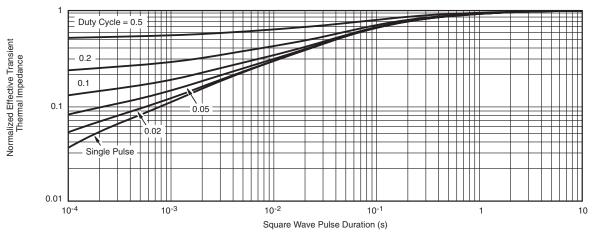
a. The power dissipation P_D is based on T_J max = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69097.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I. 11-Sep-06					

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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