

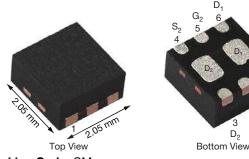
www.vishay.com

Vishay Siliconix

# **Dual N-Channel 30 V (D-S) MOSFET**

PRODUCT SUMMARY									
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) MAX.	I <sub>D</sub> (A)	Q <sub>g</sub> (TYP.)						
	0.025 at V <sub>GS</sub> = 10 V	4.5 <sup>a</sup>							
30	0.029 at V <sub>GS</sub> = 6 V	4.5 <sup>a</sup>	3 nC						
	0.033 at V <sub>GS</sub> = 4.5 V	4.5 <sup>a</sup>							

## PowerPAK® SC-70-6L Dual



Marking Code: CM **Ordering Information:** 

SiA928DJ-T1-GE3 (lead (Pb)-free and halogen free)

#### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
  - Small footprint area
  - Low on-resistance
- 100 % Ra tested

• Material categorization: for definitions of compliance please www.vishav.com/doc?99912

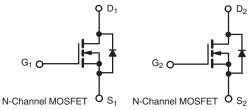


RoHS COMPLIANT HALOGEN

FREE

#### **APPLICATIONS**

- Portable devices such as smart phones, tablet PCs and mobile computing
  - Load switch
- DC/DC converter
- Power management



ABSOLUTE MAXIMUM RATING	<b>S</b> (T <sub>A</sub> = 25 °C, υ	inless otherwis	se noted)	
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage	V <sub>GS</sub>	+20 / -16	v	
	T <sub>C</sub> = 25 °C		4.5 <sup>a</sup>	
Continuous Dunin Comment (T., 150.90)	T <sub>C</sub> = 70 °C	. –	4.5 <sup>a</sup>	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	4.5 a, b, c	
	T <sub>A</sub> = 70 °C		4.5 <sup>a, b, c</sup>	А
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	30		
Continuos Como Durio Diodo Como t	T <sub>C</sub> = 25 °C		4.5 <sup>a</sup>	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	l <sub>S</sub>	1.6 <sup>b, c</sup>	
	T <sub>C</sub> = 25 °C		7.8	
Maniero Daniero Dissipation	T <sub>C</sub> = 70 °C		5	10/
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	1.9 <sup>b, c</sup>	W
	T <sub>A</sub> = 70 °C		1.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering Recommendations (Peak tempera		260		

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum Junction-to-Ambient b, f	unction-to-Ambient b, f $t \le 5$ s $R_{thJA}$ 52 65		65	°C/W					
Maximum Junction-to-Case (Drain)	Steady state	R <sub>thJC</sub>	12.5	16	7 0/00				

- a. Package limited, T<sub>C</sub> = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state condition is 110 °C/W.



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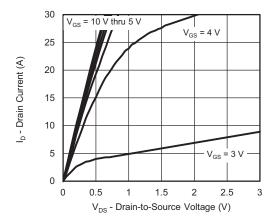
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static			ı	l	l	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>		-	14.7	-	mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250  \mu A$	-	-4.6	-	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.2	-	2.2	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = +20 / -16 \text{ V}$	-	-	± 100	nA
Zava Cata Valtaga Dvain Current		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	-	-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$		-	10	μA
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	5	-	-	Α
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	-	0.020	0.025	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 6 V, I <sub>D</sub> = 4 A	-	0.023	0.029	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	-	0.026	0.033	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 A	-	25	-	S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>		-	490	-	pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	150	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	10	-	
C <sub>rss</sub> /C <sub>iss</sub> Ratio			-	0.021	0.042	-
Total Gate Charge	0	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	-	6.6	10	nC
Total Gate Charge	$Q_g$		-	3	4.5	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	1.4	-	
Gate-Drain Charge	$Q_{gd}$		-	0.5	-	
Output Charge	Q <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$	-	4.2	-	
Gate Resistance	$R_g$	f = 1 MHz	0.9	4.6	6.9	Ω
Turn-On Delay Time	t <sub>d(on)</sub>		-	13	25	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 3 $\Omega$	-	45	90	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	13	25	
Fall Time	t <sub>f</sub>		-	25	50	ne
Turn-On Delay Time	t <sub>d(on)</sub>		-	5	10	ns
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 3 $\Omega$	-	27	55	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 5$ A, $V_{GEN}=10$ V, $R_g=1$ $\Omega$	-	10	20	
Fall Time	t <sub>f</sub>		_	8	15	
<b>Drain-Source Body Diode Characteristic</b>	s					
Continuous Source-Drain Diode Current	Is	T <sub>C</sub> = 25 °C	-	-	4.5	А
Pulse Diode Forward Current	I <sub>SM</sub>		-	-	30	A
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.85	1.2	٧
Body Diode Reverse Recovery Time	Body Diode Reverse Recovery Time t <sub>rr</sub>		-	20	40	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$I_F = 5 A$ , $dI/dt = 100 A/\mu s$ ,	-	7	15	nC
Reverse Recovery Fall Time	ta	T <sub>J</sub> = 25 °C	-	9.5	-	- ns
Reverse Recovery Rise Time	t <sub>b</sub>			10.5	1	

#### Notes

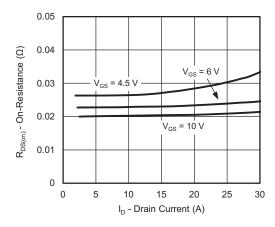
- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

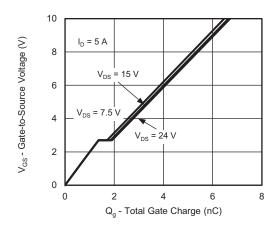




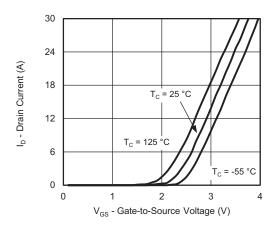
#### **Output Characteristics**



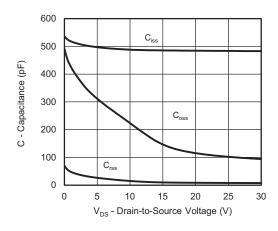
On-Resistance vs. Drain Current and Gate Voltage



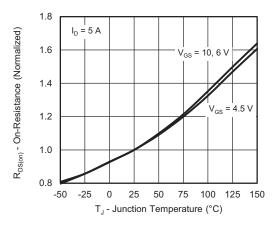
**Gate Charge** 



**Transfer Characteristics** 

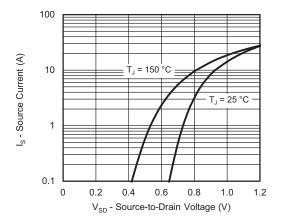


Capacitance

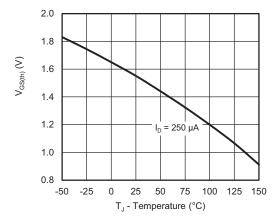


On-Resistance vs. Junction Temperature

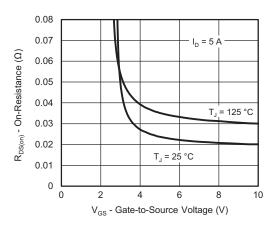




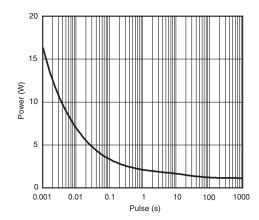
Source-Drain Diode Forward Voltage



**Threshold Voltage** 

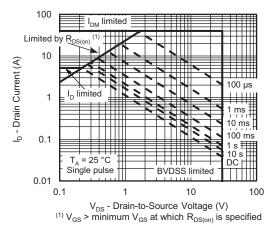


On-Resistance vs. Gate-to-Source Voltage

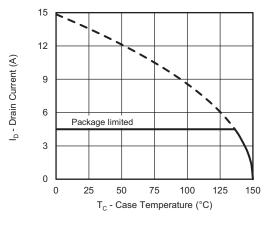


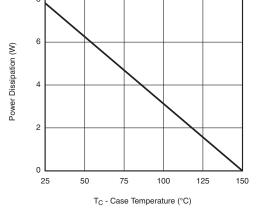
Single Pulse Power (Junction-to-Ambient)





Safe Operating Area, Junction-to-Ambient





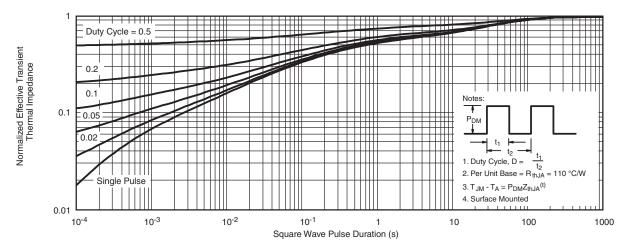
Current Derating a

**Power Derating** 

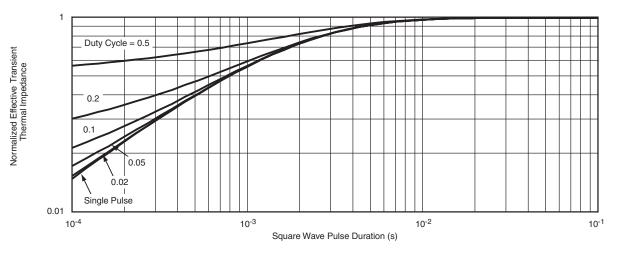
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg275168">www.vishay.com/ppg275168</a>.





Vishay Siliconix

# PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
  Package outline exclusive of mold flash and metal burr
  Package outline inclusive of plating

	SINGLE PAD						DUAL PAD					
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC		
K		0.275 TYP			0.011 TYP		0.275 TYP		0.011 TYP			
K1		0.400 TYP			0.016 TYP		0.320 TYP		0.013 TYP			
K2		0.240 TYP		0.009 TYP		0.252 TYP		0.010 TYP				
К3		0.225 TYP		0.009 TYP					•	•		
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



# RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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