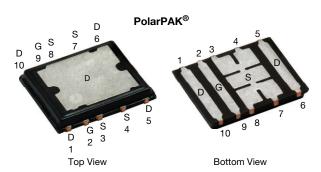
Vishay Siliconix

# N-Channel 25 V (D-S) MOSFET

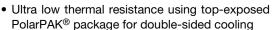


Top surface is connected to pins 1, 5, 6, and 10

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	25
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0014
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0018
Q <sub>g</sub> typ. (nC)	46
I <sub>D</sub> (A) <sup>a</sup> (package limit)	60
I <sub>D</sub> (A) <sup>a</sup> (silicon limit)	229
Configuration	Single

#### **FEATURES**

• TrenchFET® Gen III power MOSFET

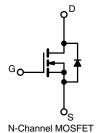




- · Leadframe-based encapsulated package
  - Die not exposed
  - Same layout regardless of die size, ≤ 100 V
- Low Q<sub>ad</sub>/Q<sub>as</sub> ratio helps prevent shoot-through
- 100 % R<sub>a</sub> and UIS tested
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

#### **APPLICATIONS**

- VRM
- DC/DC conversion: low side
- Server V<sub>CORE</sub>



ORDERING INFORMATION	
Package	PolarPAK
Lead (Pb)-free and halogen-free	SiE882DF-T1-GE3

ABSOLUTE MAXIMUM RATING	<b>iS</b> (T <sub>A</sub> = 25 °C, υ	ınless otherwi	se noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	25	V	
Gate-source voltage		V <sub>GS</sub>	± 20	V	
	T 05 °C		60 <sup>a</sup> (package limit)		
	T <sub>C</sub> = 25 °C		229 (silicon limit)		
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	60 a		
	T <sub>A</sub> = 25 °C		47 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		41 <sup>b, c</sup>	А	
Pulsed drain current		I <sub>DM</sub>	100		
Outlier and a supplied to the design of	T <sub>C</sub> = 25 °C		60 <sup>a</sup>		
Continuous source-drain diode current	T <sub>A</sub> = 25 °C	l <sub>s</sub>	4.3 <sup>b, c</sup>		
Single pulse avalanche current	1 0.1 ml l	I <sub>AS</sub>	50		
Avalanche energy	L = 0.1 mH	E <sub>AS</sub>	125	mJ	
	T <sub>C</sub> = 25 °C		125		
Marrian and a sure distribution	T <sub>C</sub> = 70 °C	1 5 6	80	14/	
Maximum power dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5.2 <sup>b, c</sup>	w	
	T <sub>A</sub> = 70 °C		3.3 <sup>b, c</sup>		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) d, e			260		

#### Notes

- a. Package limited is 60 A
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



# Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient a, b	t ≤ 10 s	$R_{thJA}$	20	24	
Maximum junction-to-case (drain top)	Steady state	R <sub>thJC</sub> (drain)	0.8	1	°C/W
Maximum junction-to-case (source) a, c	Steady State	R <sub>thJC</sub> (source)	2.2	2.7	

#### **Notes**

- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 68 °C/W
- c. Measured at source pin (on the side of the package)

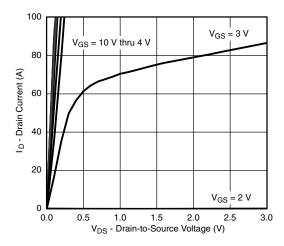
PARAMETER	AMETER SYMBOL TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	25	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	J 050 A	-	25	-	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-6	-	mV/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	1	1.7	2.2	V
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
Zana mata walitana aluain ayumuut		V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V	-	-	1	μΑ
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	25	-	-	Α
Duning and an atota maniatana a	Б	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.0011	0.0014	0
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	-	0.0015	0.0018	Ω
Forward transconductance a	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_D = 20 \text{ A}$	-	125	-	S
Dynamic <sup>b</sup>			,			,
Input capacitance	C <sub>iss</sub>		-	6400	-	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 12.5 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	1400	-	pF
Reverse transfer capacitance	C <sub>rss</sub>		-	550	-	
Total sate aboves		$V_{DS} = 12.5 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	96	145	
Total gate charge	$Q_g$		-	46	70	
Gate-source charge	Q <sub>qs</sub>	$V_{DS} = 12.5 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	-	18	-	nC
Gate-drain charge	Q <sub>gd</sub>		-	12	-	
Gate resistance	$R_g$	f = 1 MHz	0.2	1.1	2.2	Ω
Turn-on delay time	t <sub>d(on)</sub>		-	45	70	
Rise time	t <sub>r</sub>	$V_{DD} = 12.5 \text{ V}, R_L = 1.25 \Omega,$		170	255	
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	65	100	
Fall time	t <sub>f</sub>		-	85	130	1
Turn-on delay time	t <sub>d(on)</sub>			20	30	ns
Rise time	t <sub>r</sub>	$V_{DD} = 12.5 \text{ V}, R_L = 1.25 \Omega,$	-	15	25	
Turn-off delay time	t <sub>d(off)</sub>	$I_D\cong 10~A,~V_{GEN}=10~V,~R_g=1~\Omega$	-	45	70	
Fall time	t <sub>f</sub>			10	15	
<b>Drain-Source Body Diode Characterist</b>	ics					
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	60	_
Pulse diode forward current <sup>a</sup>	I <sub>SM</sub>			-	100	Α
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A	-	0.8	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>		-	55	85	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	70	105	nC
Reverse recovery fall time	ta	T <sub>J</sub> = 25 °C	-	25	-	
Reverse recovery rise time	t <sub>b</sub>	-a		30	_	ns

#### Notes

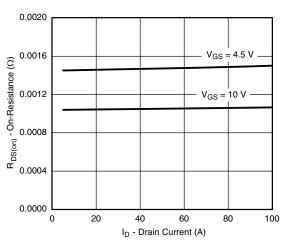
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

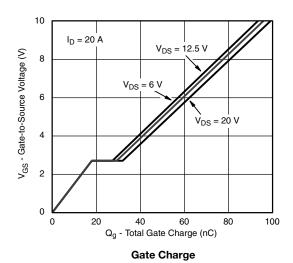


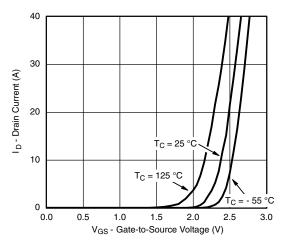


#### **Output Characteristics**

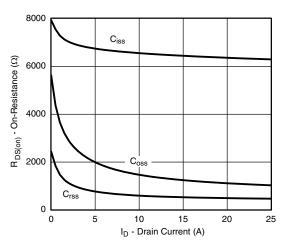


On-Resistance vs. Drain Current and Gate Voltage

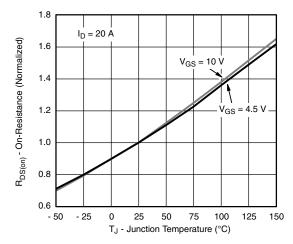




**Transfer Characteristics** 

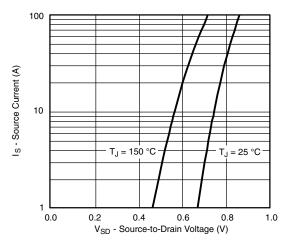


Capacitance

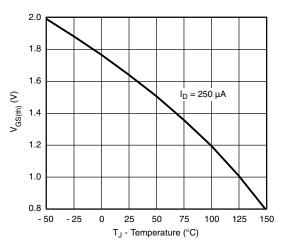


On-Resistance vs. Junction Temperature

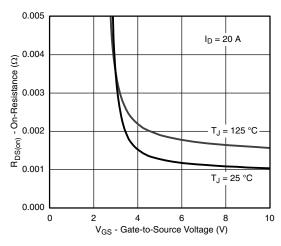




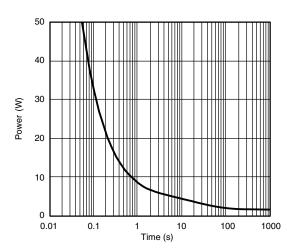
#### Source-Drain Diode Forward Voltage



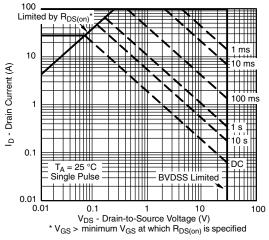
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage

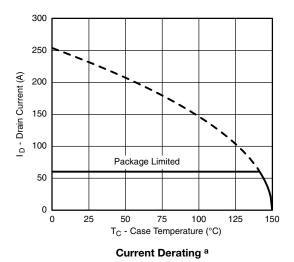


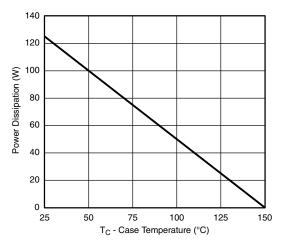
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient





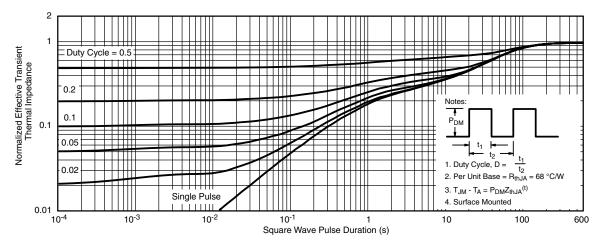


Power Derating, Junction-to-Case

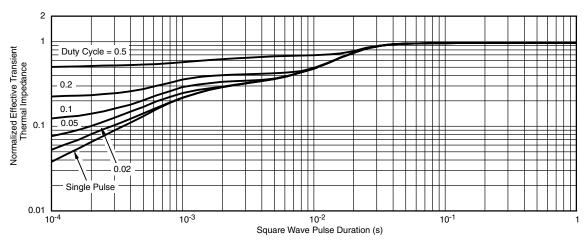
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

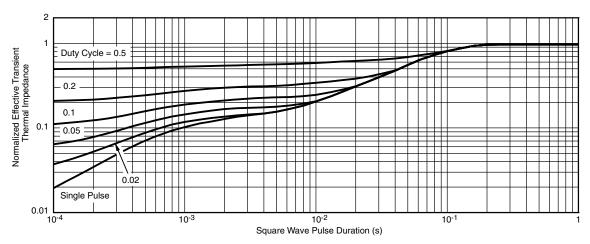




#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)



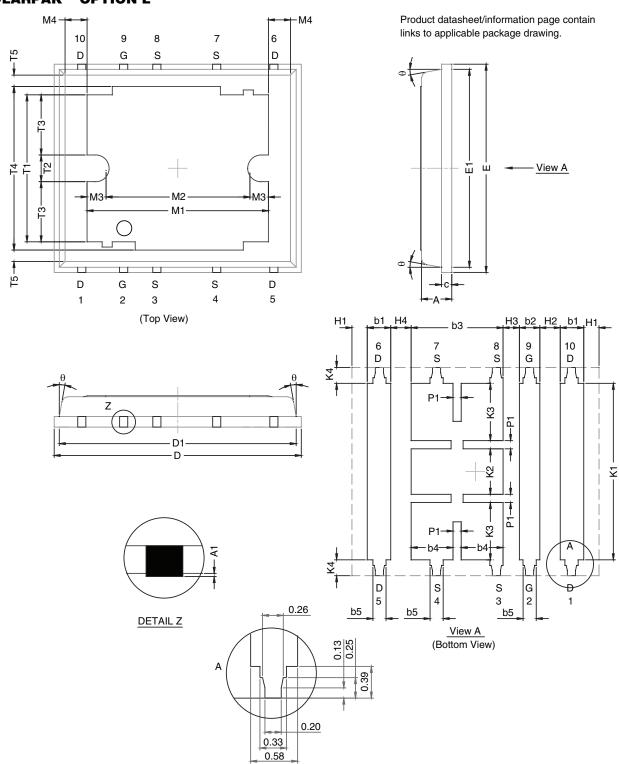
#### Normalized Thermal Transient Impedance, Junction-to-Source

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?65002">www.vishay.com/ppg?65002</a>.



Vishay Siliconix

#### POLARPAK™ OPTION L



# Package Information

# Vishay Siliconix



	MILLIMETERS			INCHES			
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.75	0.80	0.85	0.030	0.031	0.033	
A1	0.00	-	0.05	0.000	-	0.002	
b1	0.48	0.58	0.68	0.019	0.023	0.027	
b2	0.41	0.51	0.61	0.016	0.020	0.024	
b3	2.19	2.29	2.39	0.086	0.090	0.094	
b4	0.89	1.04	1.19	0.035	0.041	0.047	
b5	0.23	0.33	0.43	0.009	0.013	0.017	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	6.00	6.15	6.30	0.236	0.242	0.248	
D1	5.74	5.89	6.04	0.226	0.232	0.238	
E	5.01	5.16	5.31	0.197	0.203	0.209	
E1	4.75	4.90	5.05	0.187	0.193	0.199	
H1	0.23	-	-	0.009	-	-	
H2	0.45	-	0.56	0.018	-	0.022	
H3	0.31	0.41	0.51	0.012	0.016	0.020	
H4	0.45	-	0.56	0.018	-	0.022	
K1	4.22	4.37	4.52	0.166	0.172	0.178	
K2	1.08	1.13	1.18	0.043	0.044	0.046	
K3	1.37	-	-	0.054	-	-	
K4	0.24	-	-	0.009	-	-	
M1	4.30	4.50	4.70	0.169	0.177	0.185	
M2	3.43	3.58	3.73	0.135	0.141	0.147	
МЗ	0.22	-	-	0.009	-	-	
M4	0.05	-	-	0.002	-	-	
P1	0.15	0.20	0.25	0.006	0.008	0.010	
T1	3.48	3.64	4.10	0.137	0.143	0.161	
T2	0.56	0.76	0.95	0.022	0.030	0.037	
T3	1.20	-	-	0.047	-	=	
T4	3.90	-	-	0.153	-	-	
T5	0	0.18	0.36	0.000	0.007	0.014	
θ	0°	10°	12°	0°	10°	12°	

DWG: 5946

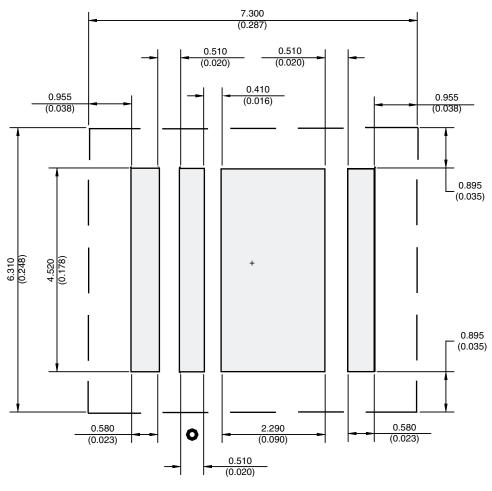
#### Notes

Millimeters govern over inches.

# APPLICATION NOTE



## RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S Dimensions in mm/(Inches) No External Traces within Broken Lines Dot indicates Gate Pin (Part Marking)

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