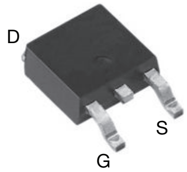
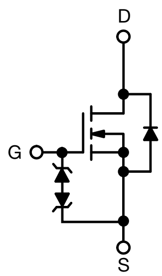
E Series Power MOSFET

DPAK (TO-252)





N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) R_{on} x Q_g
- Low effective capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Integrated Zener diode ESD protection
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT HALOGEN FREE

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	850	
$R_{DS(on)}$ typ. (Ω) at 25 °C	V_{GS} = 10 V	0.826
Q_g max. (nC)	22.5	
Q_{gs} (nC)	4	
Q_{gd} (nC)	7	
Configuration	Single	

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy

ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free and halogen-free	SiHD6N80AE-GE3
	SiHD6N80AET4-GE3

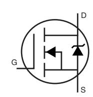
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	800	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	5	A
		T_C = 100 °C		3.2	
Pulsed drain current [a]			I_{DM}	10	
Linear derating factor				0.5	W/°C
Single pulse avalanche energy [b]			E_{AS}	20.3	mJ
Maximum power dissipation			P_D	62.5	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope		T_J = 125 °C	dv/dt	100	V/ns
Reverse diode dv/dt [d]				0.4	
Soldering recommendations (peak temperature) [c]		For 10 s		260	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 1.2 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, di/dt = 100 A/μs, starting T_J = 25 °C

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	2	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		800	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.8	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2	-	4	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 10	μA
		V_{GS} = ± 30 V		-	-	± 50	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 800 V, V_{GS} = 0 V		-	-	1	μA
		V_{DS} = 640 V, V_{GS} = 0 V, T_J = 125 °C		-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 2 A	-	0.826	0.950	Ω
Forward transconductance [a]	g_{fs}	V_{DS} = 30 V, I_D = 3 A		-	1.9	-	S
Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz		-	422	-	pF
Output capacitance	C_{oss}			-	24	-	
Reverse transfer capacitance	C_{rss}			-	4	-	
Effective output capacitance, energy related [a]	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V		-	17	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$			-	92	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 3 A, V_{DS} = 640 V	-	15	22.5	nC
Gate-source charge	Q_{gs}			-	4	-	
Gate-drain charge	Q_{gd}			-	7	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 640 V, I_D = 3 A, V_{GS} = 10 V, R_g = 9.1 Ω		-	12	24	ns
Rise time	t_r			-	10	20	
Turn-off delay time	$t_{d(off)}$			-	16	32	
Fall time	t_f			-	20	40	
Gate input resistance	R_g	f = 1 MHz, open drain		1	2	4	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5	A
Pulsed diode forward current	I_{SM}			-	-	10	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 3 A, V_{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S = 3 A, di/dt = 100 A/μs, V_R = 25 V		-	285	570	ns
Reverse recovery charge	Q_{rr}			-	1.7	3.4	μC
Reverse recovery current	I_{RRM}			-	9.9	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

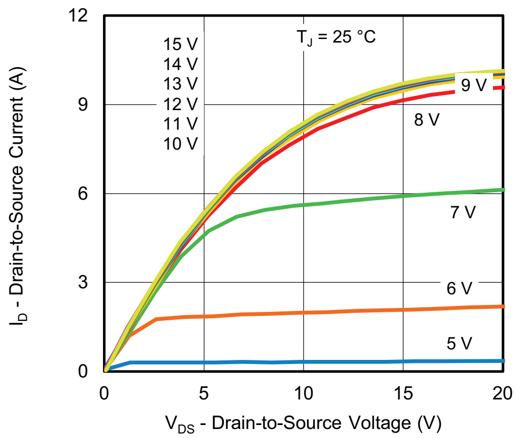


Fig. 1 - Typical Output Characteristics

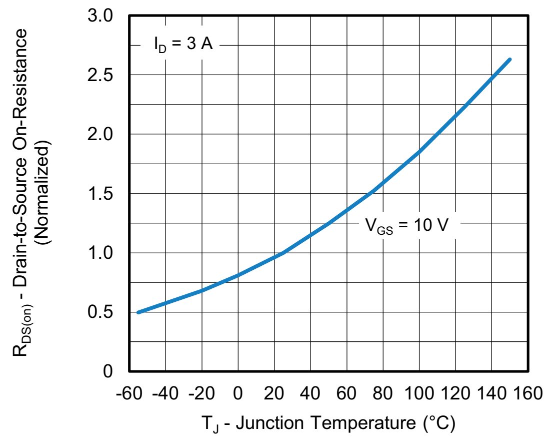


Fig. 4 - Normalized On-Resistance vs. Temperature

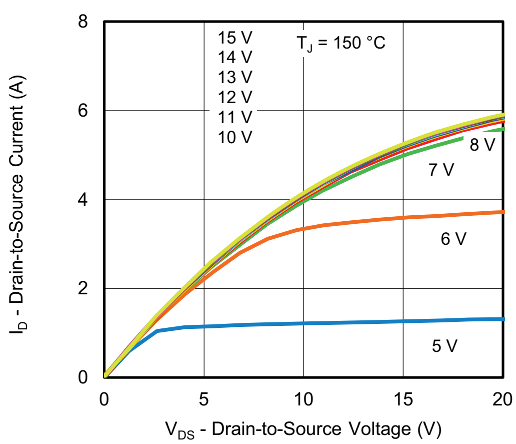


Fig. 2 - Typical Output Characteristics

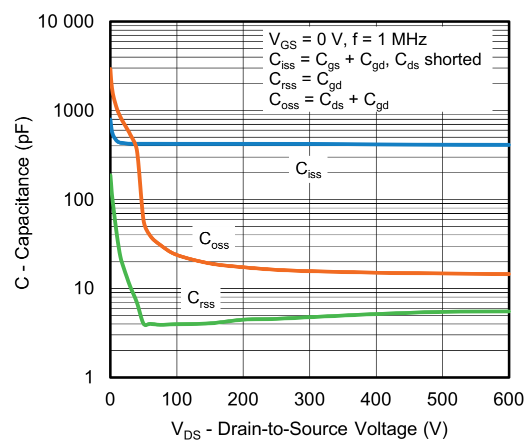


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

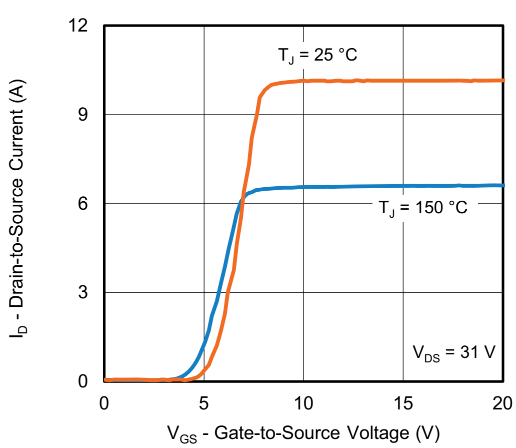


Fig. 3 - Typical Transfer Characteristics

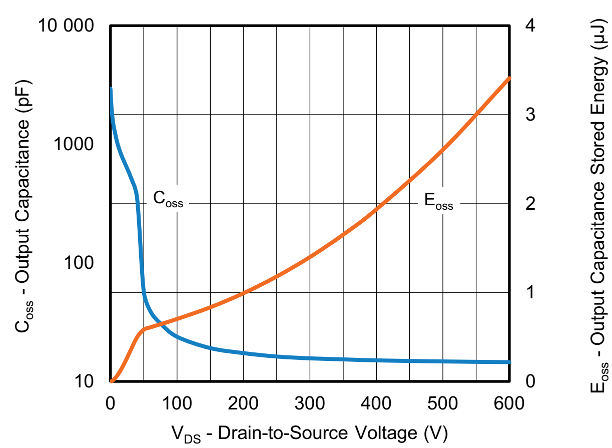


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

For technical questions, contact: hvm@vishay.com

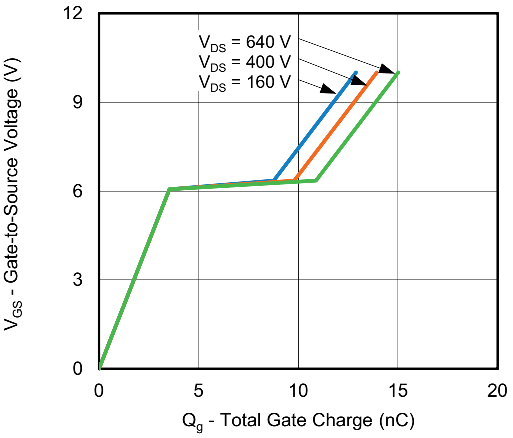


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

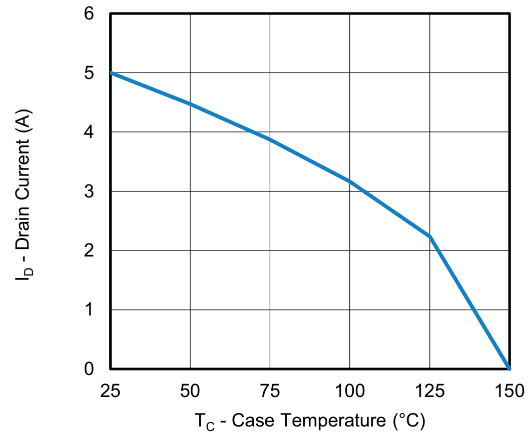


Fig. 10 - Maximum Drain Current vs. Case Temperature

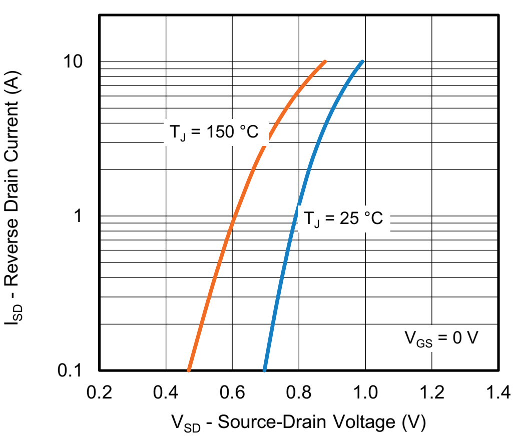


Fig. 8 - Typical Source-Drain Diode Forward Voltage

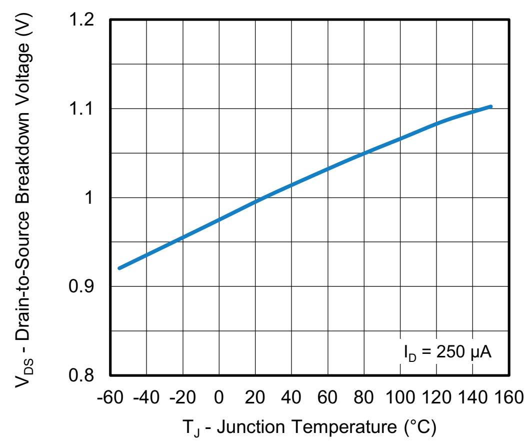


Fig. 11 - Temperature vs. Drain-to-Source Voltage

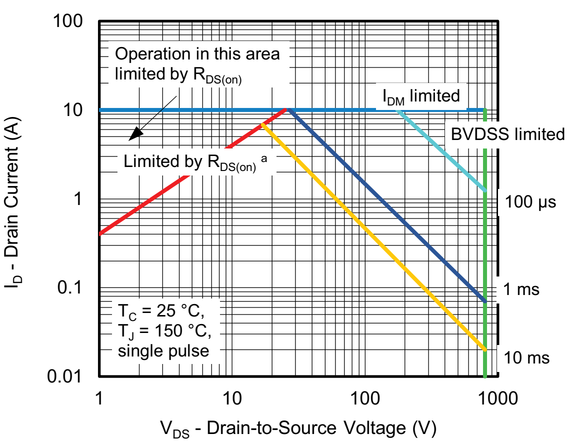


Fig. 9 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

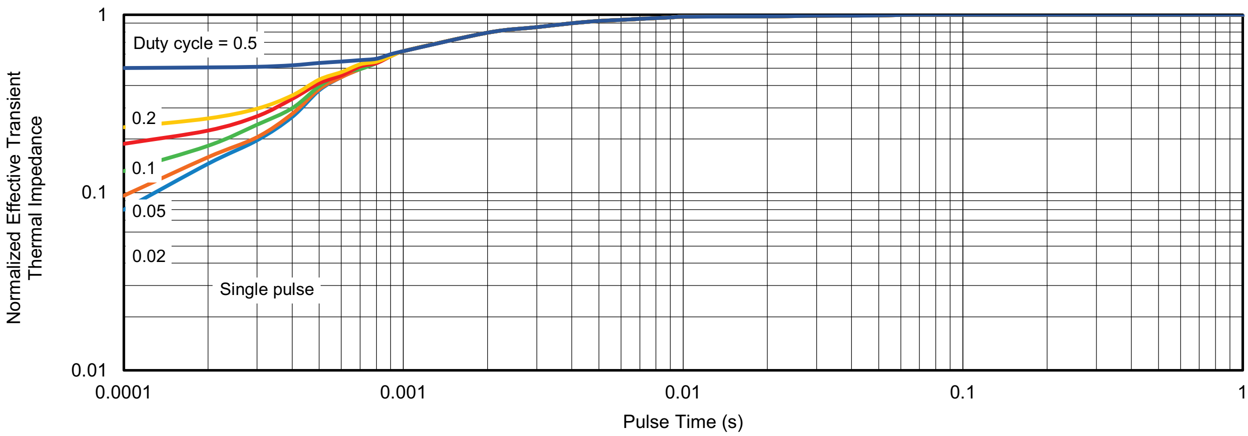


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

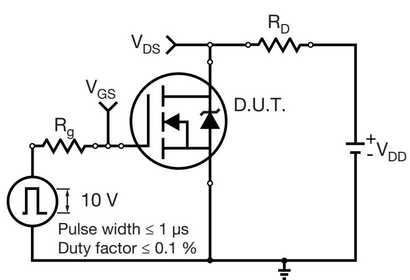


Fig. 13 - Switching Time Test Circuit

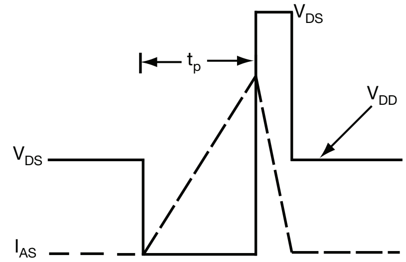


Fig. 16 - Unclamped Inductive Waveforms

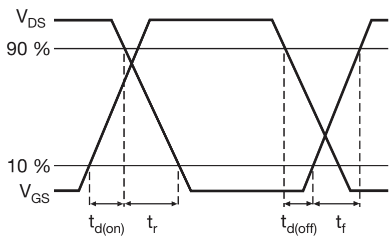


Fig. 14 - Switching Time Waveforms

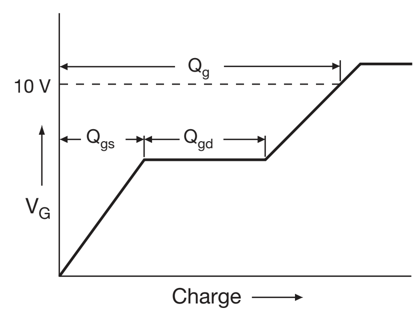


Fig. 17 - Basic Gate Charge Waveform

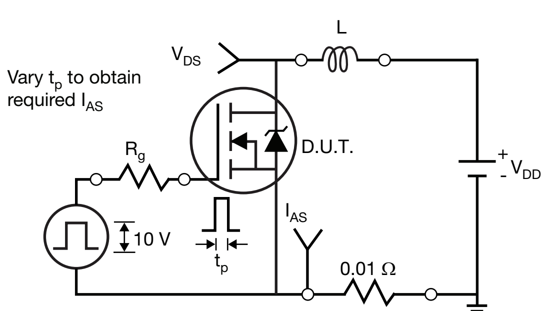


Fig. 15 - Unclamped Inductive Test Circuit

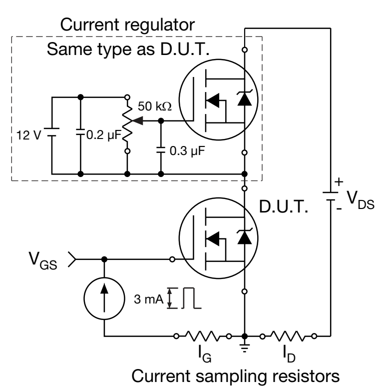
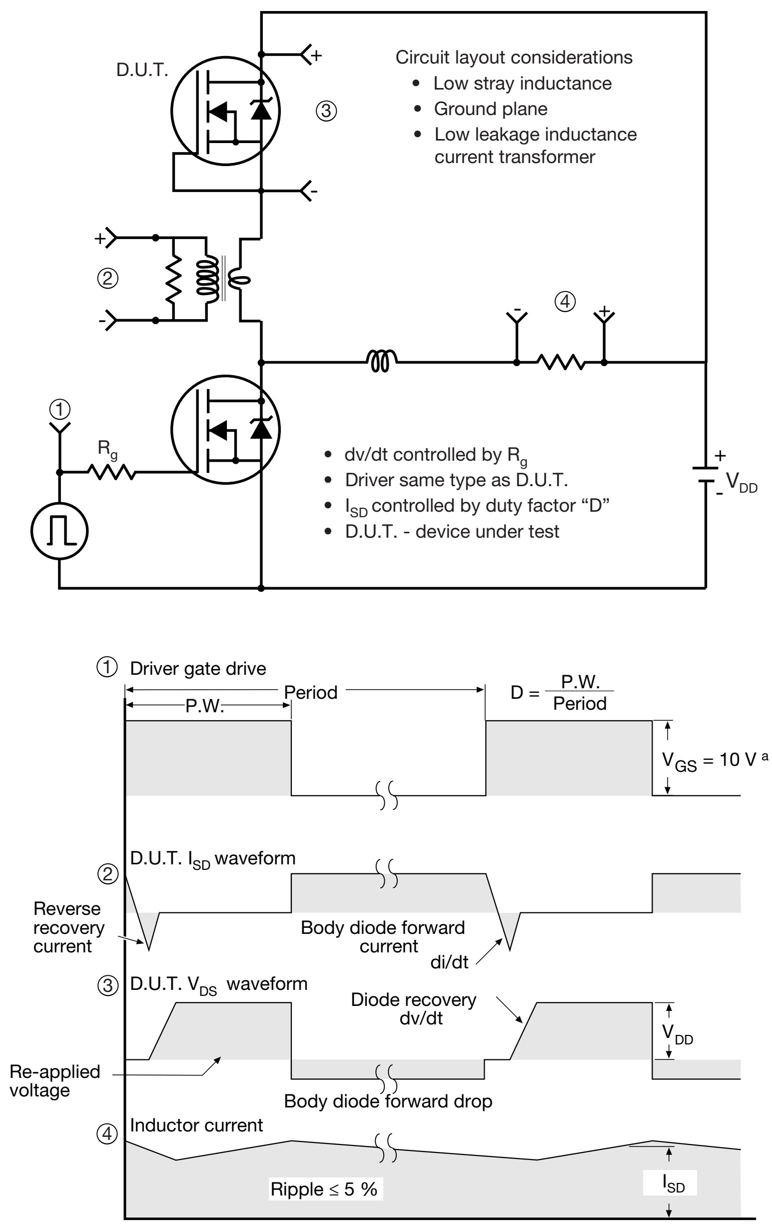


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

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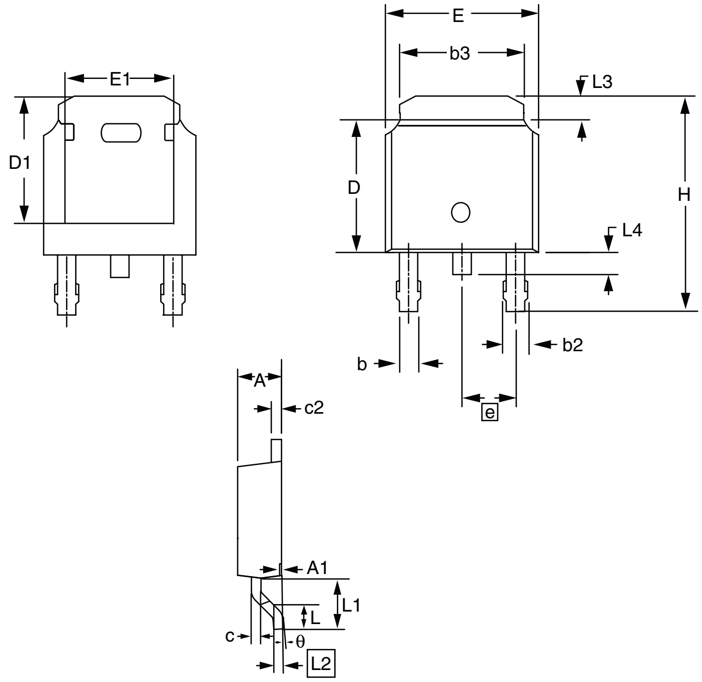
TO-252AA (HIGH VOLTAGE)

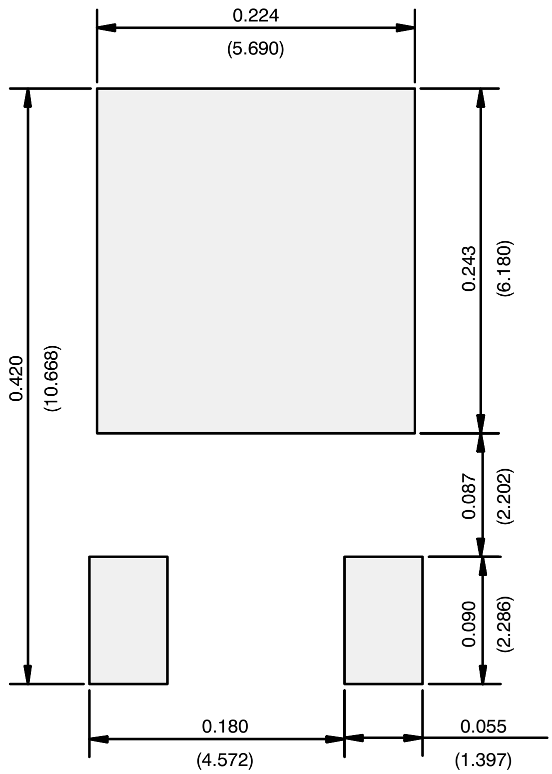


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
E	6.40	6.73	0.252	0.265
L	1.40	1.77	0.055	0.070
L1	2.743 REF		0.108 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.89	1.27	0.035	0.050
L4	0.64	1.01	0.025	0.040
D	6.00	6.22	0.236	0.245
H	9.40	10.40	0.370	0.409
b	0.64	0.88	0.025	0.035
b2	0.77	1.14	0.030	0.045
b3	5.21	5.46	0.205	0.215
e	2.286 BSC		0.090 BSC	
A	2.20	2.38	0.087	0.094
A1	0.00	0.13	0.000	0.005
c	0.45	0.60	0.018	0.024
c2	0.45	0.58	0.018	0.023
D1	5.30	-	0.209	-
E1	4.40	-	0.173	-
θ	0'	10'	0'	10'
ECN: S-81965-Rev. A, 15-Sep-08 DWG: 5973				

Notes

1. Package body sizes exclude mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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