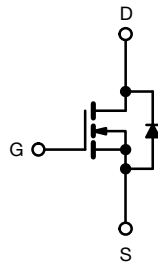
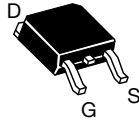


## E Series Power MOSFET

**DPAK  
(TO-252)**


N-Channel MOSFET


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### PRODUCT SUMMARY

|   |                 |       |
|---|-----------------|-------|
| $V_{DS}$ (V) at $T_J$ max.              | 650             |       |
| $R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C | $V_{GS} = 10$ V | 0.320 |
| $Q_g$ max. (nC)                         | 52              |       |
| $Q_{gs}$ (nC)                           | 6               |       |
| $Q_{gd}$ (nC)                           | 13              |       |
| Configuration                           | Single          |       |

### ORDERING INFORMATION

|                                 |               |
|---------------------------------|---------------|
| Package                         | DPAK (TO-252) |
| Lead (Pb)-free and halogen-free | SiHD9N60E-GE3 |

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


| PARAMETER   | SYMBOL           | LIMIT          | UNIT |
|---|------------------|----------------|------|
| Drain-source voltage                                      | $V_{DS}$         | 600            | V    |
| Gate-source voltage                                       | $V_{GS}$         | $\pm 30$       |      |
| Continuous drain current ( $T_J = 150$ °C)                | $V_{GS}$ at 10 V | $T_C = 25$ °C  | A    |
|   |                  | $T_C = 100$ °C |      |
| Pulsed drain current <sup>a</sup>                         | $I_{DM}$         | 22             |      |
| Linear derating factor                                    |                  | 0.63           | W/°C |
| Single pulse avalanche energy <sup>b</sup>                | $E_{AS}$         | 111            | mJ   |
| Maximum power dissipation                                 | $P_D$            | 78             | W    |
| Operating junction and storage temperature range          | $T_J, T_{stg}$   | -55 to +150    | °C   |
| Drain-source voltage slope                                | $dV/dt$          | $T_J = 125$ °C | V/ns |
| Reverse diode $dV/dt$ <sup>d</sup>                        |                  | 40             |      |
| Soldering recommendations (peak temperature) <sup>c</sup> | For 10 s         | 300            | °C   |

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.8$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.



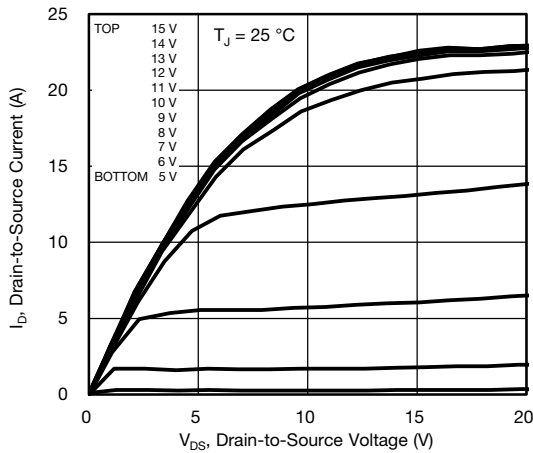
| THERMAL RESISTANCE RATINGS       |                   |      |      |      |
|----------------------------------|-------------------|------|------|------|
| PARAMETER                        | SYMBOL            | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient      | R <sub>thJA</sub> | -    | 62   | °C/W |
| Maximum Junction-to-Case (Drain) | R <sub>thJC</sub> | -    | 1.6  |      |

| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                                  |   |   |      |       |       |      |
|---|----------------------------------|---|---|------|-------|-------|------|
| PARAMETER   | SYMBOL                           | TEST CONDITIONS   |   | MIN. | TYP.  | MAX.  | UNIT |
| <b>Static</b>   |                                  |   |   |      |       |       |      |
| Drain-source breakdown voltage                                  | V <sub>DS</sub>                  | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA  |   | 600  | -     | -     | V    |
| V <sub>DS</sub> temperature coefficient                         | ΔV <sub>DS</sub> /T <sub>J</sub> | Reference to 25 °C, I <sub>D</sub> = 1 mA   |   | -    | 0.71  | -     | V/°C |
| Gate-source threshold voltage (N)                               | V <sub>GS(th)</sub>              | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA   |   | 2.5  | -     | 4.5   | V    |
| Gate-source leakage   | I <sub>GSS</sub>                 | V <sub>GS</sub> = ± 20 V  |   | -    | -     | ± 100 | nA   |
|   |                                  | V <sub>GS</sub> = ± 30 V  |   | -    | -     | ± 1   | μA   |
| Zero gate voltage drain current                                 | I <sub>DSS</sub>                 | V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V  |   | -    | -     | 1     | μA   |
|   |                                  | V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C   |   | -    | -     | 10    |      |
| Drain-source on-state resistance                                | R <sub>DS(on)</sub>              | V <sub>GS</sub> = 10 V  | I <sub>D</sub> = 4.5 A                          | -    | 0.320 | 0.368 | Ω    |
| Forward Transconductance  | g <sub>fs</sub>                  | V <sub>DS</sub> = 30 V, I <sub>D</sub> = 4.5 A  |   | -    | 2.4   | -     | S    |
| <b>Dynamic</b>  |                                  |   |   |      |       |       |      |
| Input capacitance   | C <sub>iss</sub>                 | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 100 V,<br>f = 1 MHz   |   | -    | 778   | -     | pF   |
| Output capacitance  | C <sub>oss</sub>                 |   |   | -    | 48    | -     |      |
| Reverse transfer capacitance                                    | C <sub>rss</sub>                 |   |   | -    | 4     | -     |      |
| Effective output capacitance, energy related <sup>a</sup>       | C <sub>o(er)</sub>               |   |   | -    | 29    | -     |      |
| Effective output capacitance, time related <sup>b</sup>         | C <sub>o(tr)</sub>               | V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V   |   | -    | 138   | -     |      |
| Total gate charge   | Q <sub>g</sub>                   | V <sub>GS</sub> = 10 V  | I <sub>D</sub> = 4.5 A, V <sub>DS</sub> = 480 V | -    | 26    | 52    | nC   |
| Gate-source charge  | Q <sub>gs</sub>                  |   |   | -    | 6     | -     |      |
| Gate-drain charge   | Q <sub>gd</sub>                  |   |   | -    | 13    | -     |      |
| Turn-on delay time  | t <sub>d(on)</sub>               | V <sub>DD</sub> = 480 V, I <sub>D</sub> = 4.5 A,<br>V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω  |   | -    | 14    | 28    | ns   |
| Rise time   | t <sub>r</sub>                   |   |   | -    | 13    | 26    |      |
| Turn-off delay time   | t <sub>d(off)</sub>              |   |   | -    | 31    | 62    |      |
| Fall time   | t <sub>f</sub>                   |   |   | -    | 12    | 24    |      |
| Gate input resistance   | R <sub>g</sub>                   | f = 1 MHz, open drain   |   | 0.4  | 1.2   | 2.4   | Ω    |
| <b>Drain-Source Body Diode Characteristics</b>                  |                                  |   |   |      |       |       |      |
| Continuous source-drain diode current                           | I <sub>S</sub>                   | MOSFET symbol showing the integral reverse p - n junction diode  |   | -    | -     | 9     | A    |
| Pulsed diode forward current                                    | I <sub>SM</sub>                  |   |   | -    | -     | 22    |      |
| Diode forward voltage   | V <sub>SD</sub>                  | T <sub>J</sub> = 25 °C, I <sub>S</sub> = 4.5 A, V <sub>GS</sub> = 0 V   |   | -    | -     | 1.2   | V    |
| Reverse recovery time   | t <sub>rr</sub>                  | T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 4.5 A,<br>dI/dt = 100 A/μs, V <sub>R</sub> = 25 V   |   | -    | 207   | 414   | ns   |
| Reverse recovery charge   | Q <sub>rr</sub>                  |   |   | -    | 2.2   | 4.4   | μC   |
| Reverse recovery current  | I <sub>RRM</sub>                 |   |   | -    | 20    | -     | A    |

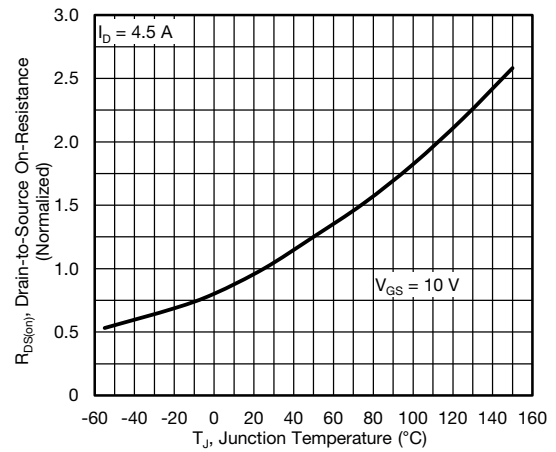
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>.
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>.

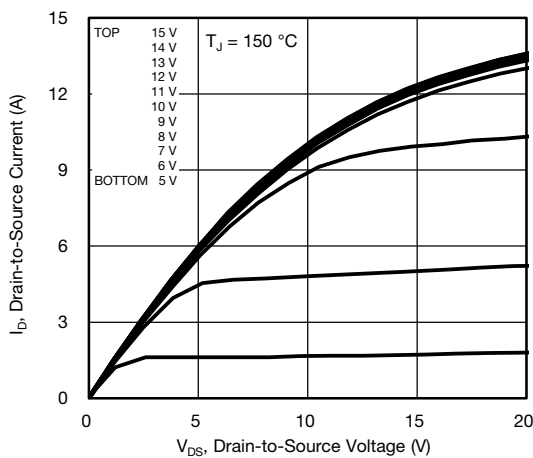
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



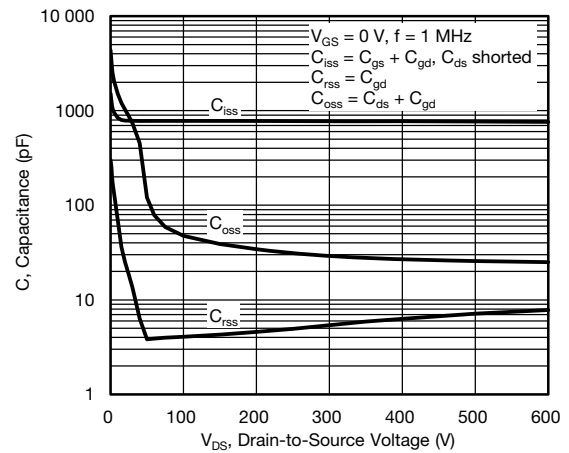
**Fig. 1 - Typical Output Characteristics**



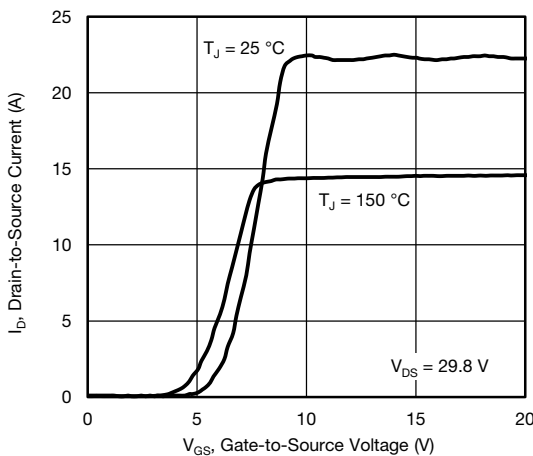
**Fig. 4 - Normalized On-Resistance vs. Temperature**



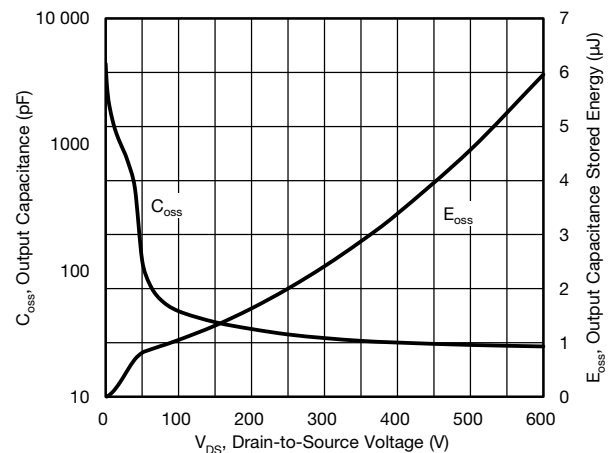
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

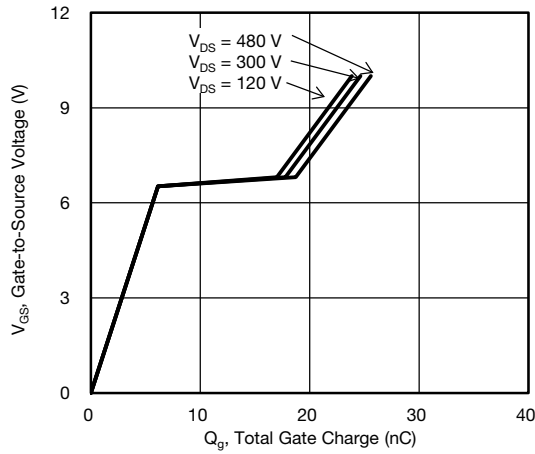


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

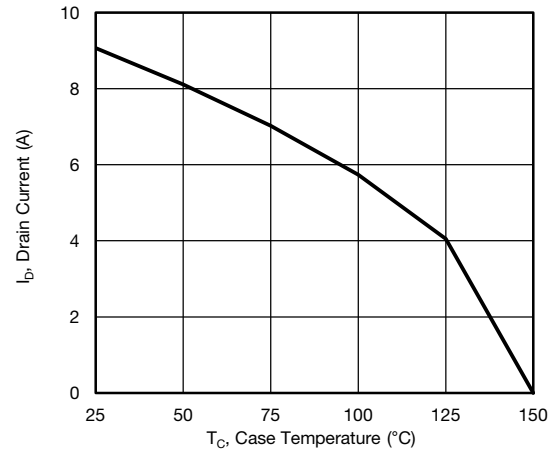


Fig. 10 - Maximum Drain Current vs. Case Temperature

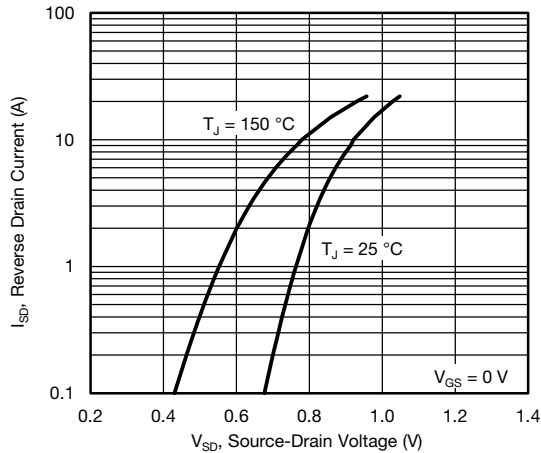


Fig. 8 - Typical Source-Drain Diode Forward Voltage

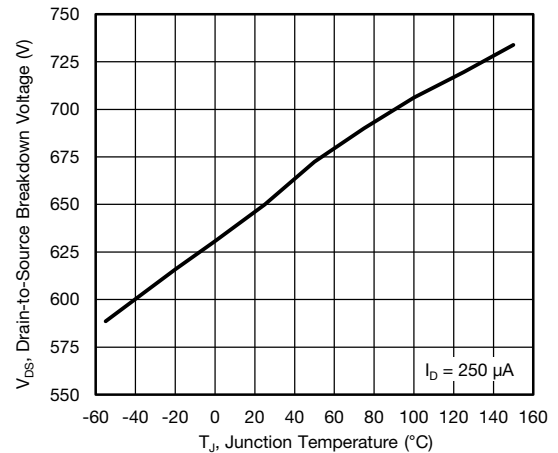


Fig. 11 - Temperature vs. Drain-to-Source Voltage

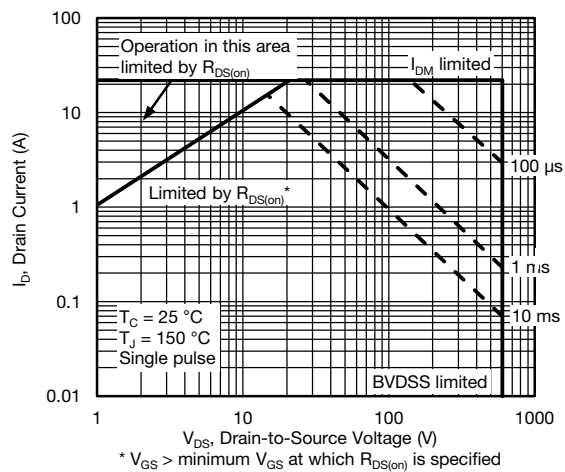


Fig. 9 - Maximum Safe Operating Area

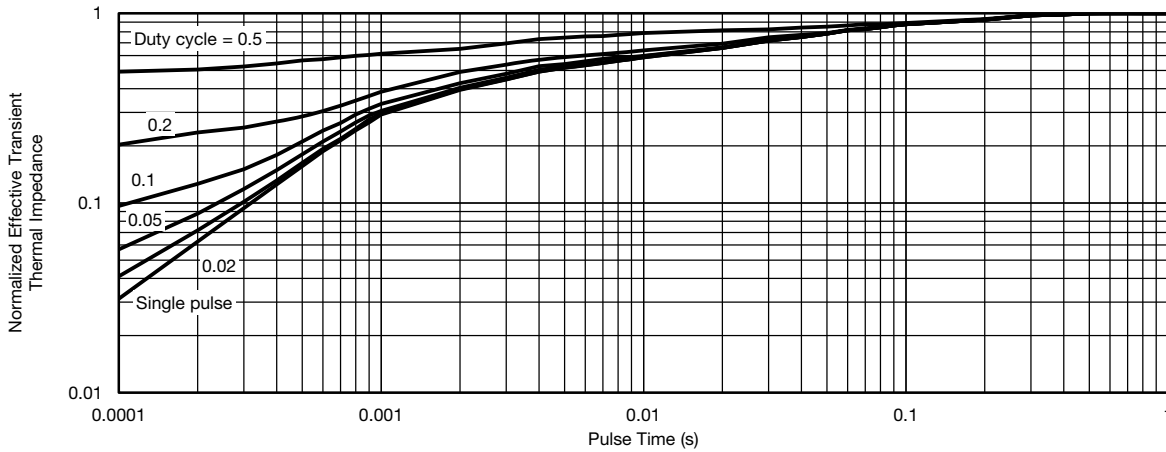


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

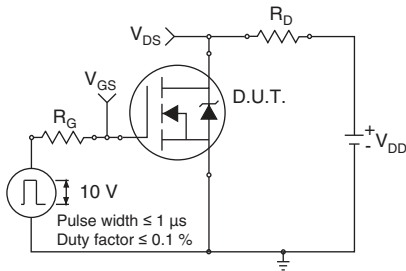


Fig. 13 - Switching Time Test Circuit

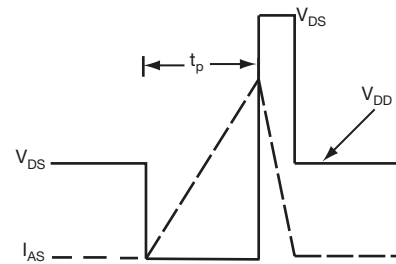


Fig. 16 - Unclamped Inductive Waveforms

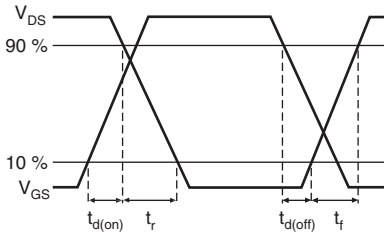


Fig. 14 - Switching Time Waveforms

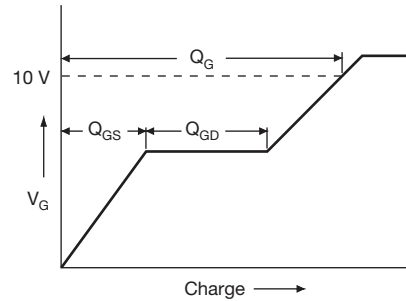


Fig. 17 - Basic Gate Charge Waveform

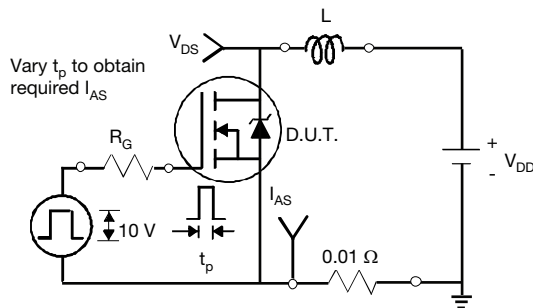


Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 19 - For N-Channel

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## TO-252AA (HIGH VOLTAGE)



| DIM. | MILLIMETERS |       | INCHES    |       |
|------|-------------|-------|-----------|-------|
|      | MIN.        | MAX.  | MIN.      | MAX.  |
| E    | 6.40        | 6.73  | 0.252     | 0.265 |
| L    | 1.40        | 1.77  | 0.055     | 0.070 |
| L1   | 2.743 REF   |       | 0.108 REF |       |
| L2   | 0.508 BSC   |       | 0.020 BSC |       |
| L3   | 0.89        | 1.27  | 0.035     | 0.050 |
| L4   | 0.64        | 1.01  | 0.025     | 0.040 |
| D    | 6.00        | 6.22  | 0.236     | 0.245 |
| H    | 9.40        | 10.40 | 0.370     | 0.409 |
| b    | 0.64        | 0.88  | 0.025     | 0.035 |
| b2   | 0.77        | 1.14  | 0.030     | 0.045 |
| b3   | 5.21        | 5.46  | 0.205     | 0.215 |
| e    | 2.286 BSC   |       | 0.090 BSC |       |
| A    | 2.20        | 2.38  | 0.087     | 0.094 |
| A1   | 0.00        | 0.13  | 0.000     | 0.005 |
| c    | 0.45        | 0.60  | 0.018     | 0.024 |
| c2   | 0.45        | 0.58  | 0.018     | 0.023 |
| D1   | 5.30        | -     | 0.209     | -     |
| E1   | 4.40        | -     | 0.173     | -     |
| θ    | 0'          | 10'   | 0'        | 10'   |

ECN: S-81965-Rev. A, 15-Sep-08  
 DWG: 5973

### Notes

1. Package body sizes exclude mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)





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