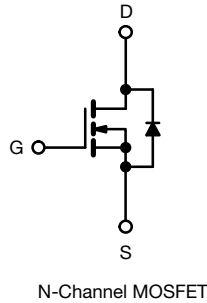


## D Series Power MOSFET

**TO-220 FULLPAK**


### FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance ( $C_{iss}$ )
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM):  $R_{on} \times Q_g$
  - Fast switching
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

### APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers

| PRODUCT SUMMARY                         |                       |
|---|-----------------------|
| $V_{DS}$ (V) at $T_J$ max.              | 450                   |
| $R_{DS(on)}$ max. ( $\Omega$ ) at 25 °C | $V_{GS} = 10$ V   1.0 |
| $Q_g$ max. (nC)                         | 18                    |
| $Q_{gs}$ (nC)                           | 3                     |
| $Q_{gd}$ (nC)                           | 4                     |
| Configuration                           | Single                |

| ORDERING INFORMATION |                |
|----------------------|----------------|
| Package              | TO-220 FULLPAK |
| Lead (Pb)-free       | SiHF6N40D-E3   |


| ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted) |                  |                |      |
|---|------------------|----------------|------|
| PARAMETER   | SYMBOL           | LIMIT          | UNIT |
| Drain-Source Voltage  | $V_{DS}$         | 400            | V    |
| Gate-Source Voltage   | $V_{GS}$         | $\pm 30$       |      |
| Gate-Source Voltage AC ( $f > 1$ Hz)                              |                  | 30             |      |
| Continuous Drain Current ( $T_J = 150$ °C) <sup>e</sup>           | $V_{GS}$ at 10 V | $T_C = 25$ °C  | A    |
|   |                  | $T_C = 100$ °C |      |
| Pulsed Drain Current <sup>a</sup>                                 | $I_{DM}$         | 13             |      |
| Linear Derating Factor  |                  | 0.24           | W/°C |
| Single Pulse Avalanche Energy <sup>b</sup>                        | $E_{AS}$         | 104            | mJ   |
| Maximum Power Dissipation   | $P_D$            | 30             | W    |
| Operating Junction and Storage Temperature Range                  | $T_J, T_{stg}$   | -55 to +150    | °C   |
| Drain-Source Voltage Slope  | $dV/dt$          | $T_J = 125$ °C | V/ns |
| Reverse Diode $dV/dt$ <sup>d</sup>                                |                  | 0.48           |      |
| Soldering Recommendations (Peak temperature) <sup>c</sup>         | For 10 s         | 300            | °C   |
| Mounting Torque   | M3 screw         | 0.6            | Nm   |

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 2.3$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 9.5$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ , starting  $T_J = 25$  °C.
- Limited by maximum junction temperature.



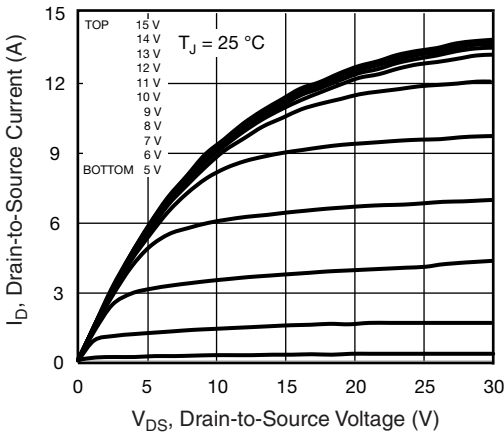
| THERMAL RESISTANCE RATINGS       |                   |      |      |      |
|----------------------------------|-------------------|------|------|------|
| PARAMETER                        | SYMBOL            | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient      | R <sub>thJA</sub> | -    | 65   | °C/W |
| Maximum Junction-to-Case (Drain) | R <sub>thJC</sub> | -    | 4.1  |      |

| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                                  |  |   |                       |      |       |      |
|---|----------------------------------|--|---|-----------------------|------|-------|------|
| PARAMETER   | SYMBOL                           | TEST CONDITIONS  |   | MIN.                  | TYP. | MAX.  | UNIT |
| <b>Static</b>   |                                  |  |   |                       |      |       |      |
| Drain-Source Breakdown Voltage                                  | V <sub>DS</sub>                  | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA   |   | 400                   | -    | -     | V    |
| V <sub>DS</sub> Temperature Coefficient                         | ΔV <sub>DS</sub> /T <sub>J</sub> | Reference to 25 °C, I <sub>D</sub> = 250 μA  |   | -                     | 0.53 | -     | V/°C |
| Gate-Source Threshold Voltage (N)                               | V <sub>GS(th)</sub>              | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA  |   | 3                     | -    | 5     | V    |
| Gate-Source Leakage   | I <sub>GSS</sub>                 | V <sub>GS</sub> = ± 30 V   |   | -                     | -    | ± 100 | nA   |
| Zero Gate Voltage Drain Current                                 | I <sub>DSS</sub>                 | V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V   |   | -                     | -    | 1     | μA   |
|   |                                  | V <sub>DS</sub> = 320 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C  |   | -                     | -    | 10    |      |
| Drain-Source On-State Resistance                                | R <sub>DS(on)</sub>              | V <sub>GS</sub> = 10 V   | I <sub>D</sub> = 3 A                          | -                     | 0.85 | 1.0   | Ω    |
| Forward Transconductance  | g <sub>fs</sub>                  | V <sub>DS</sub> = 50 V, I <sub>D</sub> = 3 A   |   | -                     | 1.7  | -     | S    |
| <b>Dynamic</b>  |                                  |  |   |                       |      |       |      |
| Input Capacitance   | C <sub>iss</sub>                 | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 100 V,<br>f = 1 MHz  |   | -                     | 311  | -     | pF   |
| Output Capacitance  | C <sub>oss</sub>                 |  |   | -                     | 38   | -     |      |
| Reverse Transfer Capacitance                                    | C <sub>rss</sub>                 |  |   | -                     | 7    | -     |      |
| Effective output capacitance, energy related <sup>a</sup>       | C <sub>o(er)</sub>               |  |   | -                     | 44   | -     |      |
| Effective output capacitance, time related <sup>b</sup>         | C <sub>o(tr)</sub>               | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 0 V to 320 V   |   | -                     | 54   | -     |      |
| Total Gate Charge   | Q <sub>g</sub>                   | V <sub>GS</sub> = 10 V   | I <sub>D</sub> = 3 A, V <sub>DS</sub> = 320 V | -                     | 9    | 18    | nC   |
| Gate-Source Charge  | Q <sub>gs</sub>                  |  |   | -                     | 3    | -     |      |
| Gate-Drain Charge   | Q <sub>gd</sub>                  |  |   | -                     | 4    | -     |      |
| Turn-On Delay Time  | t <sub>d(on)</sub>               | V <sub>DD</sub> = 400 V, I <sub>D</sub> = 3 A,<br>V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω   |   | -                     | 12   | 24    | ns   |
| Rise Time   | t <sub>r</sub>                   |  |   | -                     | 11   | 22    |      |
| Turn-Off Delay Time   | t <sub>d(off)</sub>              |  |   | -                     | 14   | 28    |      |
| Fall Time   | t <sub>f</sub>                   |  |   | -                     | 8    | 16    |      |
| Gate Input Resistance   | R <sub>g</sub>                   |  |   | f = 1 MHz, open drain |      | -     |      |
| <b>Drain-Source Body Diode Characteristics</b>                  |                                  |  |   |                       |      |       |      |
| Continuous Source-Drain Diode Current                           | I <sub>S</sub>                   | MOSFET symbol showing the integral reverse p - n junction diode<br> |   | -                     | -    | 6     | A    |
| Pulsed Diode Forward Current                                    | I <sub>SM</sub>                  |  |   | -                     | -    | 24    |      |
| Diode Forward Voltage   | V <sub>SD</sub>                  | T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3 A, V <sub>GS</sub> = 0 V  |   | -                     | -    | 1.2   | V    |
| Reverse Recovery Time   | t <sub>rr</sub>                  | T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 3 A,<br>di/dt = 100 A/μs, V <sub>R</sub> = 20 V  |   | -                     | 236  | -     | ns   |
| Reverse Recovery Charge   | Q <sub>rr</sub>                  |  |   | -                     | 1.1  | -     | μC   |
| Reverse Recovery Current  | I <sub>RRM</sub>                 |  |   | -                     | 9    | -     | A    |

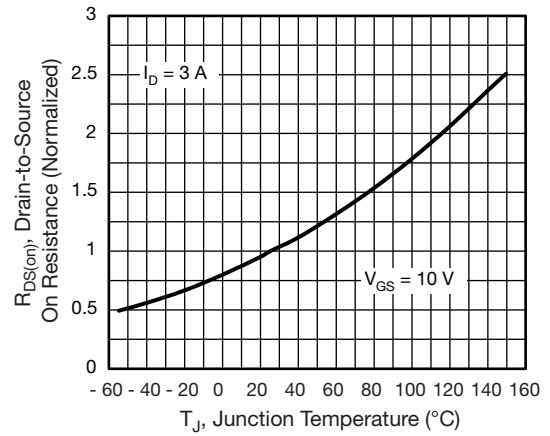
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DS</sub>.
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DS</sub>.

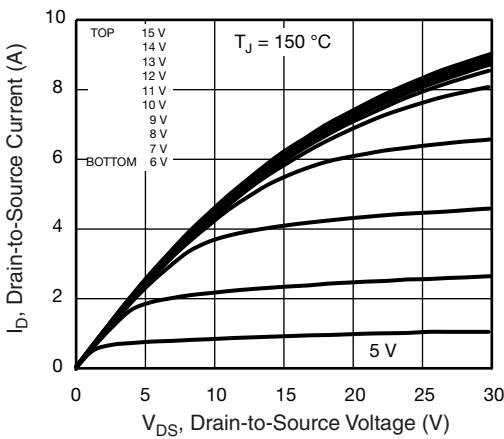
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



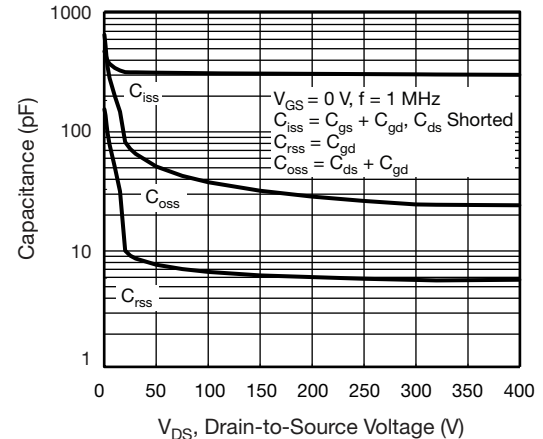
**Fig. 1 - Typical Output Characteristics**



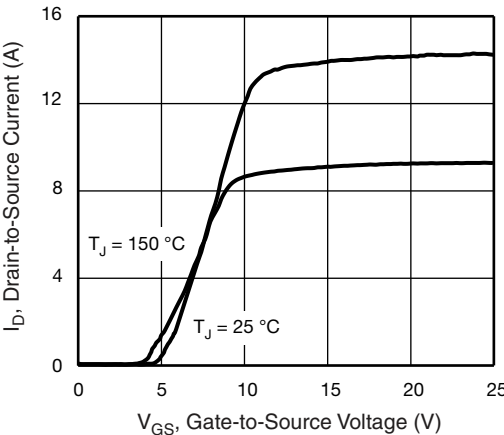
**Fig. 4 - Normalized On-Resistance vs. Temperature**



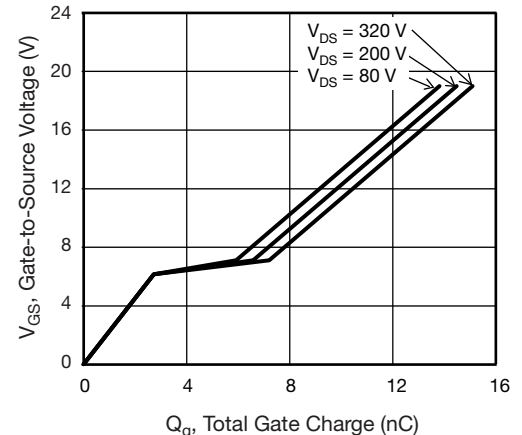
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

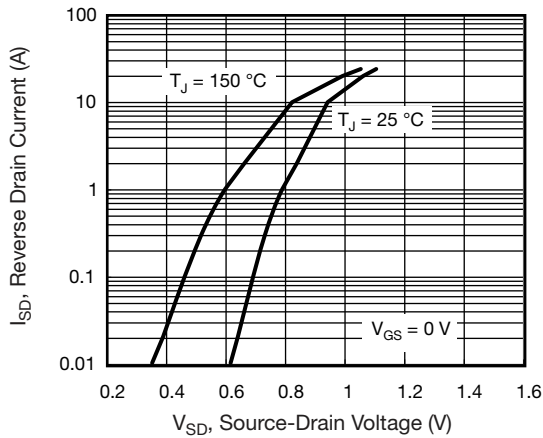


Fig. 7 - Typical Source-Drain Diode Forward Voltage

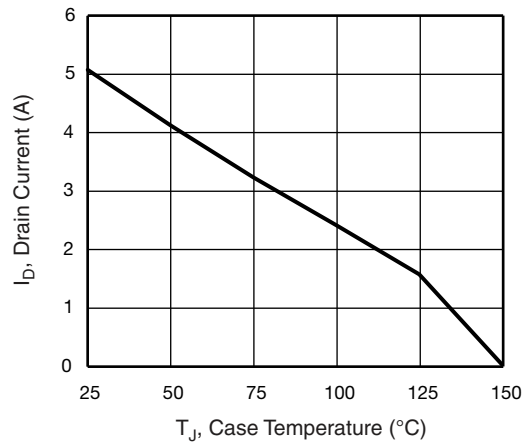


Fig. 9 - Maximum Drain Current vs. Case Temperature

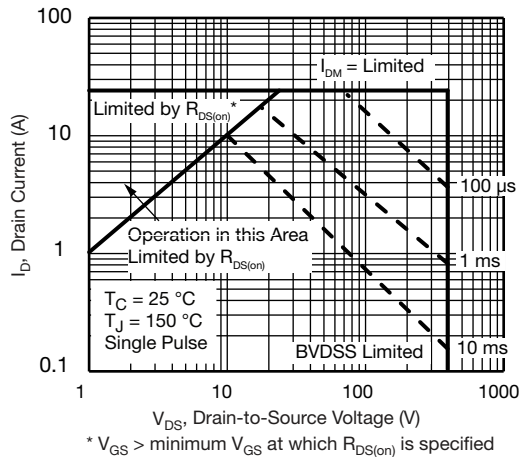


Fig. 8 - Maximum Safe Operating Area

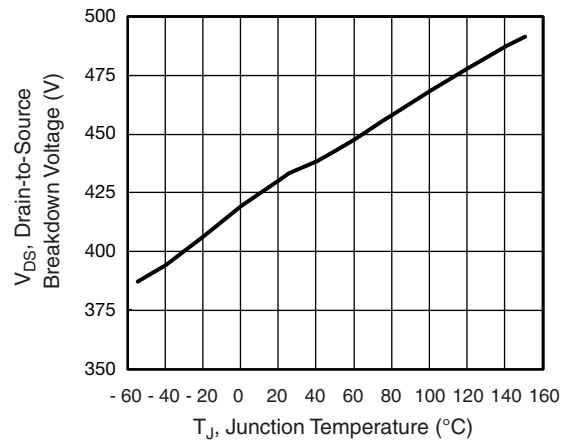


Fig. 10 - Temperature vs. Drain-to-Source Voltage

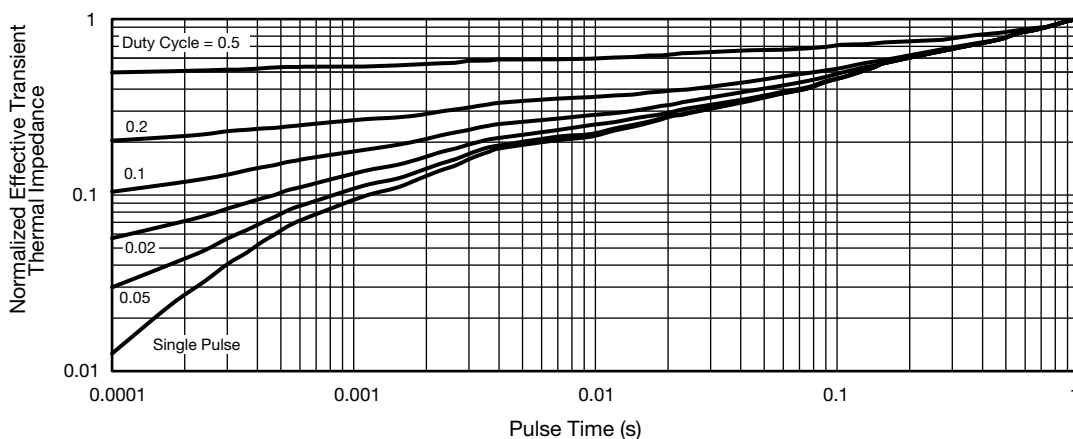


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 12 - Switching Time Test Circuit



Fig. 16 - Basic Gate Charge Waveform



Fig. 13 - Switching Time Waveforms



Fig. 17 - Gate Charge Test Circuit

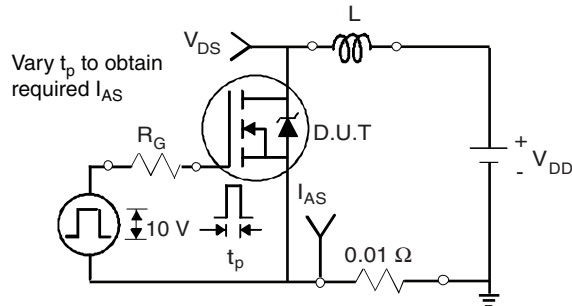


Fig. 14 - Unclamped Inductive Test Circuit

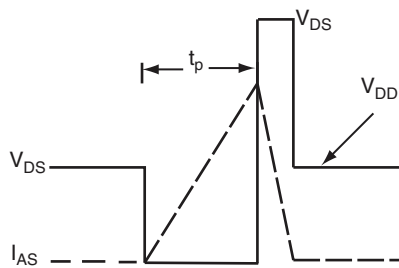


Fig. 15 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 18 - For N-Channel

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# TO-220 FULLPAK (High Voltage)

## OPTION 1: FACILITY CODE = 9



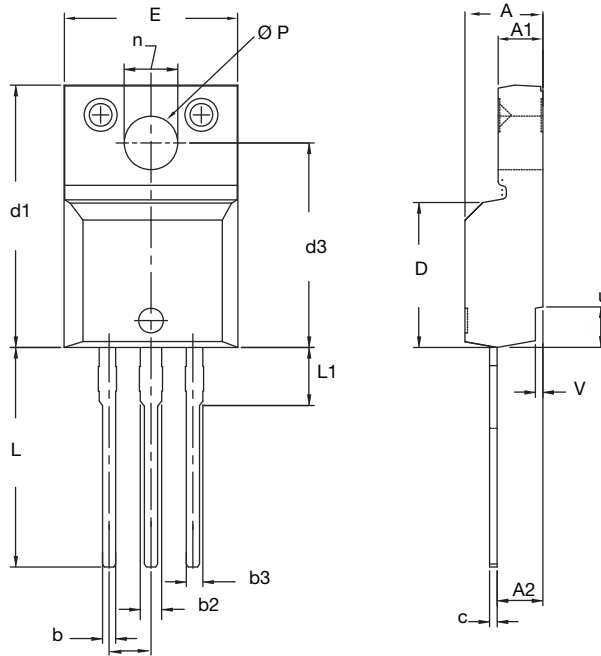
| DIM.            | MILLIMETERS |       |       |
|-----------------|-------------|-------|-------|
|                 | MIN.        | NOM.  | MAX.  |
| A               | 4.60        | 4.70  | 4.80  |
| b               | 0.70        | 0.80  | 0.91  |
| b1              | 1.20        | 1.30  | 1.47  |
| b2              | 1.10        | 1.20  | 1.30  |
| C               | 0.45        | 0.50  | 0.63  |
| D               | 15.80       | 15.87 | 15.97 |
| e               | 2.54 BSC    |       |       |
| E               | 10.00       | 10.10 | 10.30 |
| F               | 2.44        | 2.54  | 2.64  |
| G               | 6.50        | 6.70  | 6.90  |
| L               | 12.90       | 13.10 | 13.30 |
| L1              | 3.13        | 3.23  | 3.33  |
| Q               | 2.65        | 2.75  | 2.85  |
| Q1              | 3.20        | 3.30  | 3.40  |
| $\varnothing R$ | 3.08        | 3.18  | 3.28  |

### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking



**OPTION 2: FACILITY CODE = Y**



| DIM. | MILLIMETERS |        | INCHES    |       |
|------|-------------|--------|-----------|-------|
|      | MIN.        | MAX.   | MIN.      | MAX.  |
| A    | 4.570       | 4.830  | 0.180     | 0.190 |
| A1   | 2.570       | 2.830  | 0.101     | 0.111 |
| A2   | 2.510       | 2.850  | 0.099     | 0.112 |
| b    | 0.622       | 0.890  | 0.024     | 0.035 |
| b2   | 1.229       | 1.400  | 0.048     | 0.055 |
| b3   | 1.229       | 1.400  | 0.048     | 0.055 |
| c    | 0.440       | 0.629  | 0.017     | 0.025 |
| D    | 8.650       | 9.800  | 0.341     | 0.386 |
| d1   | 15.88       | 16.120 | 0.622     | 0.635 |
| d3   | 12.300      | 12.920 | 0.484     | 0.509 |
| E    | 10.360      | 10.630 | 0.408     | 0.419 |
| e    | 2.54 BSC    |        | 0.100 BSC |       |
| L    | 13.200      | 13.730 | 0.520     | 0.541 |
| L1   | 3.100       | 3.500  | 0.122     | 0.138 |
| n    | 6.050       | 6.150  | 0.238     | 0.242 |
| Ø P  | 3.050       | 3.450  | 0.120     | 0.136 |
| u    | 2.400       | 2.500  | 0.094     | 0.098 |
| v    | 0.400       | 0.500  | 0.016     | 0.020 |

ECN: E19-0180-Rev. D, 08-Apr-2019  
 DWG: 5972

**Notes**

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking





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