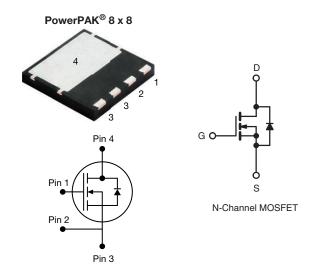
Vishay Siliconix

HALOGEN FREE

E Series Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V) at T _J max.	650				
R _{DS(on)} typ. (Ω) at 25 °C	V _{GS} = 10 V 0.153				
Q _g max. (nC)	83				
Q _{gs} (nC)	11				
Q _{gd} (nC)	20				
Configuration	Single				



FEATURES

- Fully lead (Pb)-free device
- Low figure-of-merit (FOM) R_{on} x Q_a
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Ultra low gate charge (Q_q)
- Avalanche energy rated (UIS)
- · Kelvin connection for reduced gate noise
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK 8 x 8
Lead (Pb)-free and Halogen-free	SiHH21N60E-T1-GE3

ABSOLUTE MAXIMUM RATINGS	T _C = 25 °C, un	less otherwis	se noted)		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	600	V
Gate-Source Voltage		V_{GS}	± 30	7 v	
Continuous Prain Current (T = 150 °C)	V _{GS} at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	- I _D	20	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 100 °C		12	Α
Pulsed Drain Current ^a			I _{DM}	48	
Linear Derating Factor				1.4	W/°C
Single Pulse Avalanche Energy b			E _{AS}	226	mJ
Maximum Power Dissipation			P_{D}	104	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope T _J = 125 °C			dV/dt	70	V/ns
Reverse Diode dV/dt ^c				29) v/ns

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 4 A.
- c. $I_{SD} \le I_D$, dI/dt = 100 A/ μ s, starting $T_J = 25$ °C.



Vishay Siliconix

THERMAL RESISTANCE RATINGS							
PARAMETER SYMBOL TYP. MAX. UNIT							
Maximum Junction-to-Ambient	R _{thJA}	40	52	°C/W			
Maximum Junction-to-Case (Drain)	R _{thJC}	0.55	0.72				

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	= 0 V, I _D = 250 μA	600	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.64	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = 250 μA	2	-	4	V
Cata Sauraa Laakaaa	I _{GSS}	,	V _{GS} = ± 20 V		-	± 100	nA
Gate-Source Leakage		,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
Zava Cata Valtaga Dvaia Cuwant		V _{DS} =	600 V, V _{GS} = 0 V	-	-	1	_
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 480 V	, V _{GS} = 0 V, T _J = 125 °C	-	-	50	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 11 A	-	0.153	0.176	Ω
Forward Transconductance	9 _{fs}	V _{DS}	= 30 V, I _D = 11 A	-	8.1	-	S
Dynamic				•			
Input Capacitance	C _{iss}		$V_{GS} = 0 V$	-	2015	-	
Output Capacitance	C _{oss}	,	$V_{DS} = 100 \text{ V},$	_	93	-	
Reverse Transfer Capacitance	C_{rss}		f = 1 MHz	_	6	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	- V _{DS} = 0 V to 480 V, V _{GS} = 0 V		-	60	-	pF -
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	254	-	
Total Gate Charge	Qq			-	55	83	
Gate-Source Charge	Q _{gs}	$V_{GS} = 10 \text{ V}$ $I_D = 11 \text{ A}, V_{DS} = 480 \text{ V}$		-	11	-	nC
Gate-Drain Charge	Q _{qd}			-	20	-	
Turn-On Delay Time	t _{d(on)}			-	20	40	
Rise Time	t _r	V _{DD} = 480 V, I _D = 11 A,		-	32	68	1 _
Turn-Off Delay Time	t _{d(off)}		$= 10 \text{ V}, \text{ R}_{\text{g}} = 9.1 \Omega$	-	68	102	ns -
Fall Time	t _f			_	45	90	
Gate Input Resistance	R_g	f = 1	f = 1 MHz, open drain		0.6	1.3	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET sym showing the		-	-	20	
Pulsed Diode Forward Current	I _{SM}	integral reverse p - n junction diode		-	-	48	A
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 11 A, V _{GS} = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t _{rr}			-	297	594	ns
Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = I_S = 11 \text{A},$ $dI/dt = 100 \text{A/}\mu\text{s}, V_R = 25 \text{V}$		-	4.2	8.4	μC
Reverse Recovery Current	I _{RRM}			_	26	 _	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

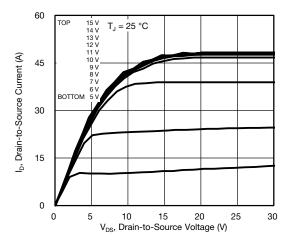


Fig. 1 - Typical Output Characteristics

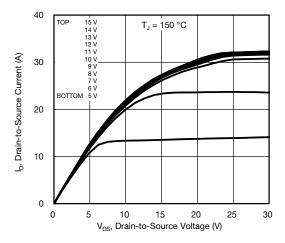


Fig. 2 - Typical Output Characteristics

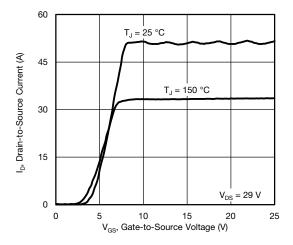


Fig. 3 - Typical Transfer Characteristics

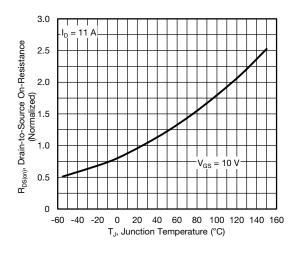


Fig. 4 - Normalized On-Resistance vs. Temperature

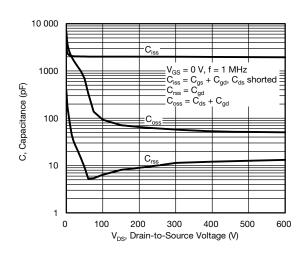


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

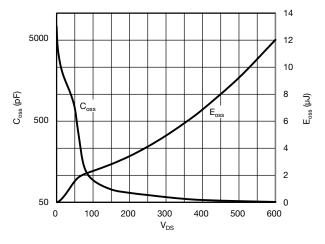


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}



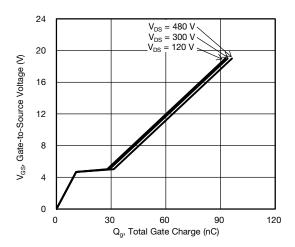


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

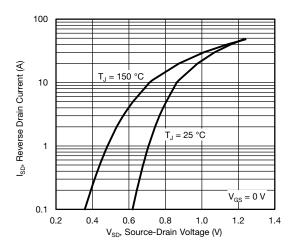


Fig. 8 - Typical Source-Drain Diode Forward Voltage

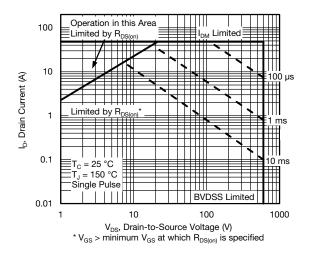


Fig. 9 - Maximum Safe Operating Area

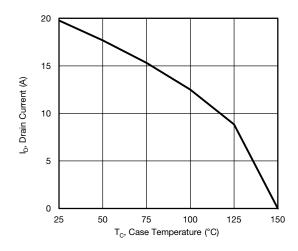


Fig. 10 - Maximum Drain Current vs. Case Temperature

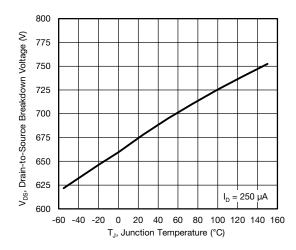


Fig. 11 - Temperature vs. Drain-to-Source Voltage



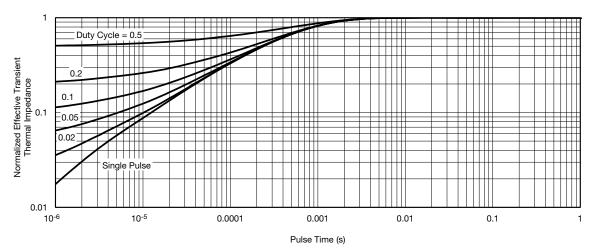


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

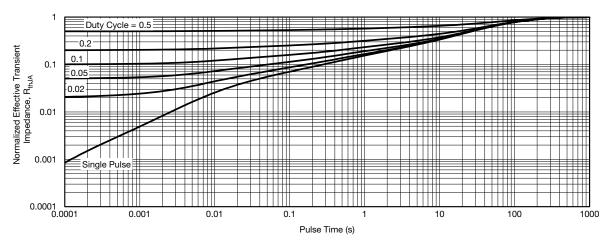


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

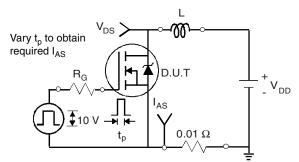


Fig. 14 - Switching Time Test Circuit

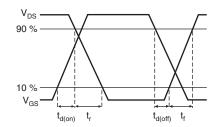


Fig. 15 - Switching Time Waveforms

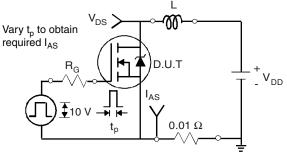


Fig. 16 - Unclamped Inductive Test Circuit

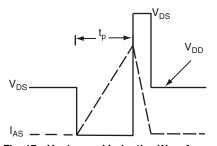


Fig. 17 - Unclamped Inductive Waveforms



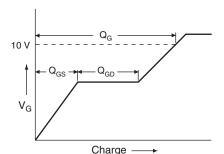


Fig. 18 - Basic Gate Charge Waveform

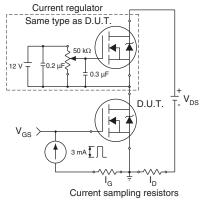
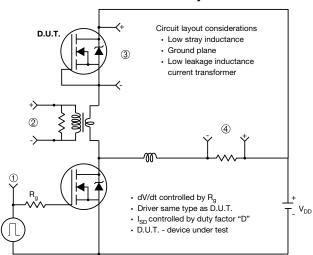


Fig. 19 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



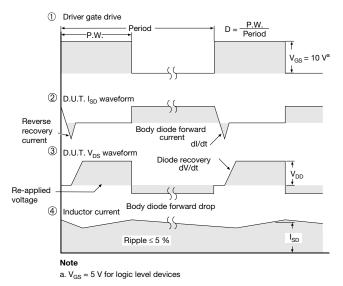


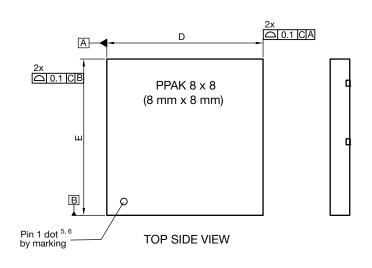
Fig. 20 - For N-Channel

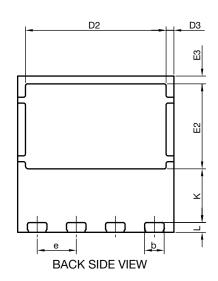
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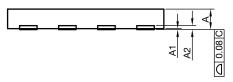


Vishay Siliconix

PowerPAK® 8 x 8 Case Outline







DIM.	MILLIMETERS			INCHES			
DIWI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.95	1.00	1.05	0.037	0.039	0.041	
A1	0.00	-	0.05	0.000	-	0.002	
A2	020 ref.			0.008 ref.			
b	0.95	1.00	1.05	0.037	0.039	0.041	
D	7.90	8.00	8.10	0.311	0.315	0.319	
D2	7.10	7.20	7.30	0.280	0.283	0.287	
D3	0.40 BSC			0.016 BSC			
е	2.00 BSC		0.079 BSC				
Е	7.90	8.00	8.10	0.311	0.315	0.319	
E2	4.30	4.35	4.40	0.169	0.171	0.173	
E3		0.40 BSC			0.016 BSC		
K	2.75 BSC		0.108 BSC				
L	0.45	0.50	0.55	0.018	0.020	0.022	
N ⁽³⁾	8			8 8			

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5 M 1994
- (3) N is the number of terminals
- (4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (5) Exact shape and size of this feature is optional

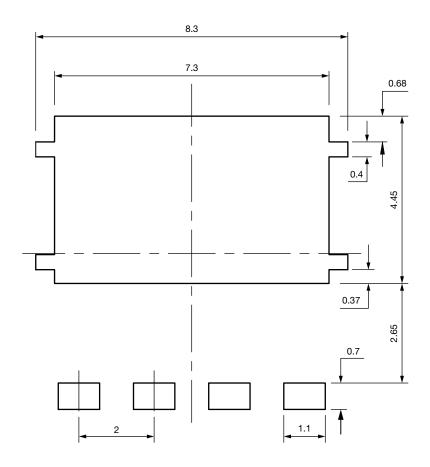
ECN: E20-0518-Rev. B, 28-Sep-2020

DWG: 6041

Revision: 28-Sep-2020 1 Document Number: 67859



Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm



Dimensions in millimeters



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