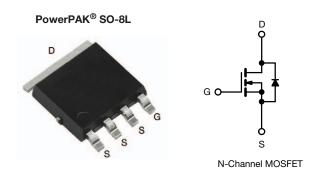


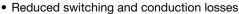
E Series Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	700			
R _{DS(on)} typ. (Ω) at 25 °C	V _{GS} = 10 V	0.755		
Q _g max. (nC)	32			
Q _{gs} (nC)	5			
Q _{gd} (nC)	7			
Configuration	Single			

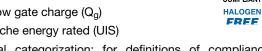


FEATURES

- Low figure-of-merit (FOM) Ron x Qa
- Low input capacitance (Ciss)



- Ultra low gate charge (Q_a)
- Avalanche energy rated (UIS)
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Consumer
 - Adaptors

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SiHJ6N65E-T1-GE3

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	650	V
Gate-Source Voltage			V_{GS}	± 30	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Continuous Drain Current (T _{.1} = 150 °C)	V _{GS} at 10 V	T _C = 25 °C		5.6	А
Continuous Drain Current (1) = 130 C)	VGS at 10 V	T _C = 100 °C	I _D	3.6	
Pulsed Drain Current ^a			I _{DM}	12	
Linear Derating Factor				0.76	W/°C
Single Pulse Avalanche Energy b			E _{AS}	36	mJ
Maximum Power Dissipation			P_{D}	74	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope T _J = 125 °C			dV/dt	70	V/ns
Reverse Diode dV/dt ^c	av/at	9.4] V/IIS		

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. $V_{DD} = 120 \text{ V}$, starting $T_J = 25 \,^{\circ}\text{C}$, $L = 28.2 \,\text{mH}$, $R_q = 25 \,\Omega$, $I_{AS} = 1.6 \,\text{A}$.
- c. $I_{SD} \le I_D$, $dI/dt = 100 \text{ A/}\mu\text{s}$, starting $T_J = 25 \,^{\circ}\text{C}$.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	52	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	1.2	1.7	C/ VV

Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static					•		
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		650	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.8	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Octo Course Lections	I _{GSS}	,	$V_{GS} = \pm 20 \text{ V}$		-	± 100	nA
Gate-Source Leakage		,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
Zara Cata Valtaga Drain Current		V _{DS} =	V _{DS} = 650 V, V _{GS} = 0 V		-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 520 V	, V _{GS} = 0 V, T _J = 125 °C	-	-	10	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	$I_D = 3 A$	-	0.755	0.868	Ω
Forward Transconductance	9 _{fs}	V _{DS}	= 30 V, I _D = 3 A	-	1.8	-	S
Dynamic							
Input Capacitance	C _{iss}		V _{GS} = 0 V,	-	596	-	
Output Capacitance	C _{oss}	Ī ,	$V_{\rm DS} = 100 \text{ V},$	-	35	-	
Reverse Transfer Capacitance	C _{rss}		f = 1 MHz	-	4	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 520 V, V _{GS} = 0 V		-	26	-	pF
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	90	-	
Total Gate Charge	Qg			-	16	32	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$I_D = 3 A, V_{DS} = 520 V$	-	5	-	nC
Gate-Drain Charge	Q _{gd}			-	7	-	
Turn-On Delay Time	t _{d(on)}			-	14	28	
Rise Time	t _r	$V_{DD} = 520 \text{ V}, I_D = 3 \text{ A},$		-	14	28	no
Turn-Off Delay Time	t _{d(off)}	V _{GS} =	$=$ 10 V, R _g = 9.1 Ω	-	25	50	ns
Fall Time	t _f	1		-	17	34	1
Gate Input Resistance	R _g	f = 1 MHz		0.4	0.8	1.6	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET sym showing the		-	-	5.6	
Pulsed Diode Forward Current	I _{SM}	integral reverse p - n junction diode		-	-	12	- A
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 3 A, V _{GS} = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t _{rr}			-	278	556	ns
Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = I_S = 3 \text{A},$ $\text{dI/dt} = 100 \text{A/µs}, V_R = 25 \text{V}$		_	2.1	4.2	μC
Reverse Recovery Current	I _{RRM}	ai/at =	100 A/μS ^{, *} R = 25 V	_	12	_	Α

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} . b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

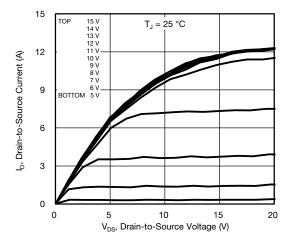


Fig. 1 - Typical Output Characteristics

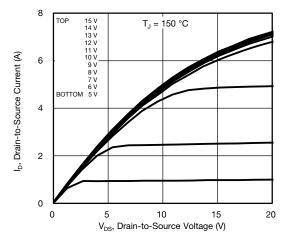


Fig. 2 - Typical Output Characteristics

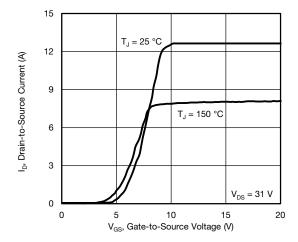


Fig. 3 - Typical Transfer Characteristics

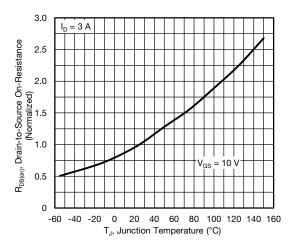


Fig. 4 - Normalized On-Resistance vs. Temperature

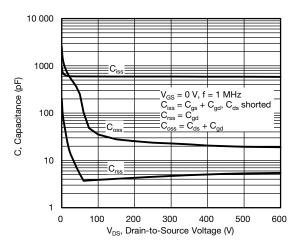


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

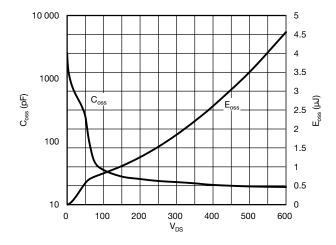


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}



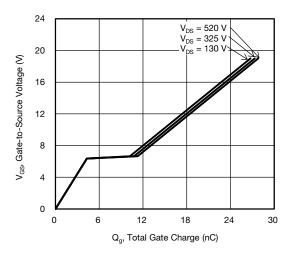


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

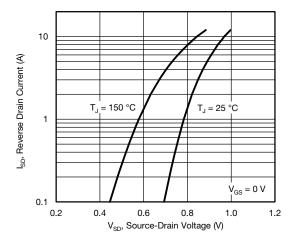


Fig. 8 - Typical Source-Drain Diode Forward Voltage

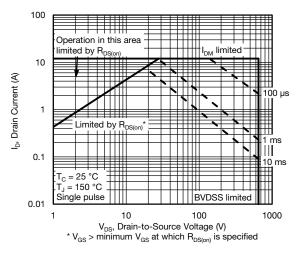


Fig. 9 - Maximum Safe Operating Area

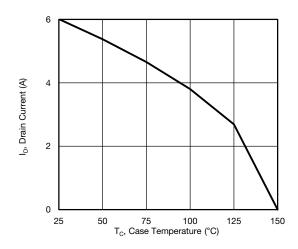


Fig. 10 - Maximum Drain Current vs. Case Temperature

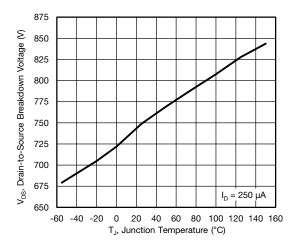


Fig. 11 - Temperature vs. Drain-to-Source Voltage



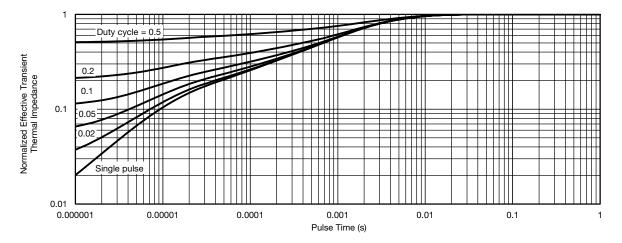


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

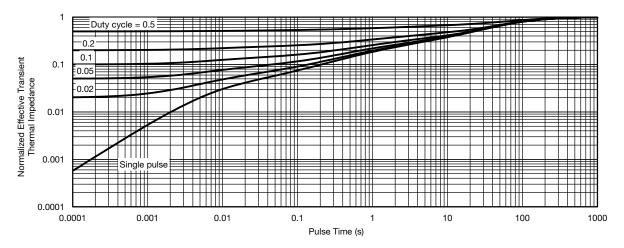


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

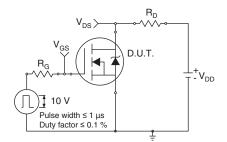


Fig. 14 - Switching Time Test Circuit

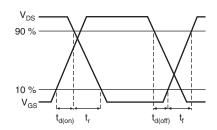


Fig. 15 - Switching Time Waveforms

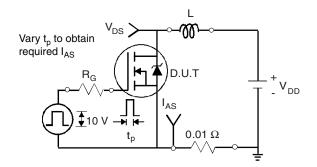


Fig. 16 - Unclamped Inductive Test Circuit

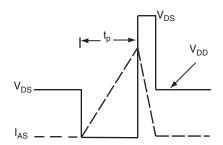


Fig. 17 - Unclamped Inductive Waveforms

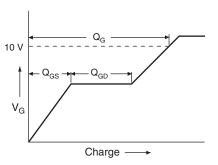


Fig. 18 - Basic Gate Charge Waveform

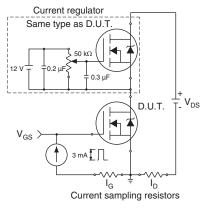
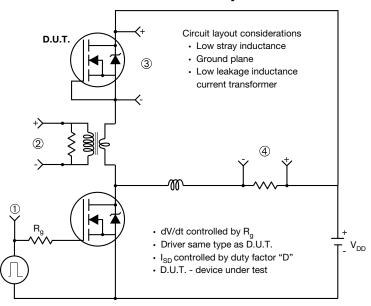


Fig. 19 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



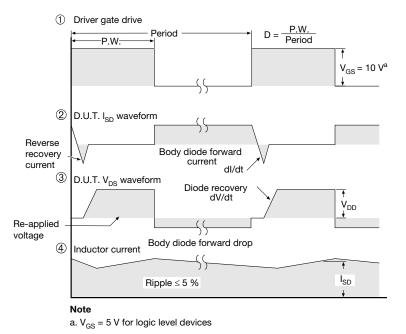


Fig. 20 - For N-Channel

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PowerPAK® SO-8L Case Outline 2



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DIM.	MILLIMETERS			INCHES		
DIN.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
А	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3		0.094		0.004		
b4		0.47			0.019	
С	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
е		1.27 BSC		0.050 BSC		
Е	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K		0.51		0.020		
W	0.23		0.009			
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°

ECN: C21-1498-Rev. C, 01-Nov-2021

DWG: 6044

Note

• Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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