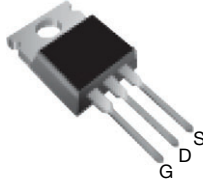


E Series Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	850	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.250
Q_g max. (nC)	62	
Q_{gs} (nC)	8	
Q_{gd} (nC)	18	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP17N80AE-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	800	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	15	A
		$T_C = 100$ °C	10	
Pulsed drain current ^a	I_{DM}	32		
Linear derating factor		1.4	W/°C	
Single pulse avalanche energy ^b	E_{AS}	127	mJ	
Maximum power dissipation	P_D	179	W	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Drain-source voltage slope	dv/dt	100	V/ns	
Reverse diode dv/dt ^d				
Soldering recommendations (peak temperature) ^c	For 10 s	260	°C	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 3$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 100$ A/ μ s, starting $T_J = 25$ °C



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	0.7	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		800	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.8	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2	-	4	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 800 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 640 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 8.5 A	-	0.250	0.290	Ω
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 8.5 A		-	7.1	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	1260	-	pF
Output capacitance	C _{oss}			-	56	-	
Reverse transfer capacitance	C _{rss}			-	5	-	
Effective output capacitance, energy related	C _{o(er)}	V _{DS} = 0 V to 480 V, V _{GS} = 0 V		-	40	-	pF
Effective output capacitance, time related	C _{o(tr)}			-	245	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 8.5 A, V _{DS} = 640 V	-	41	62	nC
Gate-source charge	Q _{gs}			-	8	-	
Gate-drain charge	Q _{gd}			-	18	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 640 V, I _D = 8.5 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	21	42	ns
Rise time	t _r			-	23	46	
Turn-off delay time	t _{d(off)}			-	45	90	
Fall time	t _f			-	31	62	
Gate input resistance	R _g	f = 1 MHz, open drain		0.2	0.5	1.1	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	15	A
Pulsed diode forward current	I _{SM}			-	-	32	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 8.5 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 8.5 A, di/dt = 100 A/μs, V _R = 25 V		-	314	628	ns
Reverse recovery charge	Q _{rr}			-	4	8	μC
Reverse recovery current	I _{RRM}			-	21	-	A

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

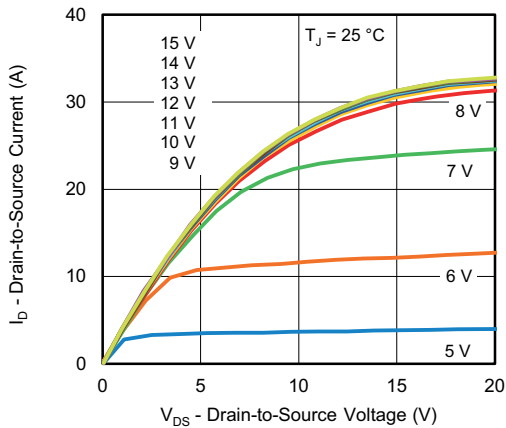


Fig. 1 - Typical Output Characteristics

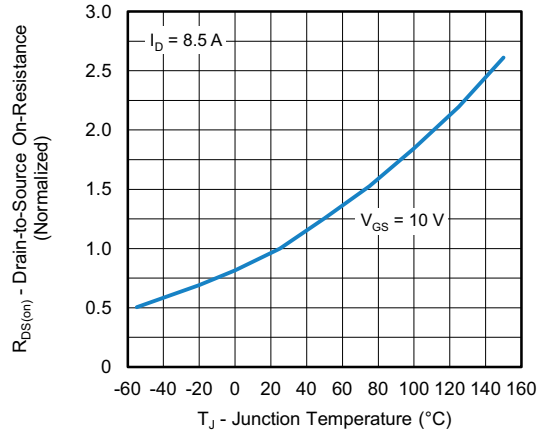


Fig. 4 - Normalized On-Resistance vs. Temperature

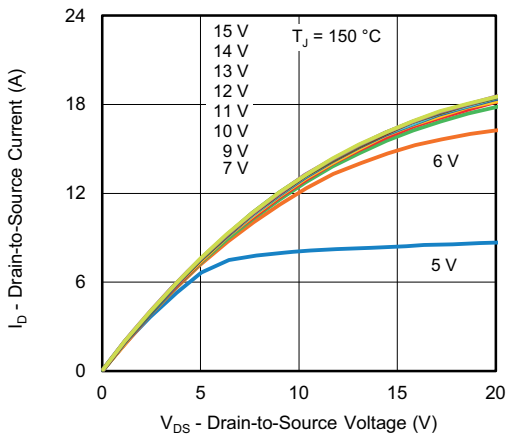


Fig. 2 - Typical Output Characteristics

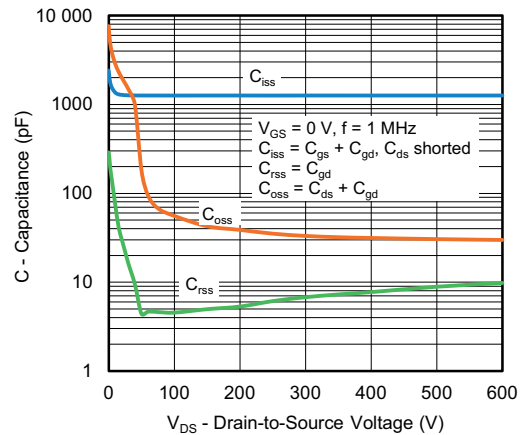


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

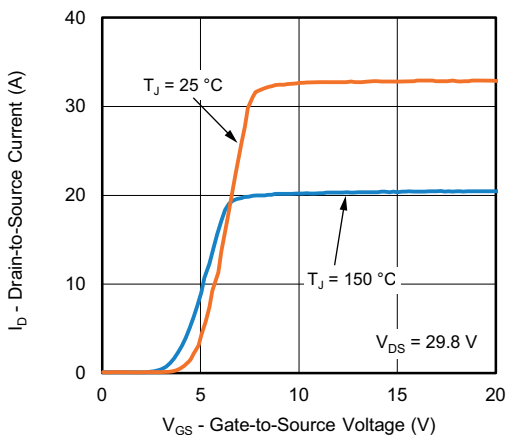


Fig. 3 - Typical Transfer Characteristics

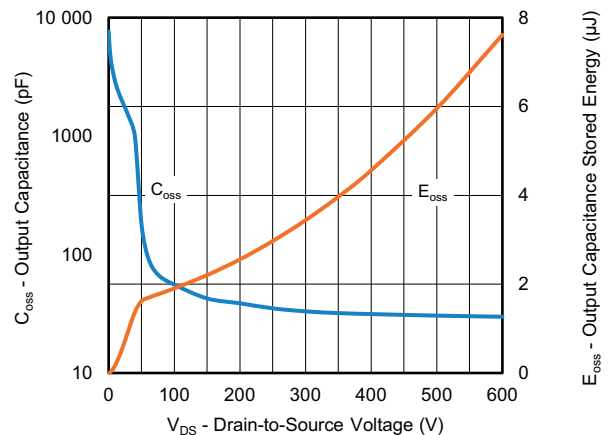


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

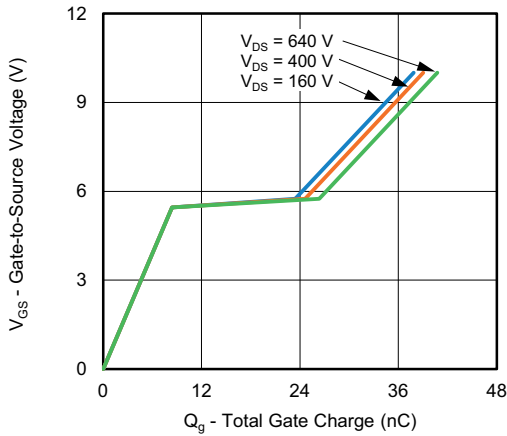


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

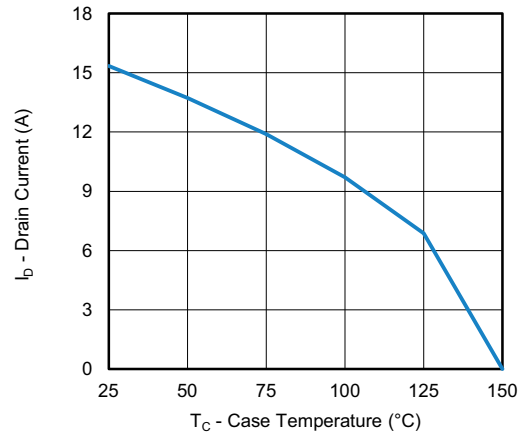


Fig. 10 - Maximum Drain Current vs. Case Temperature

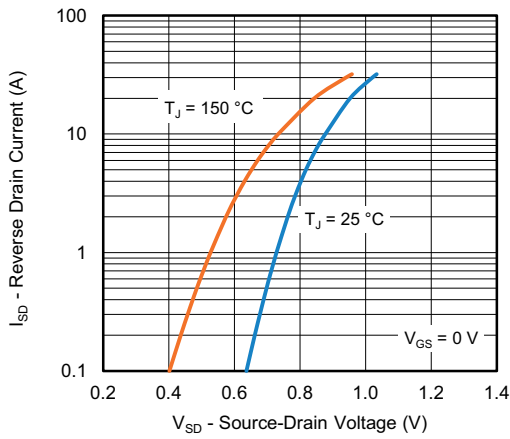


Fig. 8 - Typical Source-Drain Diode Forward Voltage

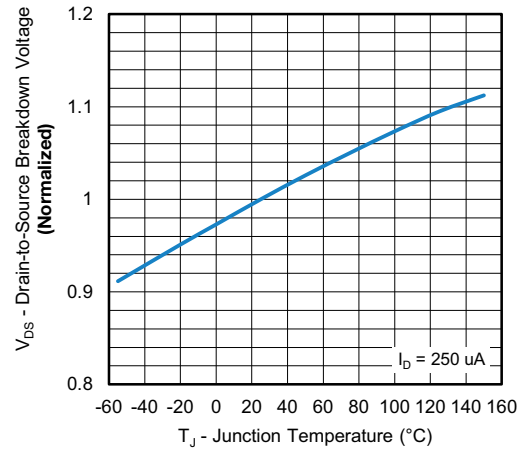


Fig. 11 - Temperature vs. Drain-to-Source Voltage

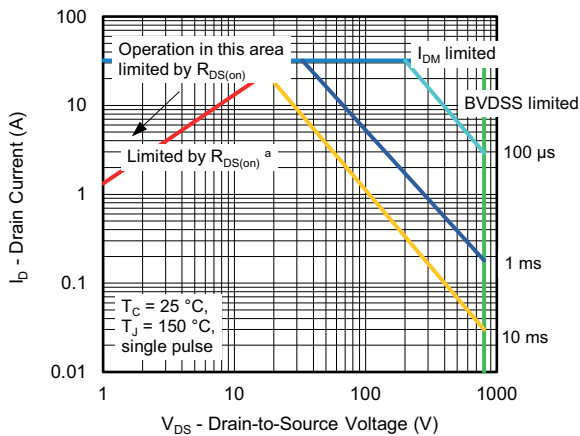


Fig. 9 - Maximum Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

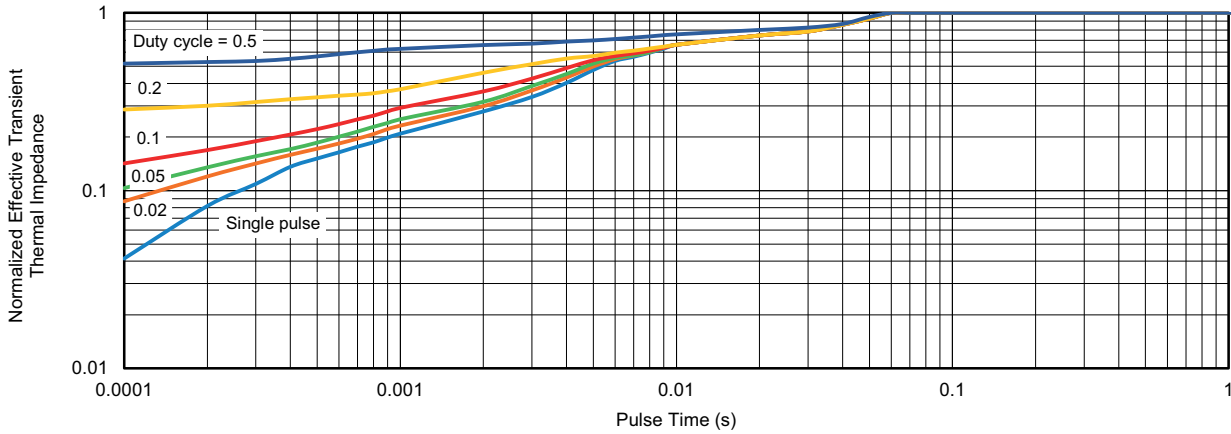


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

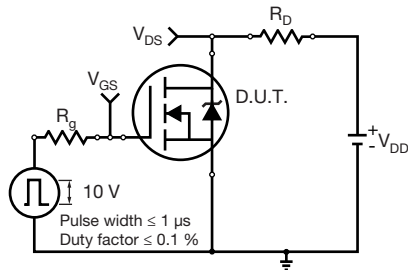


Fig. 13 - Switching Time Test Circuit

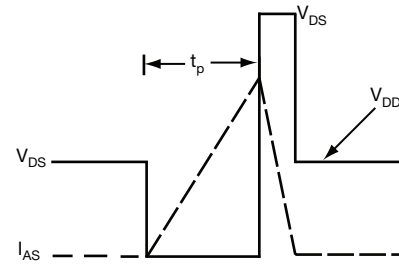


Fig. 16 - Unclamped Inductive Waveforms

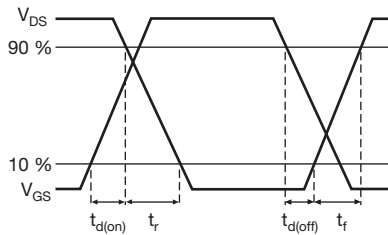


Fig. 14 - Switching Time Waveforms

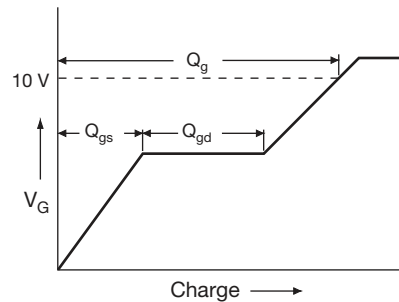


Fig. 17 - Basic Gate Charge Waveform

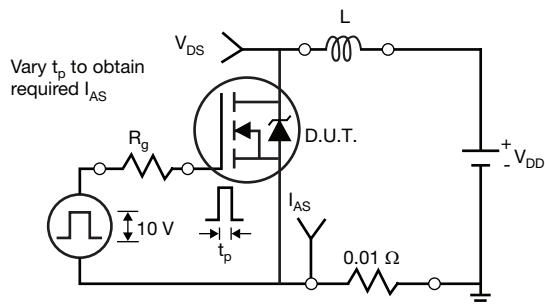


Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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