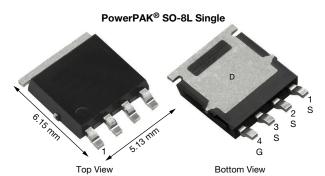
Vishay Siliconix

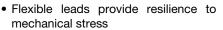
N-Channel 40 V (D-S) MOSFET



PRODUCT SUMMARY						
V _{DS} (V)	40					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.00265					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.00395					
Q _g typ. (nC)	18.5					
I _D (A) ^a	109					
Configuration	Single					

FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low Q_g and Q_{oss} reduce power loss and improve efficiency

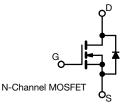




- 100 % R_a and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- DC/AC inverters



ORDERING INFORMATION						
Package	PowerPAK SO-8L					
Lead (Pb)-free and halogen-free	SiJA58ADP-T1-GE3	}				
ABSOLUTE MAXIMUM RATINGS $(T_A = 2)$	25 °C, unless otherwise noted	d)				
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-source voltage	V _{DS}	40	V			
Gate-source voltage	V _{GS}	+20, -16	v			

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V _{GS}	+20, -16	v
	T _C = 25 °C		109	
Continuous drain augrent (T. 150 °C)	T _C = 70 °C	1 , $ extstyle e$	87.3	
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	32.3 ^{b, c}	
	T _A = 70 °C		25.9 b, c	A
Pulsed drain current (t = 100 μs)		I _{DM}	150	
Continuous acures drain diada aurrent	T _C = 25 °C		51.6	
Continuous source-drain diode current	T _A = 25 °C	l _S	4.5 b, c	
Single pulse avalanche current L = 0.1 mH		I _{AS}	30	
Single pulse avalanche energy	L = U. I IIII	E _{AS}	45	mJ
	T _C = 25 °C		56.8	
Maximum power dissipation	T _C = 70 °C		36.3	W
	T _A = 25 °C	P _D	5 b, c	VV
	T _A = 70 °C		3.2 b, c	
Operating junction and storage temperature ra	T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature		260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b, f	t ≤ 10 s	R _{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.7	2.2	C/ VV

Notes

- a. $T_C = 25$ °C
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10.9
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 70 °C/W

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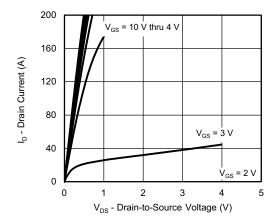
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$		-	25	-	1400
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu A$	-	-6	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.1	-	2.4	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20, -16 \text{ V}$	-	-	± 100	nA
7		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	-	-	10	μA
On-state drain current a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30	-	-	Α
5	_	V _{GS} = 10 V, I _D = 15 A	-	0.00220	0.00265	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	0.00330	0.00395	Ω
Forward transconductance a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 15 \text{ A}$	-	80	-	S
Dynamic ^b						
Input capacitance	C _{iss}		-	3030	-	
Output capacitance	C _{oss}		-	550	-	pF
Reverse transfer capacitance	C _{rss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	52	-	
C _{rss} /C _{iss} ratio			-	0.018	0.036	
		$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$	-	40.5	61	
Total gate charge	Qg		-	18.5	28	
Gate-source charge	Q _{qs}	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$	-	9.3	-	nC
Gate-drain charge	Q _{gd}		-	2.8	-	
Output charge	Q _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	-	21.5	-	
Gate resistance	R_g	f = 1 MHz	0.5	1.4	2.5	Ω
Turn-on delay time	t _{d(on)}		-	13	26	
Rise time	t _r	$V_{DD} = 20 \text{ V}, R_{L} = 2 \Omega$	-	5	10	
Turn-off delay time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	30	60	
Fall time	t _f		-	5	10	
Turn-on delay time	t _{d(on)}		-	28	56	ns
Rise time	t _r	$V_{DD} = 20 \text{ V}, R_L = 2 \Omega$	-	60	120	
Turn-off delay time	t _{d(off)}	$I_D\cong 10~A,~V_{GEN}=4.5~V,~R_g=1~\Omega$	-	30	60	
Fall time	t _f		-	10	20	
Drain-Source Body Diode Characteristic	s		<u> </u>			
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	51.6	
Pulse diode forward current (t _p = 100 μs)	I _{SM}		-	-	150	A
Body diode voltage	V _{SD}	I _S = 5 A	-	0.73	1.1	V
Body diode reverse recovery time	t _{rr}		-	29	58	ns
Body diode reverse recovery charge	Q _{rr}	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	17	34	nC
Reverse recovery fall time	t _a	T _J = 25 °C	-	14	-	
Reverse recovery rise time	t _b		-	15	-	ns

Notes

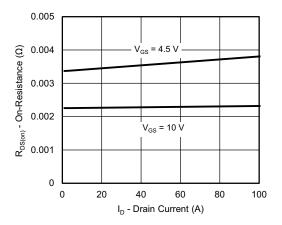
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

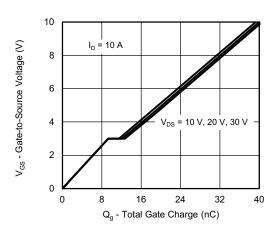




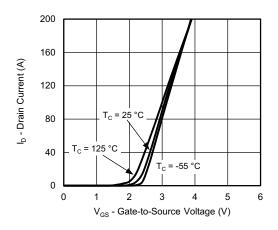
Output Characteristics



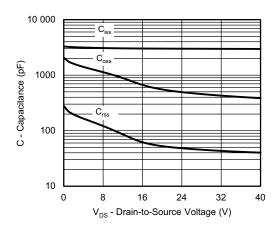
On-Resistance vs. Drain Current



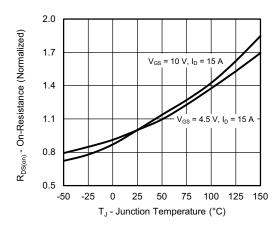
Gate Charge



Transfer Characteristics

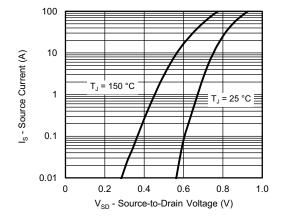


Capacitance

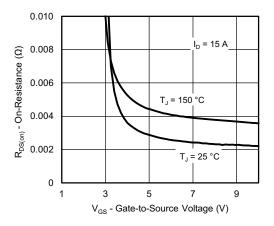


On-Resistance vs. Junction Temperature

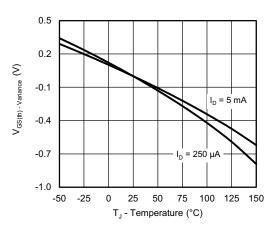




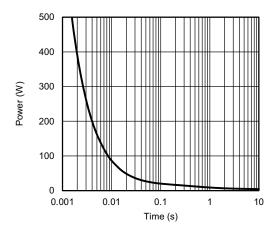
Source-Drain Diode Forward Voltage



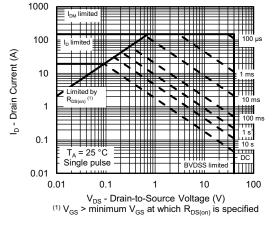
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

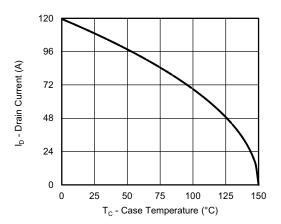


Single Pulse Power, Junction-to-Ambient

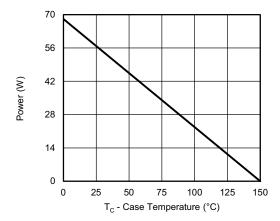


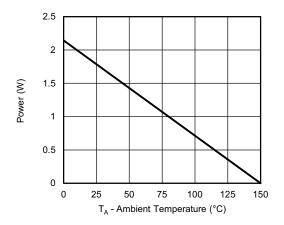
Safe Operating Area





Current Derating a





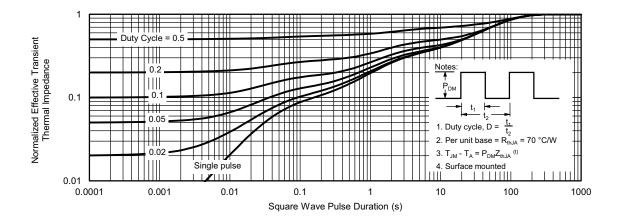
Power, Junction-to-Case

Power, Junction-to-Ambient

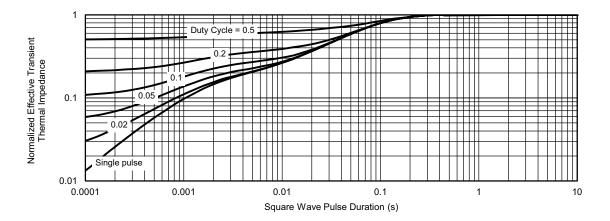
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient

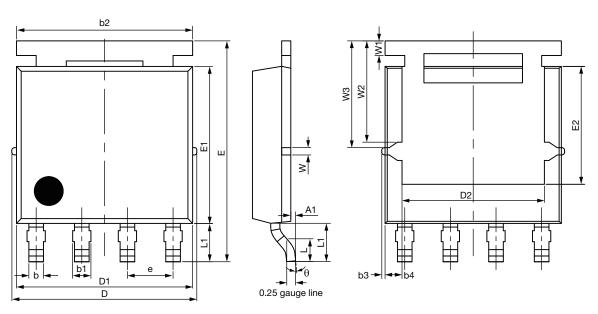


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg276918.

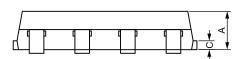


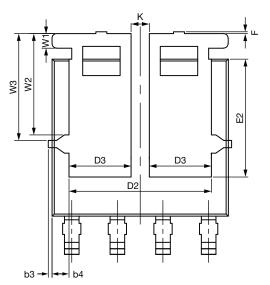
PowerPAK® SO-8L Case Outline 1



Topside view

Backside view (single)





Backside view (dual)



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DIM	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094	•		0.004		
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC	•	0.050 BSC			
E	6.05	6.05 6.15 6.25 0.		0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	3.18	3.28	3.38	0.125	0.129	0.133	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51		0.020			
W	0.23			0.009			
W1	0.41			0.016			
W2	2.82			0.111			
W3		2.96			0.117		
θ	0°	-	10°	0°	-	10°	

ECN: S19-0643-Rev. E, 05-Aug-2019

DWG: 5976

Note

• Millimeters will gover



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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