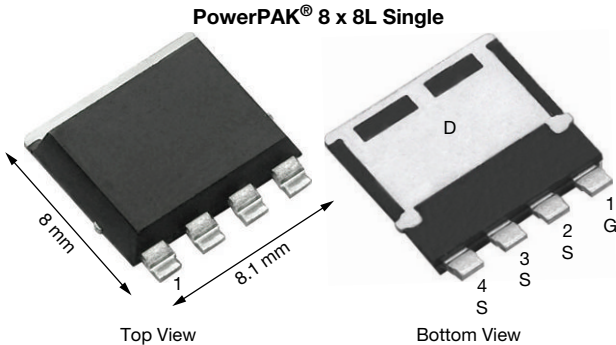


N-Channel 40 V (D-S) 175 °C MOSFET



FEATURES

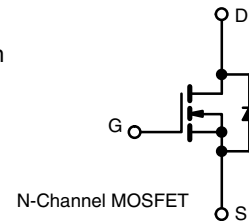
- TrenchFET® Gen IV power MOSFET
- Fully lead (Pb)-free device
- Optimized Q_g , Q_{gd} , and Q_{gd}/Q_{gs} ratio reduces switching related power loss
- Up to 200 A maximum continuous drain current
- 50 % smaller footprint than D²PAK / TO-263
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- OR-ing
- Motor drive control
- Battery management



PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00096
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00115
Q_g typ. (nC)	127
I_D (A) ^{a, g}	200
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SiJH440E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	+20 / -16	V
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	200 ^a
		$T_C = 70$ °C	200 ^a
		$T_A = 25$ °C	40 ^b
		$T_A = 70$ °C	33.8 ^b
Pulsed drain current ($t = 100$ μ s)	I_{DM}	500	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	160
		$T_A = 25$ °C	2.67 ^{b, c}
Single pulse avalanche current	I_{AS}	60	
Single pulse avalanche energy	E_{AS}	180	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	158
		$T_C = 70$ °C	110
		$T_A = 25$ °C	3 ^b
		$T_A = 70$ °C	2.1 ^b
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	42	50	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.8	0.95	

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 50 °C/W.
- $T_C = 25$ °C.

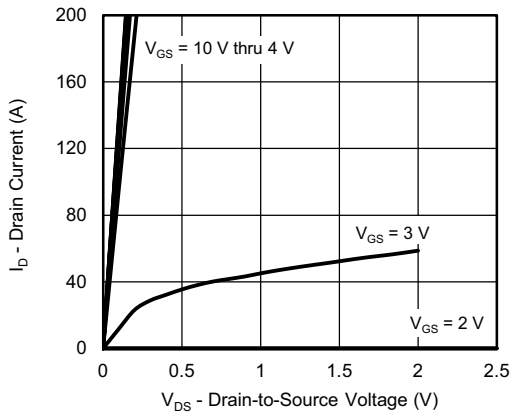
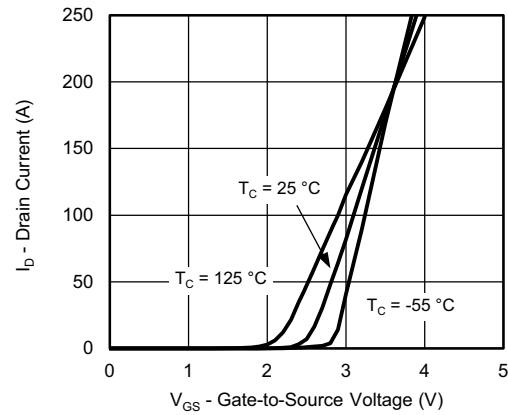
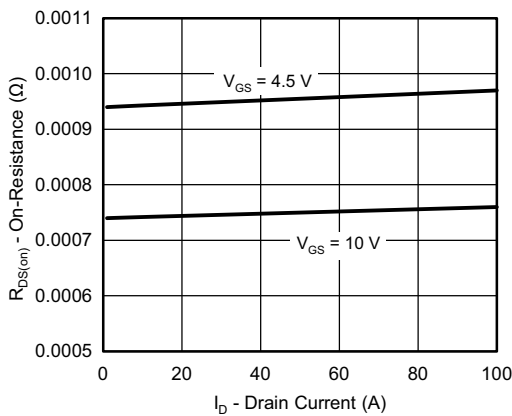
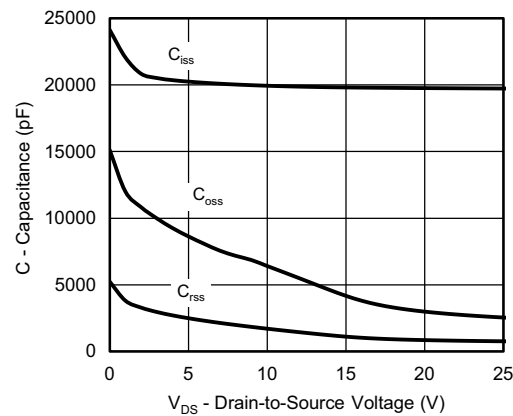
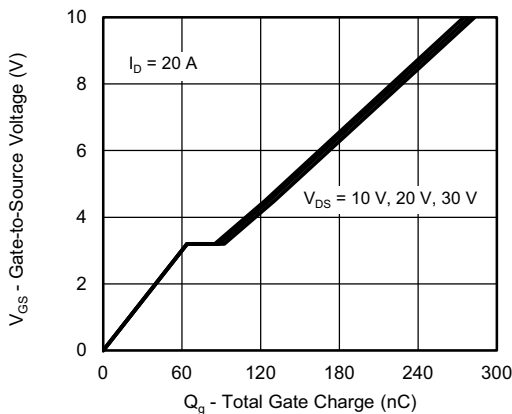
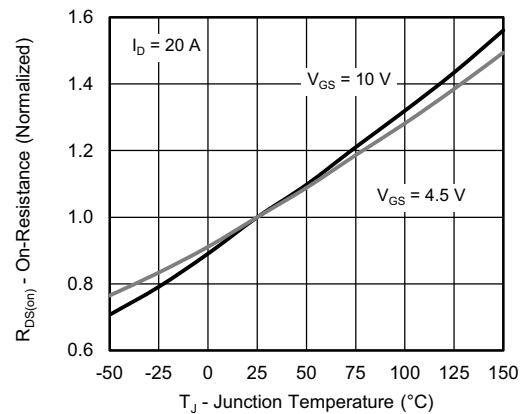


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	24	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-6.6	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.3	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20 / -16 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	60	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00080	0.00096	Ω
		V _{GS} = 4.5 V, I _D = 20 A	-	0.00096	0.00115	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A	-	140	-	S
Dynamic ^b						
Input capacitance	C _{ISS}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	20 330	-	pF
Output capacitance	C _{OSS}		-	2920	-	
Reverse transfer capacitance	C _{RSS}		-	820	-	
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 20 A	-	279	420	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 20 A	-	127	195	
Gate-source charge	Q _{gs}		-	64	-	
Gate-drain charge	Q _{gd}		-	24.5	-	
Gate resistance	R _g	f = 1 MHz	0.5	1.7	3.0	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 10 Ω, I _D ≅ 20 A, V _{GEN} = 10 V, R _g = 1 Ω	-	28	56	ns
Rise time	t _r		-	35	70	
Turn-off delay time	t _{d(off)}		-	105	210	
Fall time	t _f		-	30	60	
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1 Ω, I _D ≅ 20 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	140	280	
Rise time	t _r		-	290	580	
Turn-off delay time	t _{d(off)}		-	78	156	
Fall time	t _f		-	53	106	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	160	A
Pulse diode forward current	I _{SM}		-	-	300	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.68	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs, T _J = 25 °C	-	92	184	ns
Body diode reverse recovery charge	Q _{rr}		-	245	490	nC
Reverse recovery fall time	t _a		-	54	-	ns
Reverse recovery rise time	t _b		-	38	-	

Notes

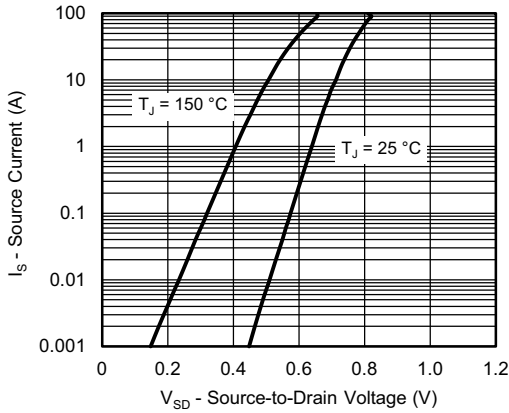
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

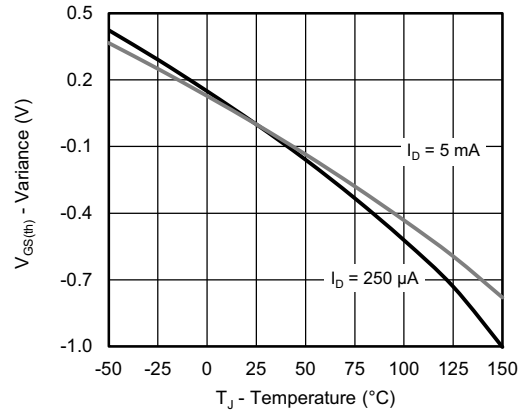
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



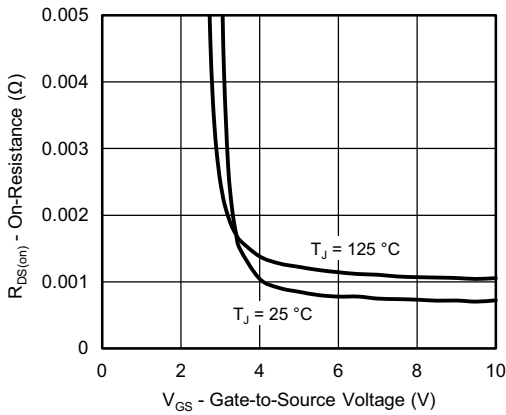
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



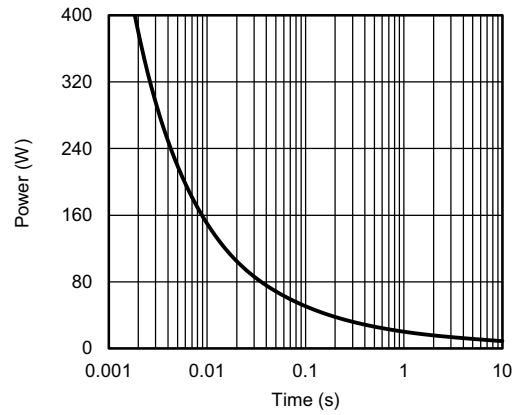
Source-Drain Diode Forward Voltage



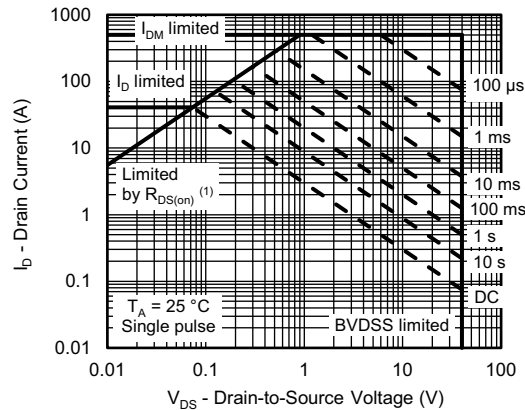
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

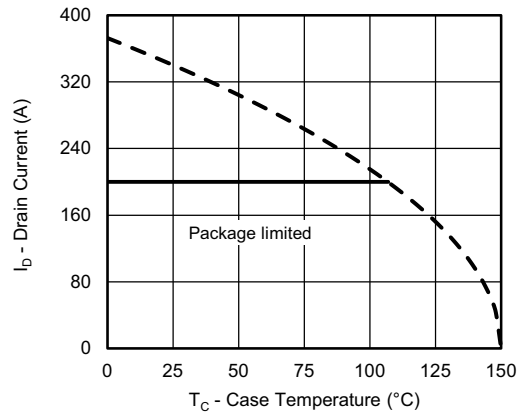


Safe Operating Area, Junction-to-Ambient

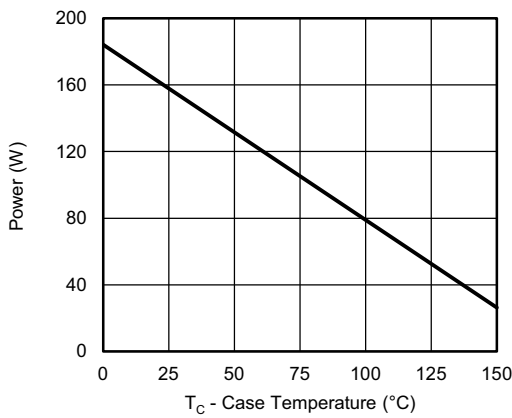
(1) VGS > minimum VGS at which RDS(on) is specified



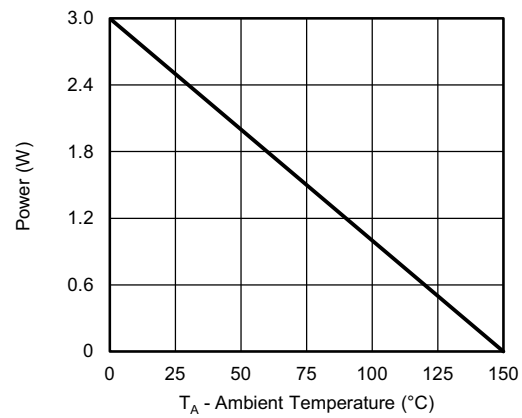
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



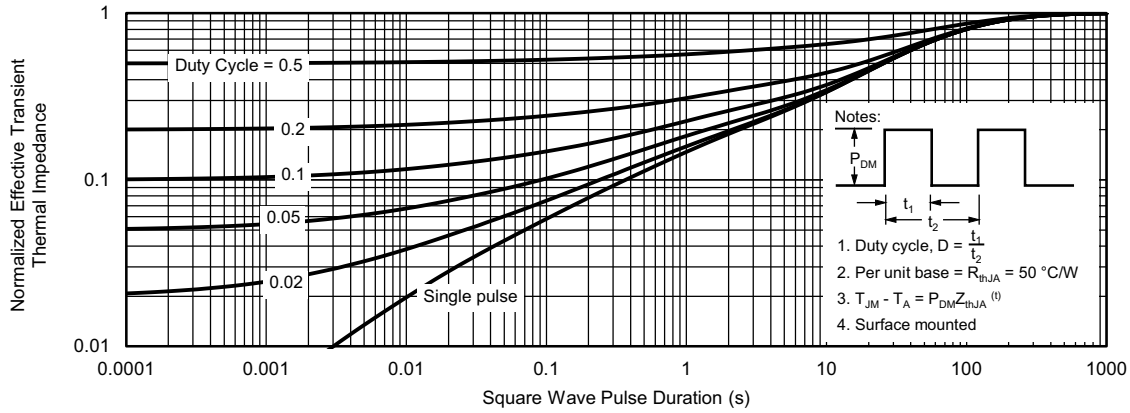
Power, Junction-to-Ambient

Note

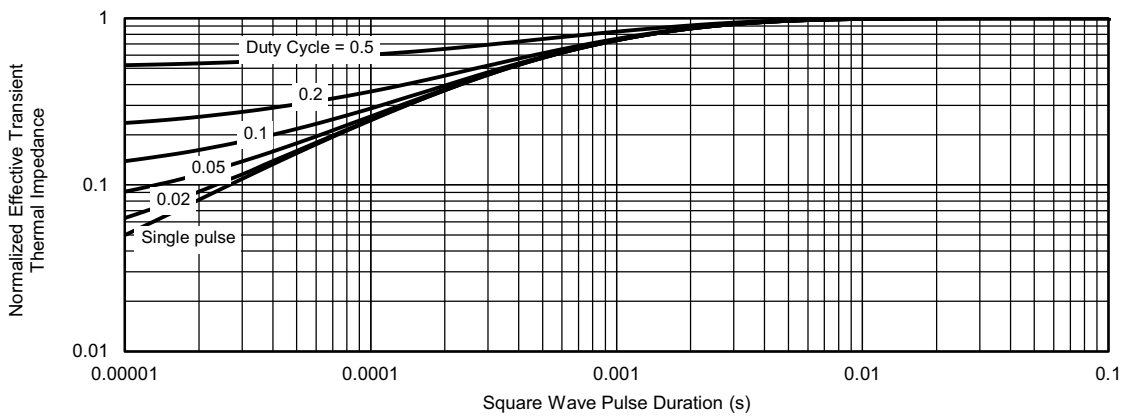
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



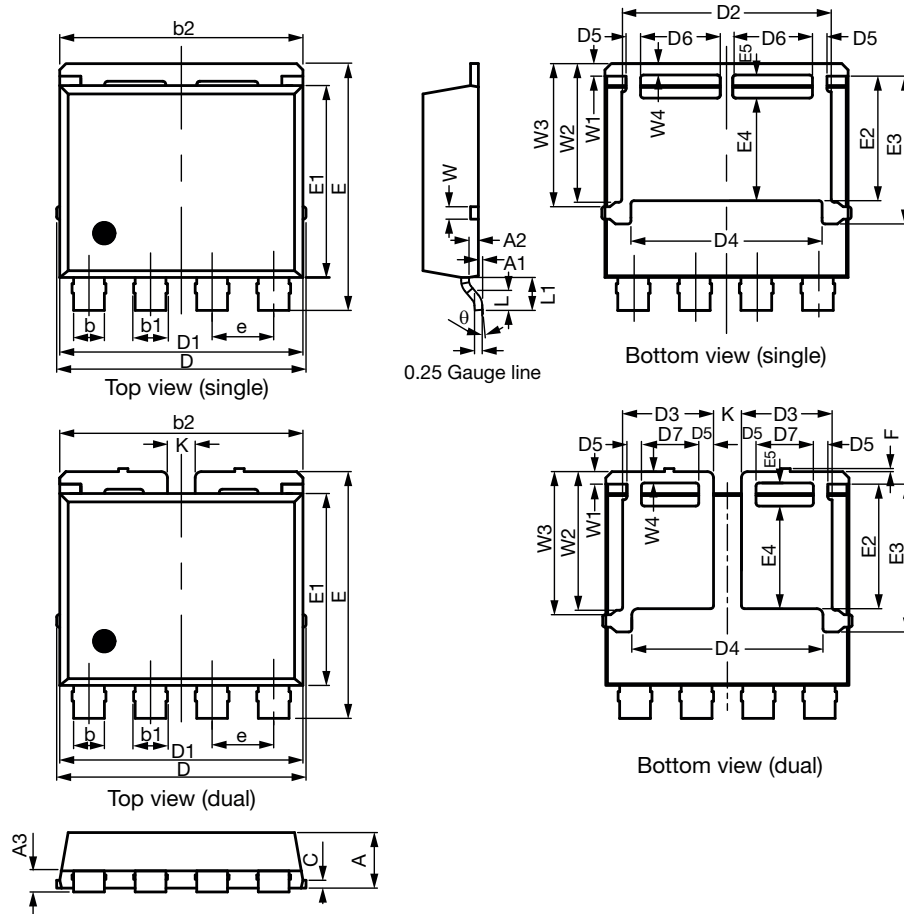
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK[®] 8 x 8L Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.70	1.80	1.90	0.067	0.071	0.075
A1	0.00	0.08	0.13	0.000	0.003	0.005
A2	0.25	0.30	0.35	0.010	0.012	0.014
A3	0.55	0.62	0.70	0.022	0.024	0.028
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	7.80	7.90	8.00	0.307	0.311	0.315
c	0.20	0.25	0.30	0.008	0.010	0.012
D	8.00	8.10	8.25	0.315	0.319	0.325
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D3	2.85	2.95	3.05	0.112	0.116	0.120
D4	6.11	6.21	6.31	0.241	0.244	0.248
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
D7	1.76	1.86	1.96	0.069	0.073	0.077



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
e	1.95	2.00	2.05	0.077	0.079	0.081
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	3.94	4.04	4.14	0.140	0.159	0.163
E3	4.69	4.79	4.89	0.185	0.189	0.193
E4	3.23	3.33	3.43	0.127	0.131	0.135
E5	0.65	0.75	0.85	0.026	0.030	0.033
F	0.00	0.10	0.15	0.000	0.004	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.80	0.90	1.00	0.031	0.035	0.039
W	0.30	0.40	0.50	0.012	0.016	0.020
W1	0.30	0.40	0.50	0.012	0.016	0.020
W2	4.39	4.49	4.59	0.173	0.177	0.181
W3	4.54	4.64	4.74	0.179	0.183	0.187
W4	0.32	0.37	0.42	0.013	0.015	0.017
θ	6°	10°	14°	6°	10°	14°

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DWG: 6026



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