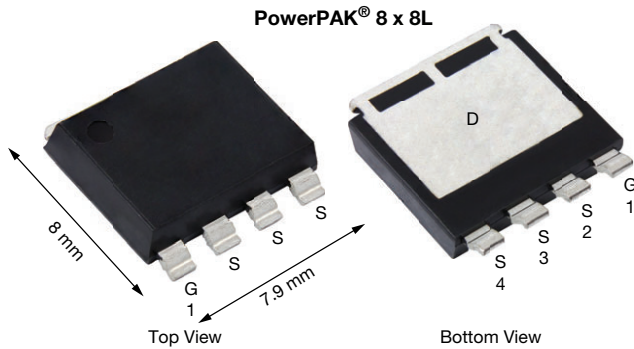


## N-Channel 60 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00092
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.00115
$Q_g$ typ. (nC)	141
$I_D$ (A) <sup>a</sup>	373
Configuration	Single

### FEATURES

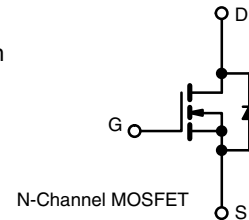
- TrenchFET® Gen IV power MOSFET
- Fully lead (Pb)-free device
- Optimized  $Q_g$ ,  $Q_{gd}$ , and  $Q_{gd}/Q_{gs}$  ratio reduces switching related power loss
- 50 % smaller footprint than D<sup>2</sup>PAK (TO-263)
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- OR-ing
- Motor drive control
- Battery management
- Power supply



ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SIJH600E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	60	V	
Gate-source voltage	$V_{GS}$	$\pm 20$	V	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	373	A
		$T_C = 70$ °C	312	
		$T_A = 25$ °C	37 <sup>b</sup>	
		$T_A = 70$ °C	31 <sup>b</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	500		
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	303	
		$T_A = 25$ °C	3 <sup>b</sup>	
Single pulse avalanche current	$I_{AS}$	80		
Single pulse avalanche energy	$E_{AS}$	320	mJ	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	333	W
		$T_C = 70$ °C	233	
		$T_A = 25$ °C	3.3 <sup>b</sup>	
		$T_A = 70$ °C	2.3 <sup>b</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>c</sup>		260		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	36	45	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	0.36	0.45	

#### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	30	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-8.3	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	-	4	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20	-	-	100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.00065	0.00092	Ω
		V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	0.00080	0.00115	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 50 A	-	170	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	9950	-	pF
Output capacitance	C <sub>OSS</sub>		-	2575	-	
Reverse transfer capacitance	C <sub>RSS</sub>		-	78	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	141	212	nC
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	107	161	
Gate-source charge	Q <sub>gs</sub>		-	42	-	
Gate-drain charge	Q <sub>gd</sub>		-	20	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.23	1.2	2.4	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 10 Ω, I <sub>D</sub> ≅ 3 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	22	45	ns
Rise time	t <sub>r</sub>		-	15	30	
Turn-off delay time	t <sub>d(off)</sub>		-	55	110	
Fall time	t <sub>f</sub>		-	20	40	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 10 Ω, I <sub>D</sub> ≅ 3 A, V <sub>GEN</sub> = 7.5 V, R <sub>g</sub> = 1 Ω	-	30	60	
Rise time	t <sub>r</sub>		-	20	40	
Turn-off delay time	t <sub>d(off)</sub>		-	50	100	
Fall time	t <sub>f</sub>		-	20	40	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	303	A
Pulse diode forward current	I <sub>SM</sub>		-	-	500	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.73	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	87	175	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	130	260	nC
Reverse recovery fall time	t <sub>a</sub>		-	42	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	45	-	

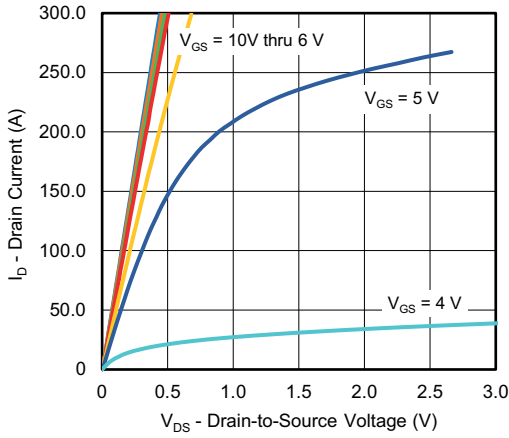
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

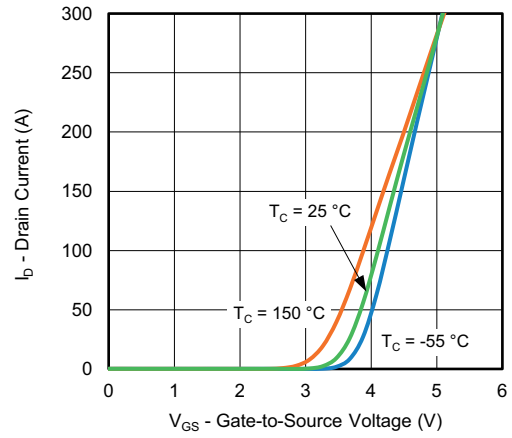
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



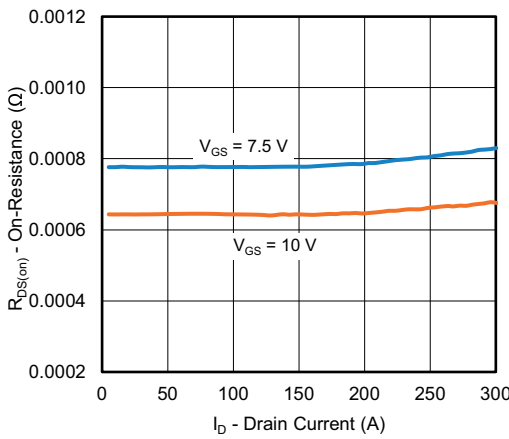
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



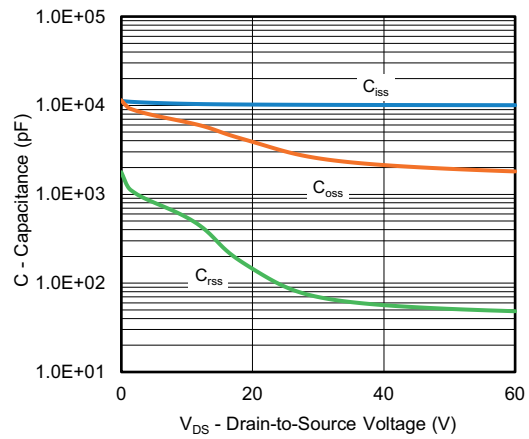
**Output Characteristics**



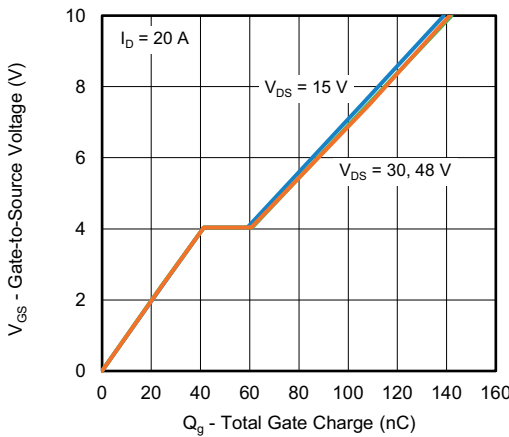
**Transfer Characteristics**



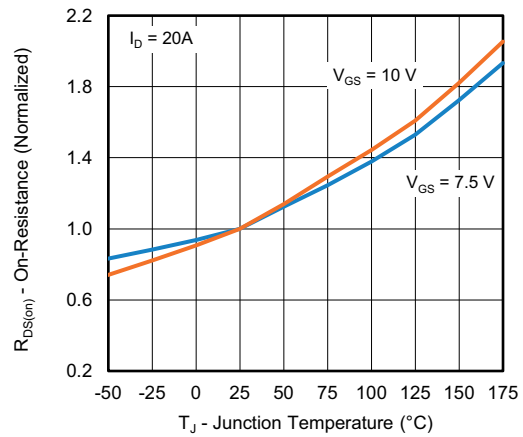
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

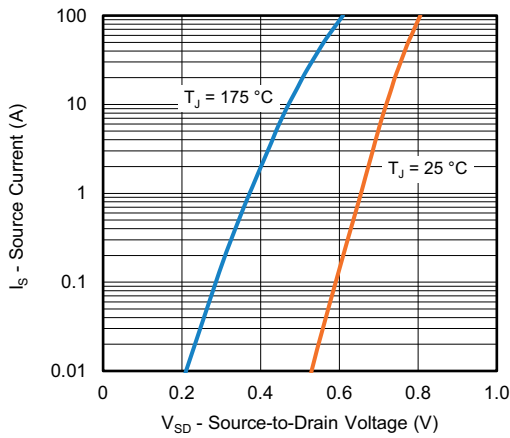


**Gate Charge**

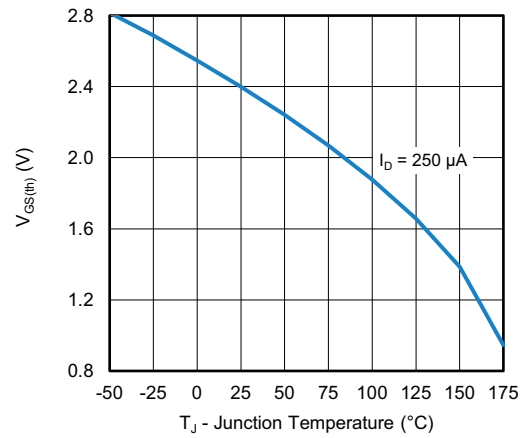


**On-Resistance vs. Junction Temperature**

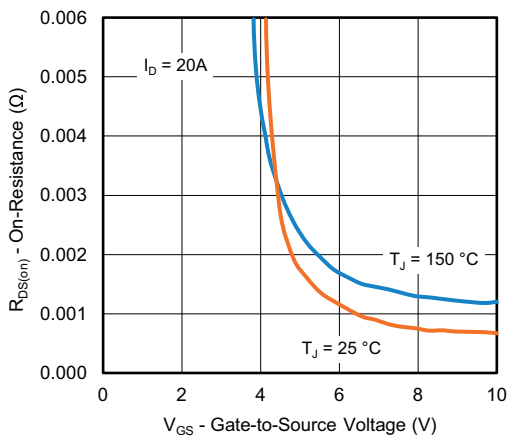
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



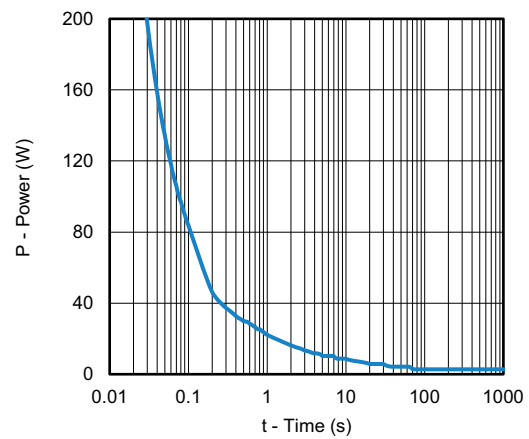
**Source-Drain Diode Forward Voltage**



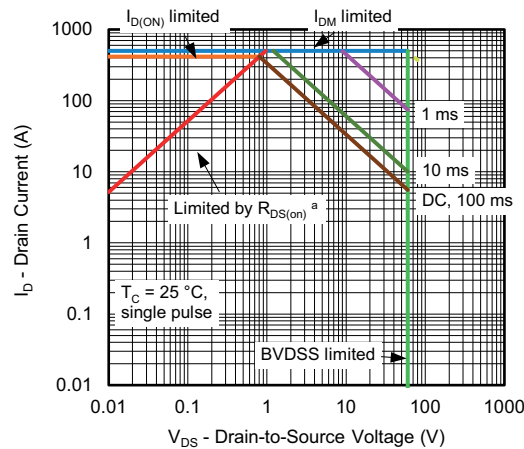
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**Single Pulse Power, Junction-to-Ambient**



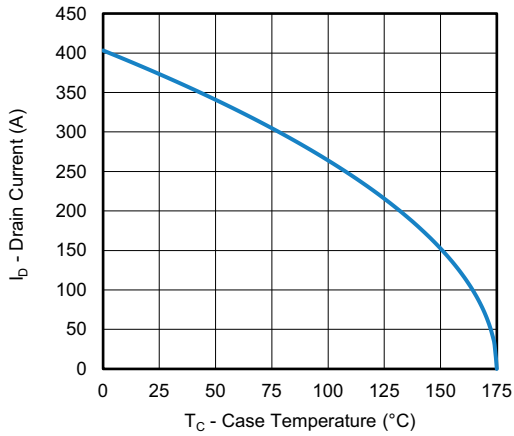
**Safe Operating Area, Junction-to-Ambient**

**Note**

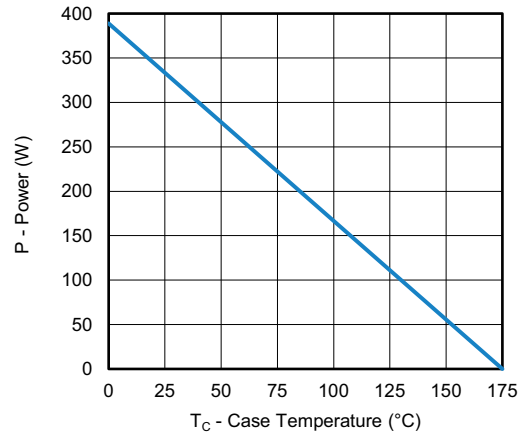
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



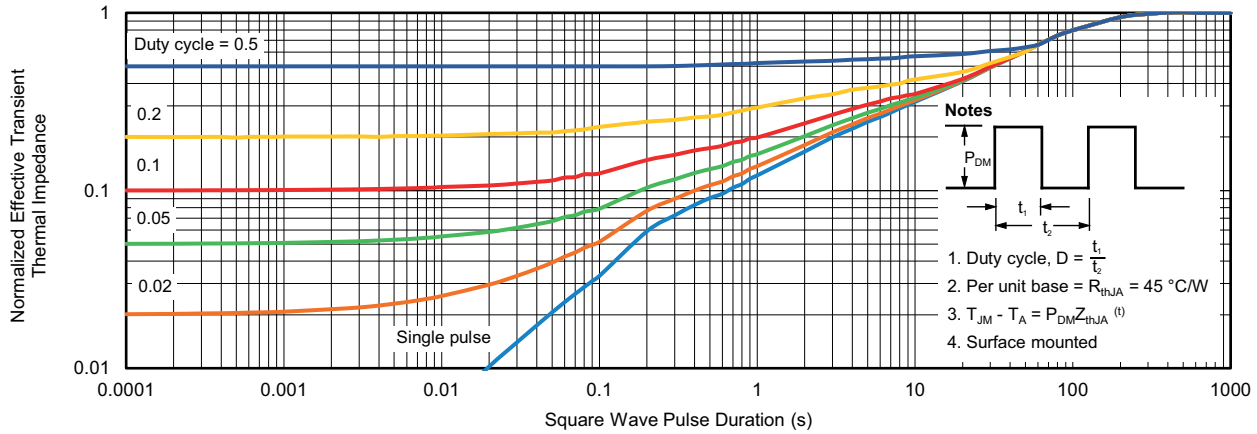
**Power, Junction-to-Case**

**Note**

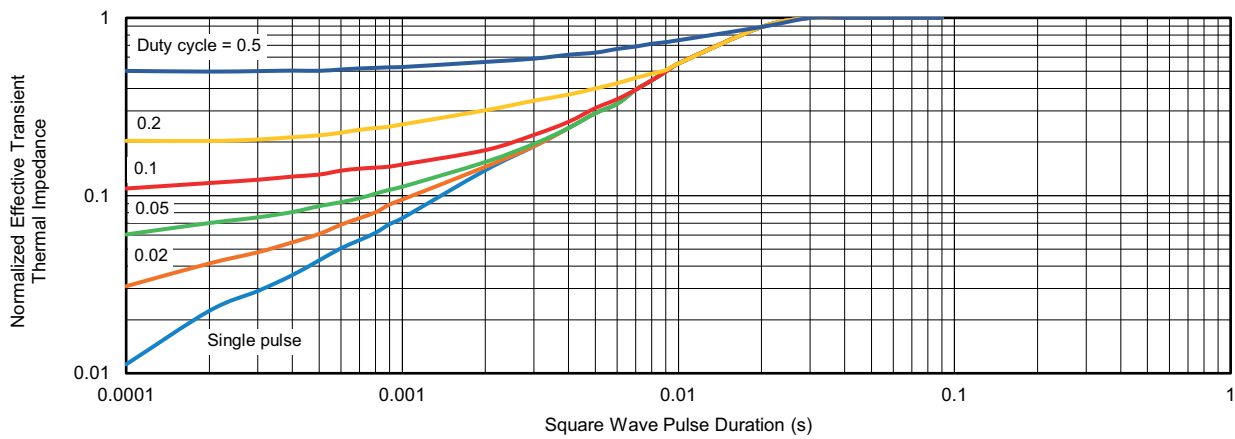
- a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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