SiRC18DP

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ISHA

Vishay Siliconix

N-Channel 30 V (D-S) MOSFET With Schottky Diode



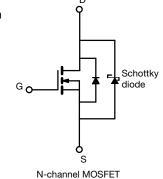
PRODUCT SUMMARY	
MOSFET	
V _{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00110
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00154
Q _g typ. (nC)	35
I _D (A) ^{a, g}	60
SCHOTTKY	
V _F (V) at 10 A	0.55
I _F (A) ^{a, g}	60
Configuration	Single plus integrated Schottky

FEATURES

- TrenchFET[®] Gen IV power MOSFET
- SkyFET[®] with monolithic Schottky diode
- Optimized $R_{DS} \times Q_g$ and $R_{DS} \times Q_{gd}$ FOM elevates efficiency for high-frequency switching
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Synchronous buck
- Synchronous rectification
- DC/DC conversion



ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiRC18DP-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	30	V	
Gate-source voltage		V _{GS}	+20, -16	v	
	T _C = 25 °C		60 ^a		
	T _C = 70 °C		60 ^a		
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	52 ^{b, c}		
	T _A = 70 °C		42 ^{b, c}	_	
Pulsed drain current (t = 100 µs)		I _{DM}	250	— A	
	T _C = 25 °C		60 ^a		
Continuous source current (MOSFET diode conduction)	T _A = 25 °C	I _S	5 ^{a, b}		
Single pulse avalanche current		I _{AS}	30		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	45	mJ	
	T _C = 25 °C		54.3		
••• · · · · · · · · · · · · · · · · · ·	T _C = 70 °C	_	34.7	14/	
Maximum power dissipation	T _A = 25 °C	P _D	5 ^{b, c}		
	T _A = 70 °C		3.2 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		
Soldering recommendations (peak temperature)			260		

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THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b, f	t ≤ 10 s	R _{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.8	2.3	0,00

Notes

a. Package limitedb. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

f. Maximum under steady state conditions is 65 °C/W

g. T_C = 25 °C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1	-	2.4	v	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = +20 V, -16 V$	-	-	± 100	nA	
Zara gata valtaga drain aurrant		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$ - 0.06		0.06	0.20	m 4	
Zero gate voltage drain current	IDSS	V_{DS} = 30 V, V_{GS} = 0 V, T_{J} = 70 °C	-	1	10	ШA	
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	А	
Drain source on state resistance a	Passa	V _{GS} = 10 V, I _D = 15 A	-	0.00085	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	0	
Drain-source on-state resistance ~	N-state resistance a $R_{DS(on)}$ $V_{GS} = 10$ Nonductance a g_{fs} $V_{GS} = 4.5$ conductance a g_{fs} $V_{DS} = 10$ nce C_{iss} $V_{DS} = 15 V, V_{GS}$ ance C_{oss} $V_{DS} = 15 V, V_{GS}$ er capacitance C_{rss} $V_{DS} = 15 V, V_{GS}$ ge Q_{gs} $V_{DS} = 15 V, V_{GS}$ narge Q_{gs} $V_{DS} = 15 V, V_{GS}$ en arge Q_{gd} $V_{DS} = 15 V, V_{GS}$ en arge V_{gd} $V_{SS} = 15 V, V_{SS}$ en arge V_{gd} $V_{SS} = 15 V, V_{SS}$ en arge V_{gd} V_{SS} en arge V_{gd} V_{SS} en arge V_{gd} V_{SS} en arge V_{gd} V_{SS} en arge V_{SS} V_{SS} <	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	0.00135	0.00154	52	
Forward transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 15 A	-	70	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	5060	-		
Output capacitance		\/	-	2400	-	pF	
Reverse transfer capacitance		$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	-	350	-		
C _{rss} /C _{iss} ratio			-	0.069	0.140		
Total gata abarga	0	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	74	111	1	
Total gate charge	Qg		- 35 53 nC				
Gate-source charge	Q _{gs}	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A	-	11.8	-	A Ω S pF	
Gate-drain charge			-	8.4	-		
Gate resistance	R _g	f = 1 MHz	0.1	0.5	0.9	Ω	
Turn-on delay time	t _{d(on)}		-	16	32		
Rise time	t _r	V_{DD} = 15 V, R_L = 1.5 Ω , $I_D \cong$ 10 A,	-	21	42		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$	-	30	60		
Fall time	t _f		-	12	24	1	
Turn-on delay time	t _{d(on)}		-	31	62	ns	
Rise time	t _r	$V_{DD} = 15 \text{ V}, \text{ R}_{\text{L}} = 1.5 \Omega, \text{ I}_{D} \cong 10 \text{ A},$	-	77	154		
Turn-off delay time	t _{d(off)}	$V_{\text{GEN}} = 4.5 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$	-	38	76		
Fall time	t _f		-	37	74		
Drain-source Body Diode Characteris	tics						
Continuous source-drain diode current	I _S	$T_{\rm C} = 25^{\circ}{\rm C}$	-	-	60	А	
Pulse diode forward current	I _{SM}		-	-	100	A	
Body diode voltage	V _{SD}	$I_{\rm S} = 5$ A, $V_{\rm GS} = 0$ V	-	0.41	0.55	V	
Body diode reverse recovery time	t _{rr}		-	58	116	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 10 A, di/dt = 100 A/μs,	-	72	144	nC	
Reverse recovery fall time	t _a	$T_J = 25 \ ^{\circ}C$	-	26	-		
Reverse recovery rise time	t _b		-	32	-	ns	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

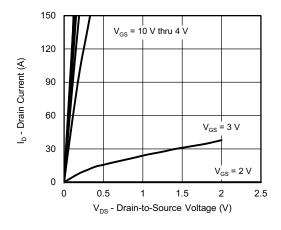
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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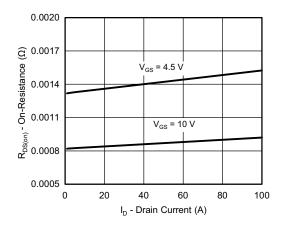


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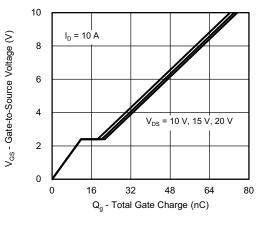
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



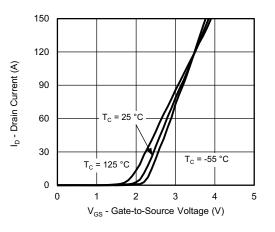
Output Characteristics



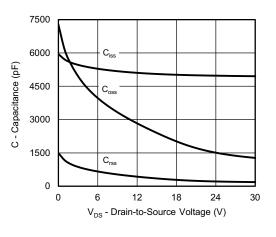
On-Resistance vs. Drain Current and Gate



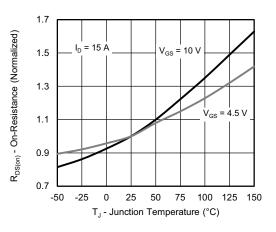
Gate Charge



Transfer Characteristics



Capacitance



On-Resistance vs. Junction Temperature

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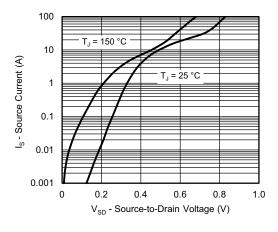
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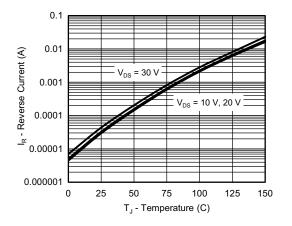


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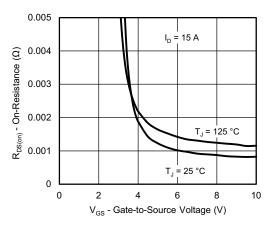
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



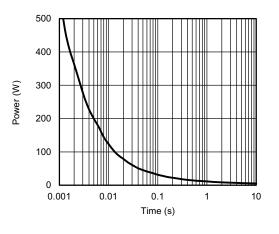
Source-Drain Diode Forward Voltage



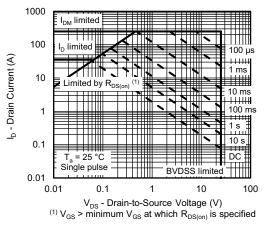
Reverse Current vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power



Safe Operating Area, Junction-to-Ambient

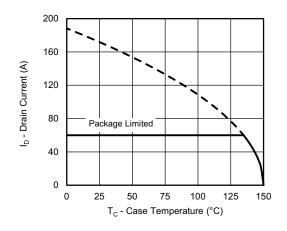
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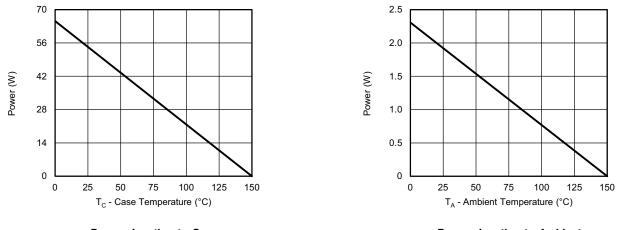


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case

Power, Junction-to-Ambient

Note

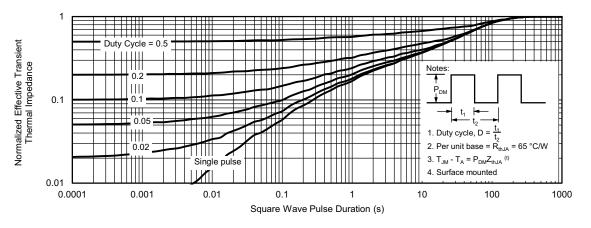
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



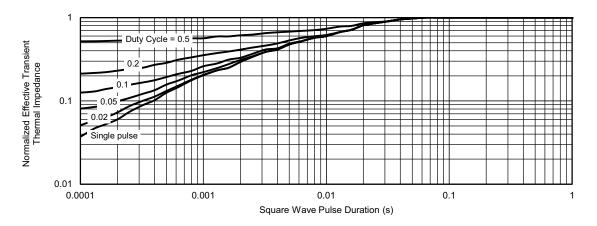
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76402.

D2

E3

Backside View of Dual Pad



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PowerPAK[®] SO-8, (Single/Dual)



Notes

1. Inch will govern.

2 Dimensions exclusive of mold gate burrs.

3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX		
А	0.97	1.04	1.12	0.038	0.041	0.044		
A1		-	0.05	0	-	0.00		
b	0.33	0.41	0.51	0.013	0.016	0.02		
С	0.23	0.28	0.33	0.009	0.011	0.01		
D	5.05	5.15	5.26	0.199	0.203	0.20		
D1	4.80	4.90	5.00	0.189	0.193	0.19		
D2	3.56	3.76	3.91	0.140	0.148	0.154		
D3	1.32	1.50	1.68	0.052	0.059	0.066		
D4		0.57 typ.			0.0225 typ.			
D5		3.98 typ.			0.157 typ.			
E	6.05	6.15	6.25	0.238	0.242	0.246		
E1	5.79	5.89	5.99	0.228	0.232	0.23		
E2	3.48	3.66	3.84	0.137	0.144	0.15		
E3	3.68	3.78	3.91	0.145	0.149	0.154		
E4		0.75 typ.		0.030 typ.				
е		1.27 BSC		0.050 BSC				
К		1.27 typ.		0.050 typ.				
K1	0.56	-	-	0.022	-	-		
Н	0.51	0.61	0.71	0.020	0.024	0.028		
L	0.51	0.61	0.71	0.020	0.024	0.028		
L1	0.06	0.13	0.20	0.002	0.005	0.008		
θ	0°	-	12°	0°	-	12°		
W	0.15	0.25	0.36	0.006	0.010	0.014		
М		0.125 typ.			0.005 typ.			



Application Note 826

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RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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