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N-Channel 40 V (D-S) Fast Switching MOSFET

PowerPAK® 1212-8SH

Top View **Bottom View**

PRODUCT SUMMARY						
V _{DS} (V)	40					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0078					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0100					
Q _g typ. (nC)	15					
I _D (A)	16.4					
Configuration	Single					

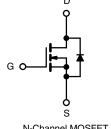
FEATURES

- TrenchFET® power MOSFET
- PWM optimized
- 100 % R_q tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Synchronous rectification
- Intermediate switch
- Synchronous buck



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH116DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless	otherwise no	ted)			
PARAMETER		SYMBOL	10 s	STEADY STATE	UNIT	
Drain-source voltage		V_{DS}	40	40		
Gate-source voltage		V _{GS}	± 20	± 20	V	
Continuous drain current (T _J = 150 °C) ^a	T _A = 25 °C	- I _D	16.4	10.5		
	T _A = 70 °C		13.1	8.4		
Pulsed drain current		I _{DM}	60	60	А	
Continuous source current (diode conduction) a		I _S	3.2	1.3		
Avalanche current		I _{AS}	15	15		
Avalanche energy	L = 0 1 mH		11	11	mJ	
Marrian var a sur a disaina di	T _A = 25 °C	Б	3.8	1.5	14/	
Maximum power dissipation ^a	T _A = 70 °C	P _D	2	0.8	W	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) b, c			260			

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient a	iunation to ambient â t ≤ 10 s	ם	24	33	
Waximum junction-to-ambient ~	Steady state	R _{thJA}	65	81	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.9	2.4	

- a. Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	1		1			
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.5	-	2.5	V
Gate-body leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
Zava gata valtaga duain avumant		V _{DS} = 40 V, V _{GS} = 0 V		-	1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α
Drain-source on-state resistance a	В	V _{GS} = 10 V, I _D = 16.4 A	-	0.0065	0.0078	Ω
	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 14.5 A	-	0.0083	0.0100	
Forward transconductance a	9 _{fs}	V _{DS} = 15 V, I _D = 16.4 A	-	68	-	S
Diode forward voltage ^a	V _{SD}	I _S = 3.2 A, V _{GS} = 0 V	-	0.8	1.2	V
Dynamic ^b						
Total gate charge	Qg		-	15	23	
Gate-source charge	Q _{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 16.4 \text{ A}$	-	6.7	-	nC
Gate-drain charge	Q_{gd}		-	5.1	-	ĺ
Gate resistance	Rg	f = 1 MHz	0.7	1.4	2.1	Ω
Turn-on delay time	t _{d(on)}		-	10	15	
Rise time	t _r	V_{DD} = 20 V, R_L = 20 Ω	-	10	15	
Turn-off delay time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω	-	36	55	ns
Fall time	t _f		-	10	15	
Source-drain reverse recovery time	t _{rr}	1 2 2 A di/d+ 100 A/va	-	30	60	
Body diode reverse recovery charge	Q _{rr}	$I_F = 3.2 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	26	52	nc

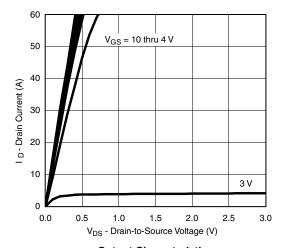
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

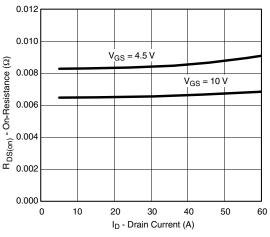
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



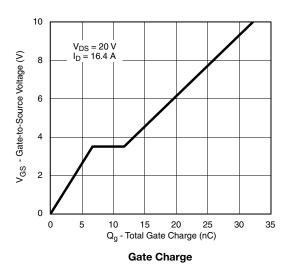
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

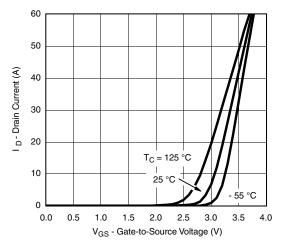


Output Characteristics

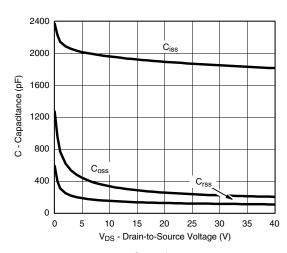


On-Resistance vs. Drain Current

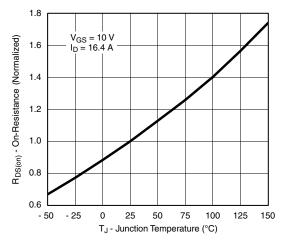




Transfer Characteristics



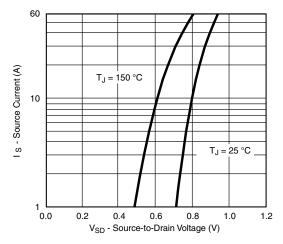
Capacitance



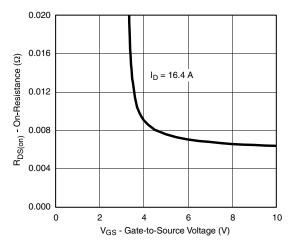
On-Resistance vs. Junction Temperature



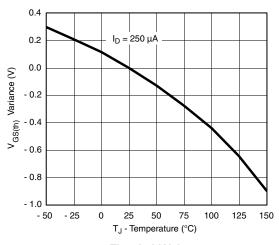
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



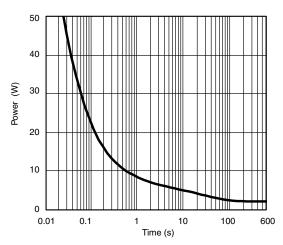
Source-Drain Diode Forward Voltage



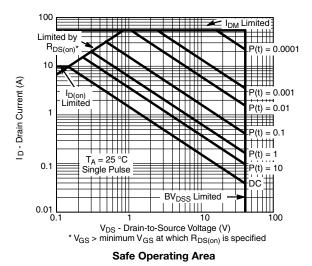
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

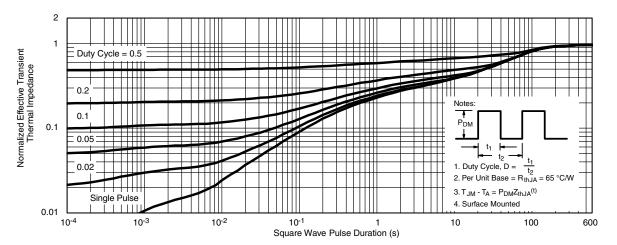


Single Pulse Power, Junction-to-Ambient

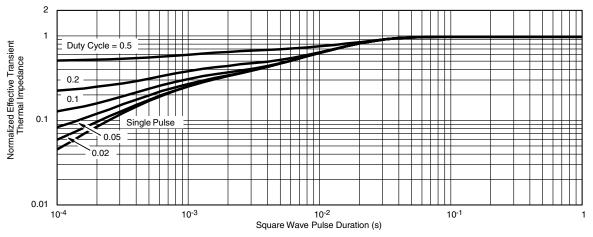




TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



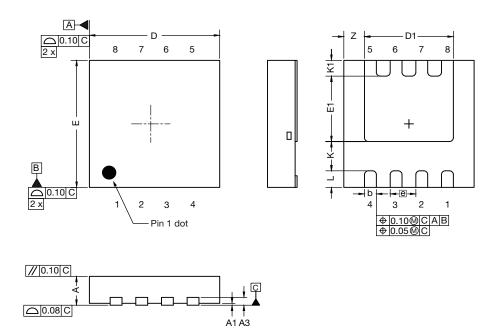
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?79240.



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Case Outline for PowerPAK® 1212-SWLH and PowerPAK® 1212-8SH



DIM.	MILLIMETERS			INCHES				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Α	0.82	0.90	0.98	0.032	0.035	0.038		
A1	0.00	-	0.05	0.000	-	0.002		
A3		0.20 ref.			0.008 ref.			
b	0.25	0.30	0.35	0.010	0.012	0.014		
D	3.20	3.30	3.40	0.126	0.130	0.134		
D1	2.15	2.25	2.35	0.085	0.089	0.093		
Е	3.20	3.30	3.40	0.126	0.130	0.134		
E1	1.60	1.70	1.80	0.063	0.067	0.071		
е		0.65 bsc.			0.026 bsc.			
K		0.76 ref.			0.030 ref.			
K1	0.41 ref.		0.016 ref.					
L	0.33	0.43	0.53	0.013	0.017	0.021		
Z	0.525 ref.			0.021 ref.				

DWG: 6062



RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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