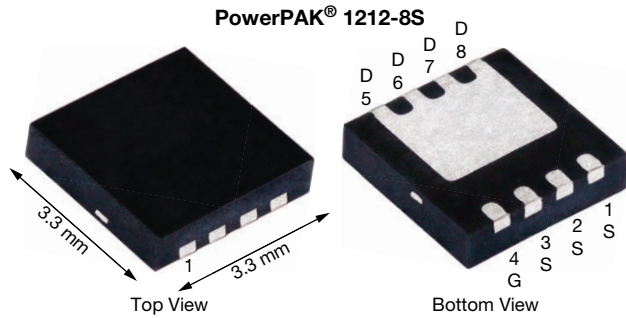


N-Channel 80 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	80
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0072
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0095
Q_g typ. (nC)	17.7
I_D (A)	63
Configuration	Single

FEATURES

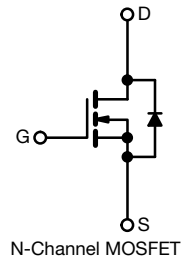
- TrenchFET® Gen IV power MOSFET
- Very low $R_{DS} - Q_g$ figure-of-merit (FOM)
- Tuned for the lowest $R_{DS} - Q_{oss}$ FOM
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Motor drive switch
- Battery and load switch
- Industrial



N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS32LDN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	63	A
	$T_C = 70$ °C	50.3	
	$T_A = 25$ °C	17.4 ^{b, c}	
	$T_A = 70$ °C	13.9 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	150	A
Continuous source-drain diode current	$T_C = 25$ °C	59.7	A
	$T_A = 25$ °C	4.5 ^{b, c}	
Single pulse avalanche current	$L = 0.1$ mH	20	mJ
Single pulse avalanche energy		20	
Maximum power dissipation	$T_C = 25$ °C	65.7	W
	$T_C = 70$ °C	42	
	$T_A = 25$ °C	5 ^{b, c}	
	$T_A = 70$ °C	3.2 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	R_{thJC}	1.5	1.9	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 63 °C/W
- $T_C = 25$ °C



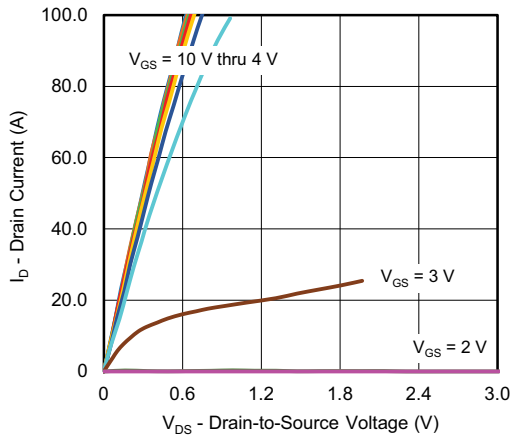
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	80	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	60	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-4.8	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	40	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.0058	0.0072	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.0073	0.0095	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A	-	55	-	S
Dynamic ^b						
Input capacitance	C _{ISS}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	-	2550	-	pF
Output capacitance	C _{OSS}		-	250	-	
Reverse transfer capacitance	C _{RSS}		-	15.5	-	
Total gate charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 10 A	-	37.5	57	nC
		V _{DS} = 40 V, V _{GS} = 4.5 V, I _D = 10 A	-	17.7	27	
Gate-source charge	Q _{gs}	V _{DS} = 40 V, V _{GS} = 4.5 V, I _D = 10 A	-	7.3	-	
Gate-drain charge	Q _{gd}		-	4.6	-	
Output charge	Q _{OSS}		V _{DS} = 40 V, V _{GS} = 0 V	-	35	
Gate resistance	R _g	f = 1 MHz	0.3	0.86	1.5	
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	12	24	ns
Rise time	t _r		-	6	12	
Turn-off delay time	t _{d(off)}		-	28	56	
Fall time	t _f		-	6	12	
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	22	44	
Rise time	t _r		-	61	122	
Turn-off delay time	t _{d(off)}		-	26	52	
Fall time	t _f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	59.7	A
Pulse diode forward current	I _{SM}		-	-	150	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.75	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	40	80	ns
Body diode reverse recovery charge	Q _{rr}		-	45	90	nC
Reverse recovery fall time	t _a		-	24	-	ns
Reverse recovery rise time	t _b		-	16	-	

Notes

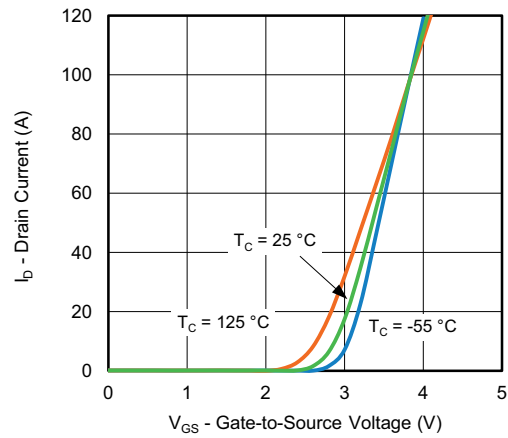
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

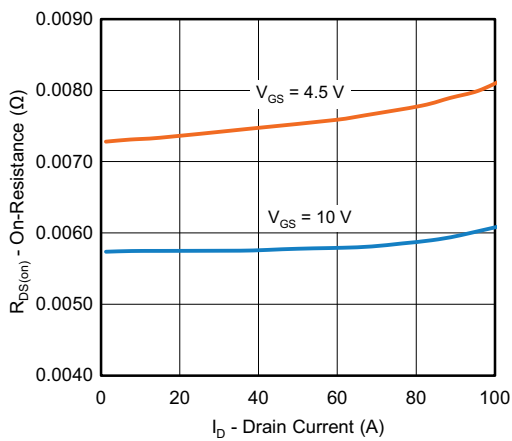
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



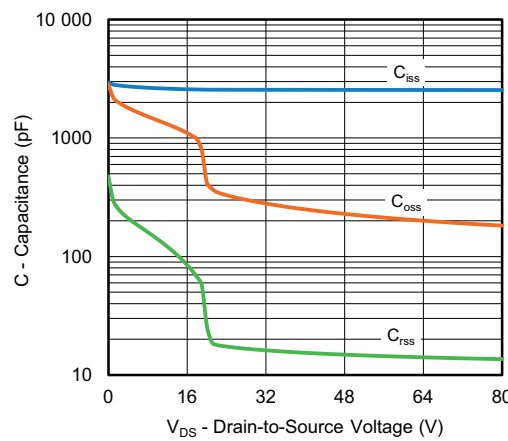
Output Characteristics



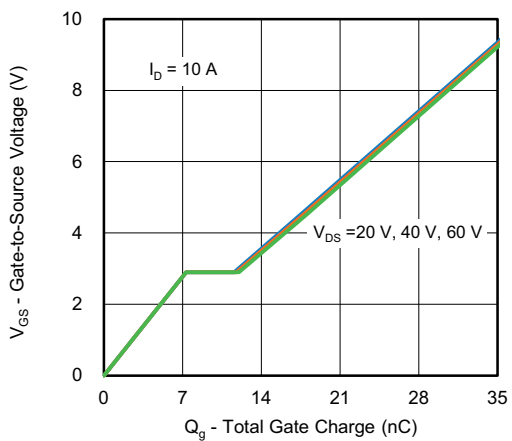
Transfer Characteristics



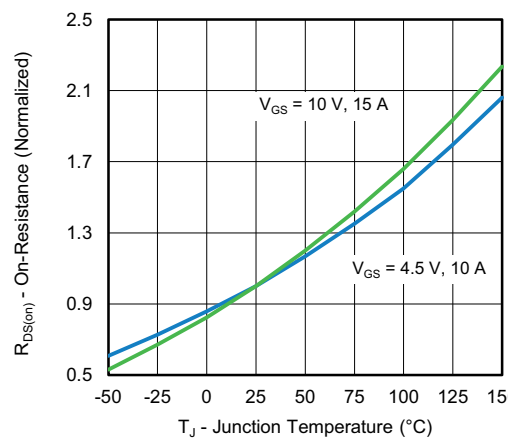
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



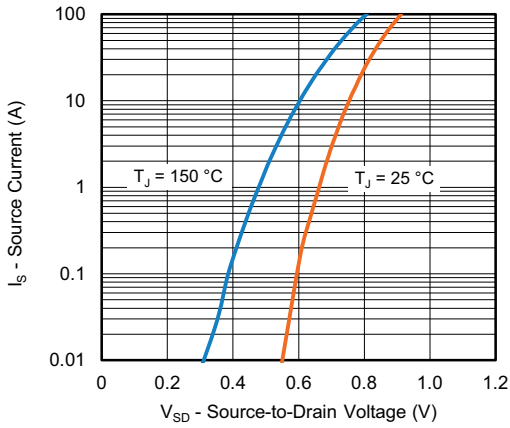
Gate Charge



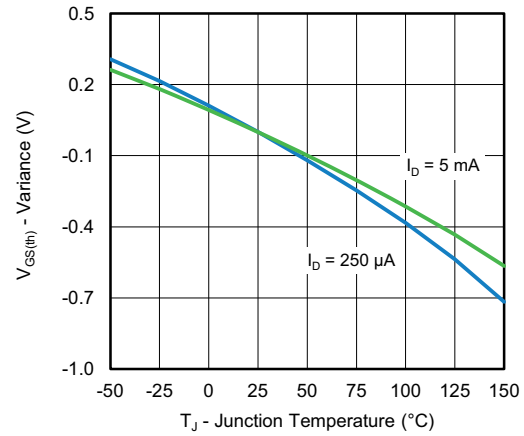
On-Resistance vs. Junction Temperature



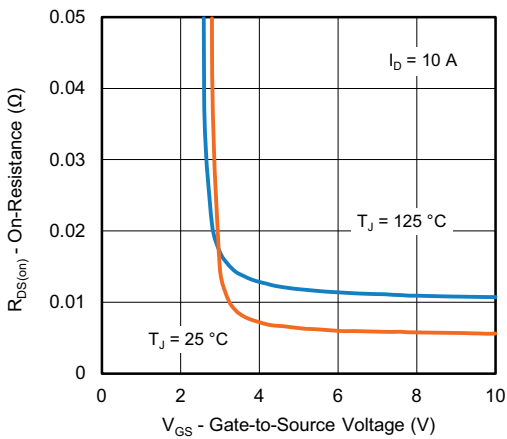
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



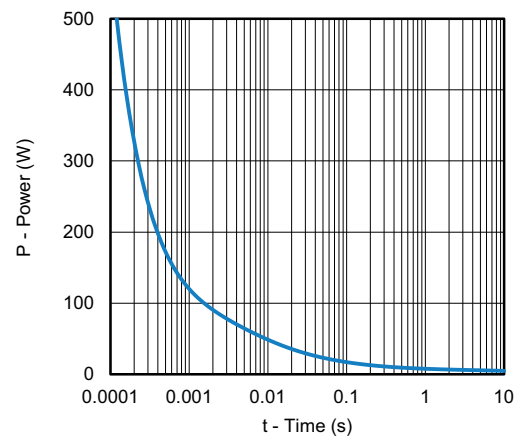
Source-Drain Diode Forward Voltage



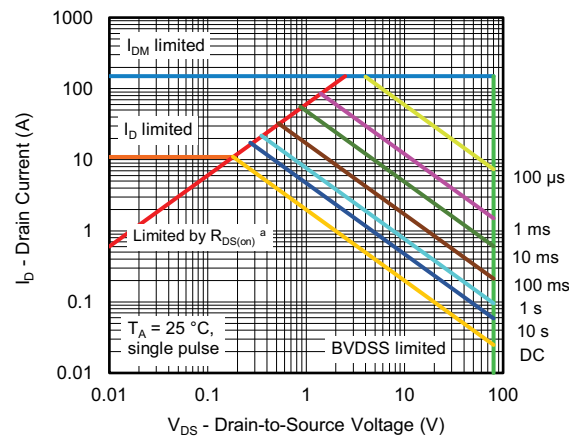
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



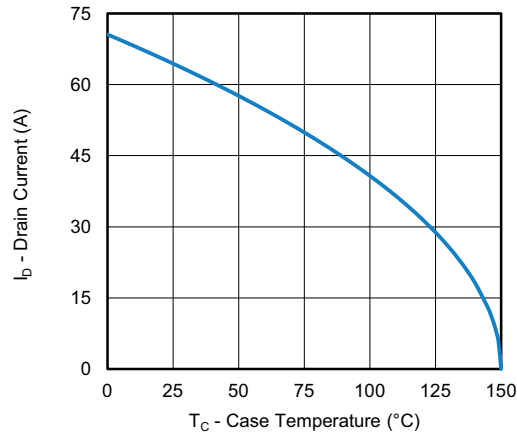
Safe Operating Area, Junction-to-Ambient

Note

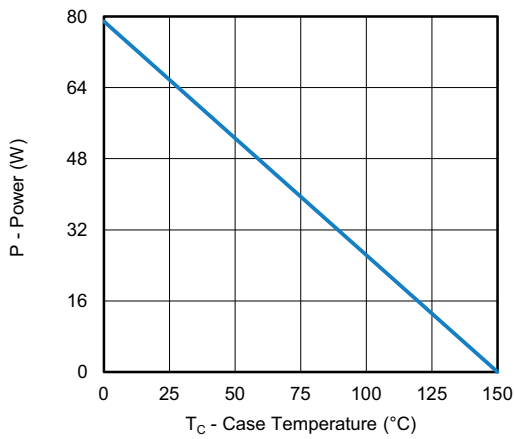
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



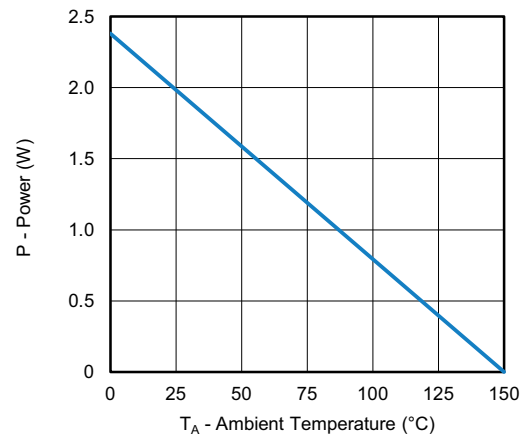
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating^a



Power, Junction-to-Case

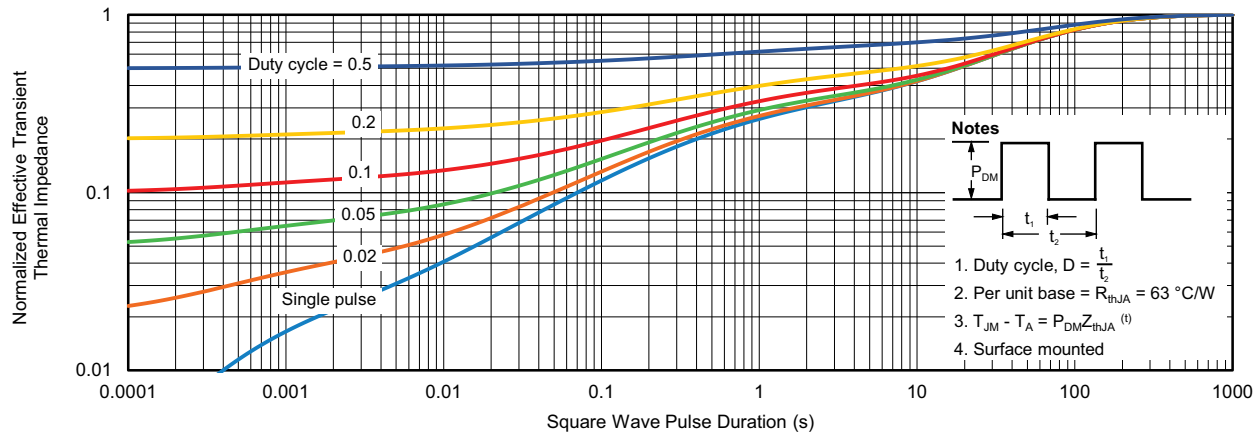


Power, Junction-to-Ambient

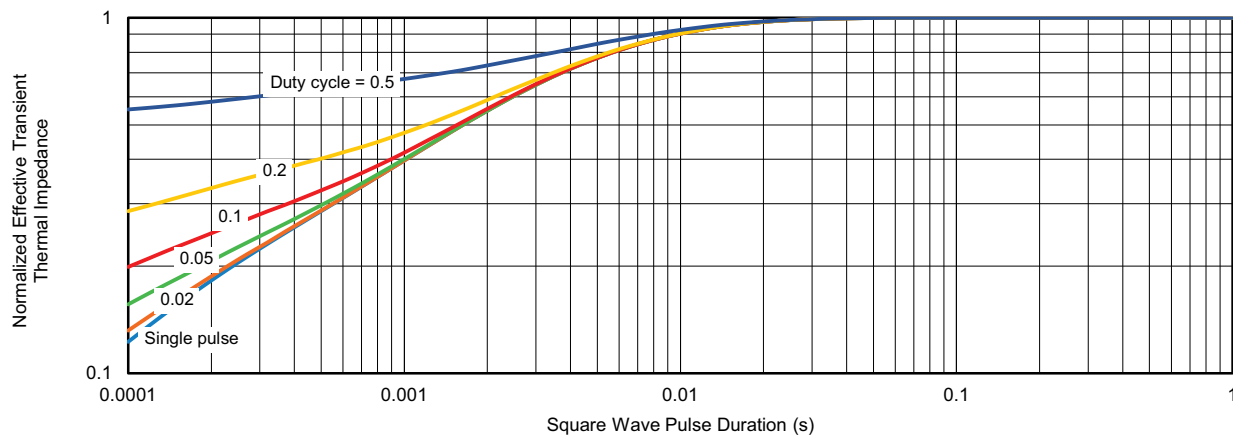
Note

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

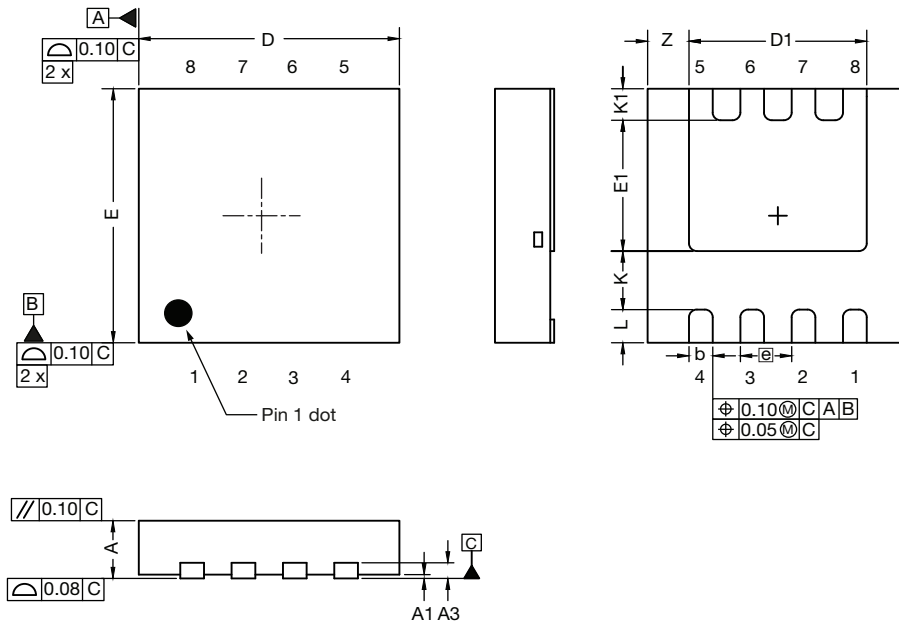


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77179.



Case Outline for PowerPAK® 1212-SWLH and PowerPAK® 1212-8SH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: S20-0930-Rev. C, 07-Dec-2020
DWG: 6062

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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