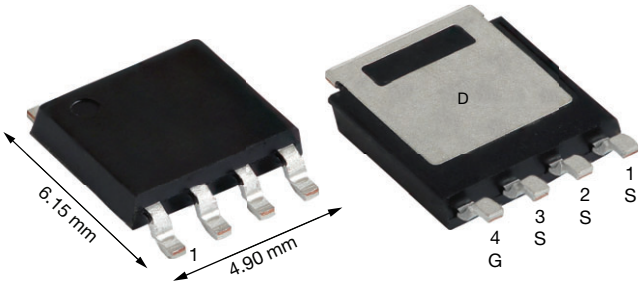
Automotive P-Channel 12 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L



Top View | Bottom View

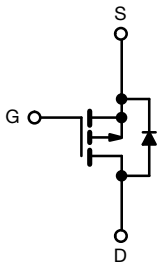
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE



P-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	-12
$R_{DS(on)}$ (Ω) at V_{GS} = -4.5 V	0.0040
$R_{DS(on)}$ (Ω) at V_{GS} = -2.5 V	0.0064
I_D (A)	-238
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ123ELP (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-12	V
Gate-source voltage [a]		V_{GS}	± 8	
Continuous drain current	T_C = 25 °C [b]	I_D	-238	A
	T_C = 125 °C		-137	
Continuous source current (diode conduction) [b]		I_S	-340	
Pulsed drain current [c]		I_{DM}	400	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	73	
Single pulse avalanche energy		E_{AS}	270	mJ
Maximum power dissipation [c]	T_C = 25 °C	P_D	375	W
	T_C = 125 °C		125	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [f]	R_{thJA}	44	°C/W
Junction-to-case (drain)		R_{thJC}	0.4	

Notes

a. Not intended for continuous use with positive gate voltage > 5.0 V
b. Package limited
c. When mounted on 1" square PCB (FR4 material)
d. See solder profile (www.vishay.com/doc?73257). For PowerPAK SO-8L, the end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

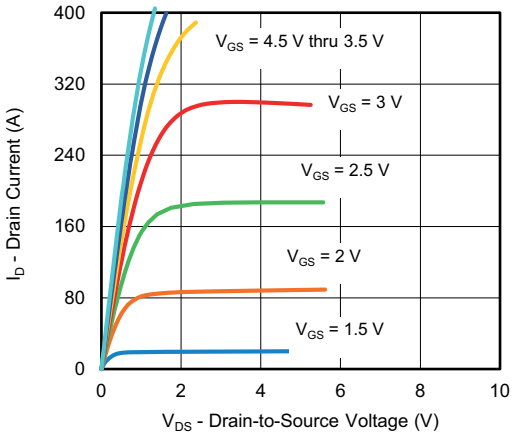
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = -250 µA		-12	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA		-0.45	-0.6	-1.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = -12 V	-	-	-1	µA
		V_{GS} = 0 V	V_{DS} = -12 V, T_J = 125 °C	-	-	-50	
		V_{GS} = 0 V	V_{DS} = -12 V, T_J = 175 °C	-	-	-150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = -4.5 V	V_{DS} ≥ -5 V	-30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -4.5 V	I_D = -10 A	-	0.0029	0.0040	Ω
		V_{GS} = -4.5 V	I_D = -10 A, T_J = 125 °C	-	-	0.0057	
		V_{GS} = -4.5 V	I_D = -10 A, T_J = 175 °C	-	-	0.0066	
		V_{GS} = -2.5 V	I_D = -10 A	-	0.0040	0.0064	
		V_{GS} = -1.8 V	I_D = -8 A	-	0.0070	0.0012	
Forward transconductance [b]	g_{fs}	V_{DS} = -6 V, I_D = -20 A		-	82	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = -6 V, f = 1 MHz	-	8342	11 680	pF
Output capacitance	C_{oss}			-	3173	4443	
Reverse transfer capacitance	C_{rss}			-	2844	3982	
Total gate charge [c]	Q_g	V_{GS} = -4.5 V	V_{DS} = -6 V, I_D = -15 A	-	120	180	nC
Gate-source charge [c]	Q_{gs}			-	15	-	
Gate-drain charge [c]	Q_{gd}			-	38	-	
Gate resistance	R_g	f = 1 MHz		1.1	2.2	3.3	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = -6 V, R_L = 0.4 Ω, I_D ≅ -15 A, V_{GEN} = -4.5 V, R_g = 1 Ω		-	31	47	ns
Rise time [c]	t_r			-	53	80	
Turn-off delay time [c]	$t_{d(off)}$			-	181	272	
Fall time [c]	t_f			-	126	189	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	-1360	A
Forward voltage	V_{SD}	I_F = -10 A, V_{GS} = 0 V		-	-0.76	-1.2	V
Body diode reverse recovery time	t_{rr}	I_F = -10 A, di/dt = 100 A/µs, V_{DD} = 9 V, R_L = 10 Ω, L = 0.1 mH		-	105	210	ns
Body diode reverse recovery charge	Q_{rr}			-	172	346	nC
Reverse recovery fall time	t_a			-	51	-	ns
Reverse recovery rise time	t_b			-	56	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-2.8	-	A

Notes

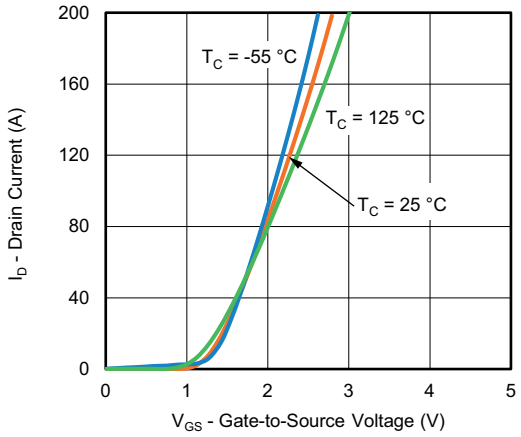
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

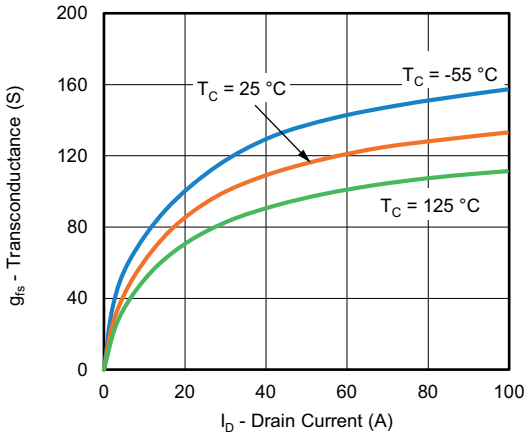
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



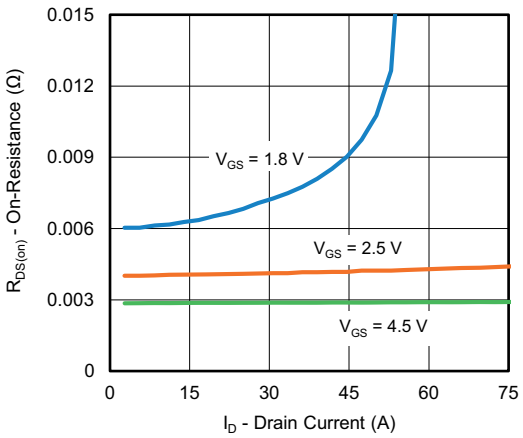
Output Characteristics



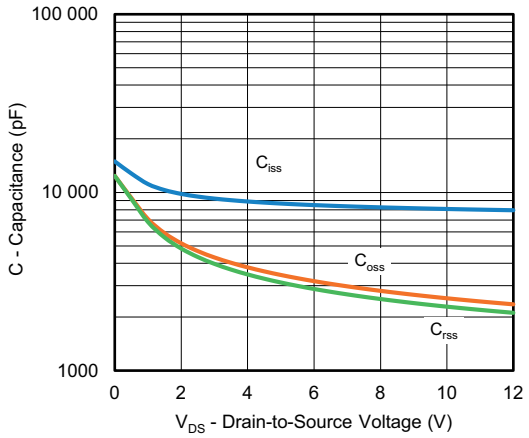
Transfer Characteristics



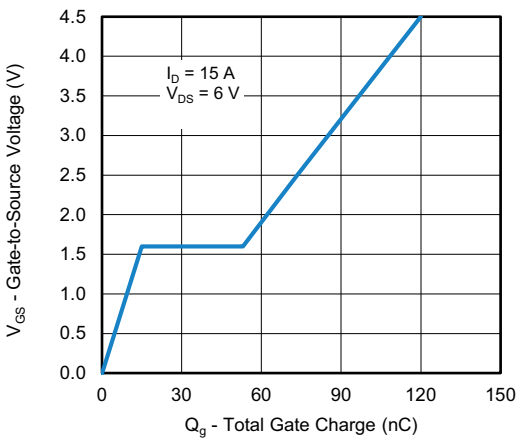
Transconductance



On-Resistance vs. Drain Current

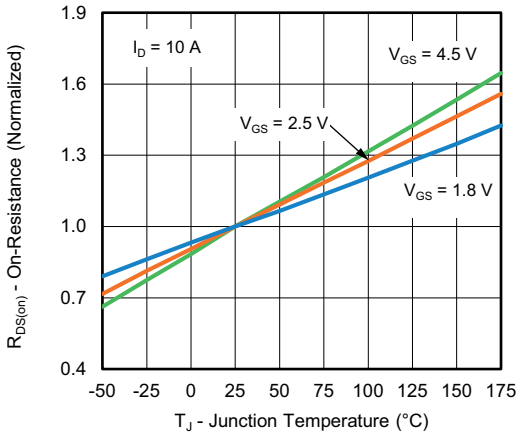


Capacitance

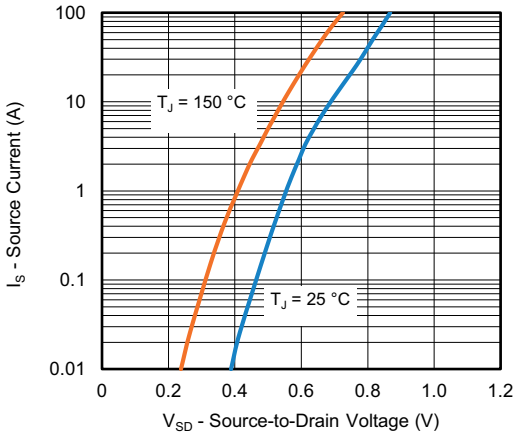


Gate Charge

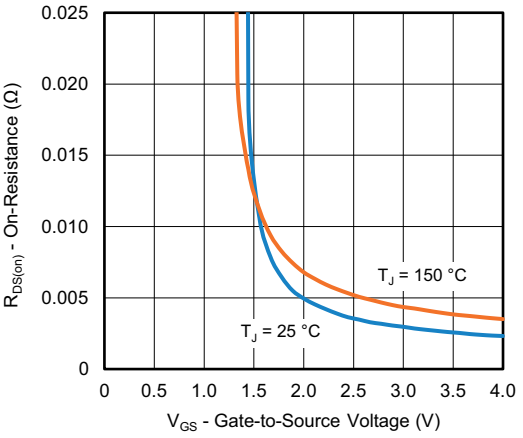
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



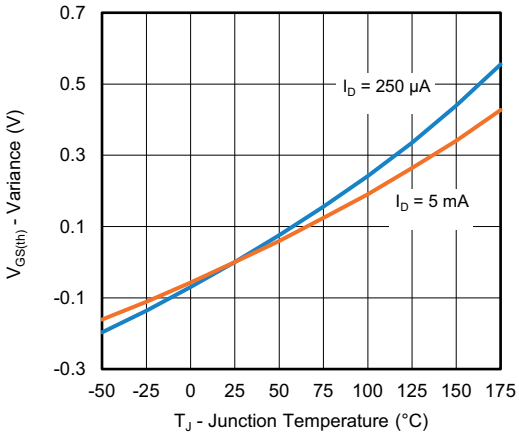
On-Resistance vs. Junction Temperature



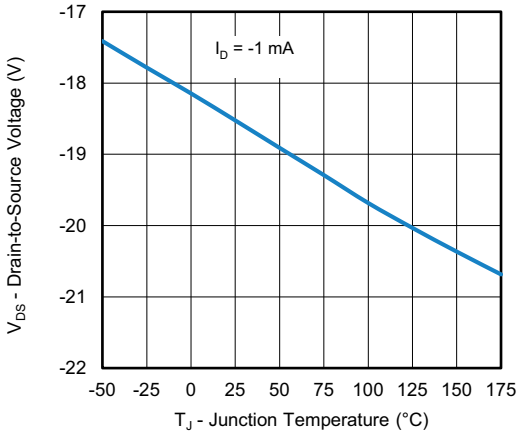
Source Drain Diode Forward Voltage



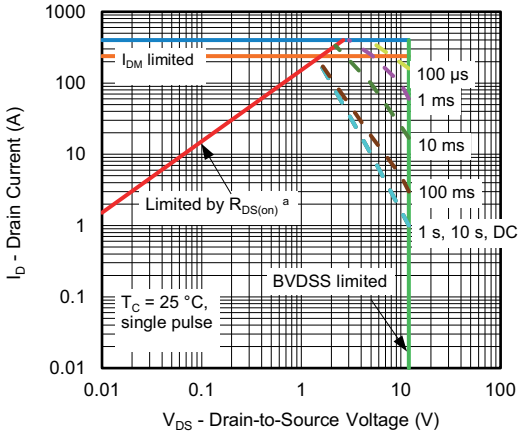
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Drain-Source Breakdown vs. Junction Temperature

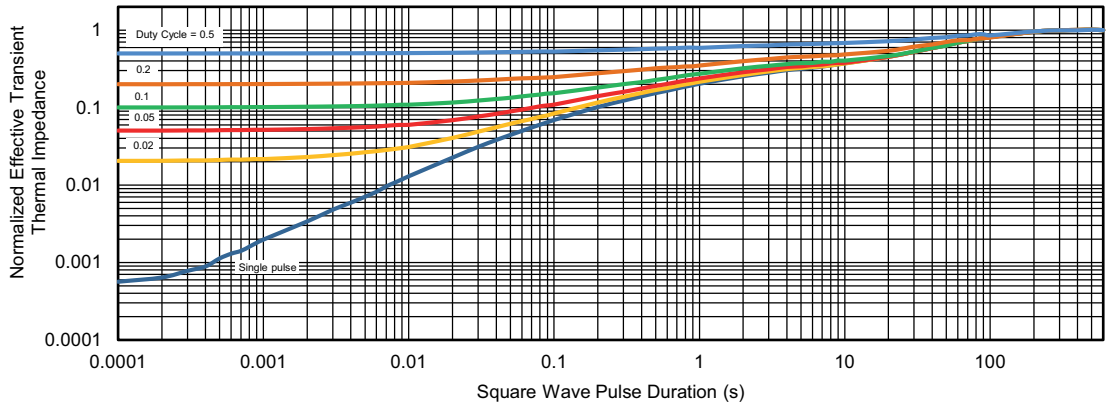


Safe Operating Area

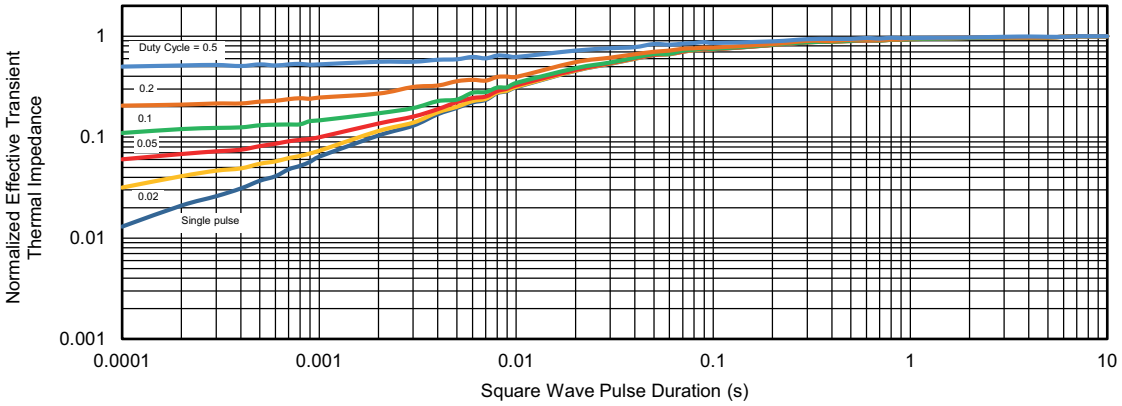
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

THERMAL RATINGS (T_C = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

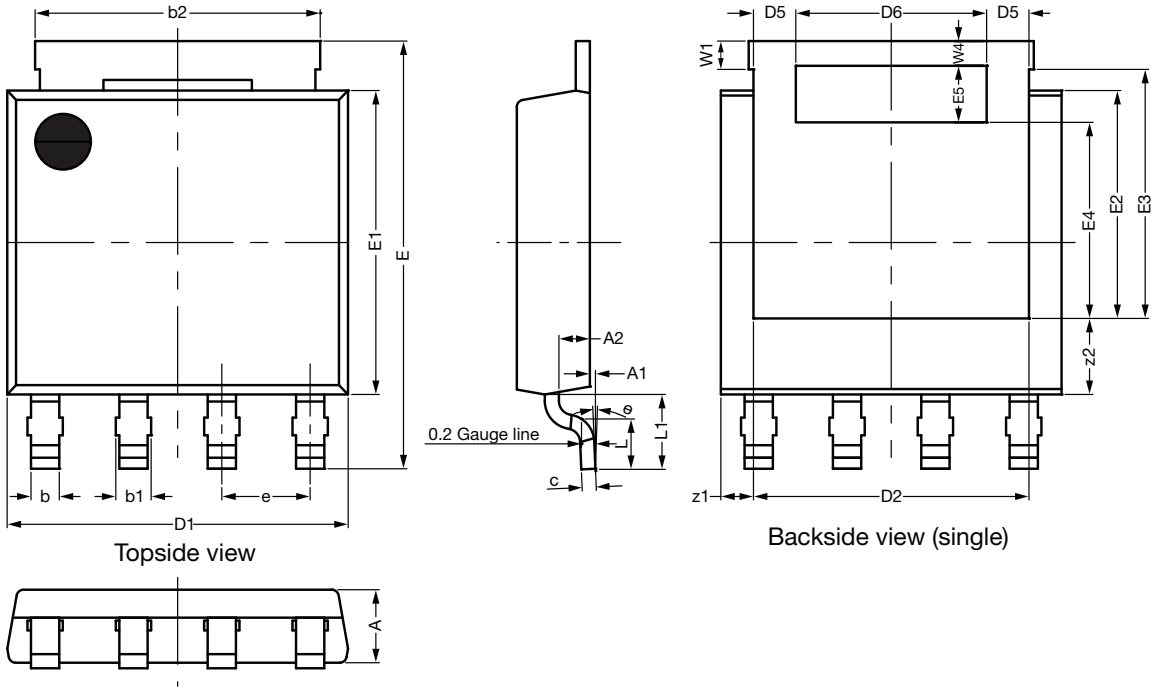
Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?79217.

PowerPAK® SO-8L Case Outline 3



Topside view

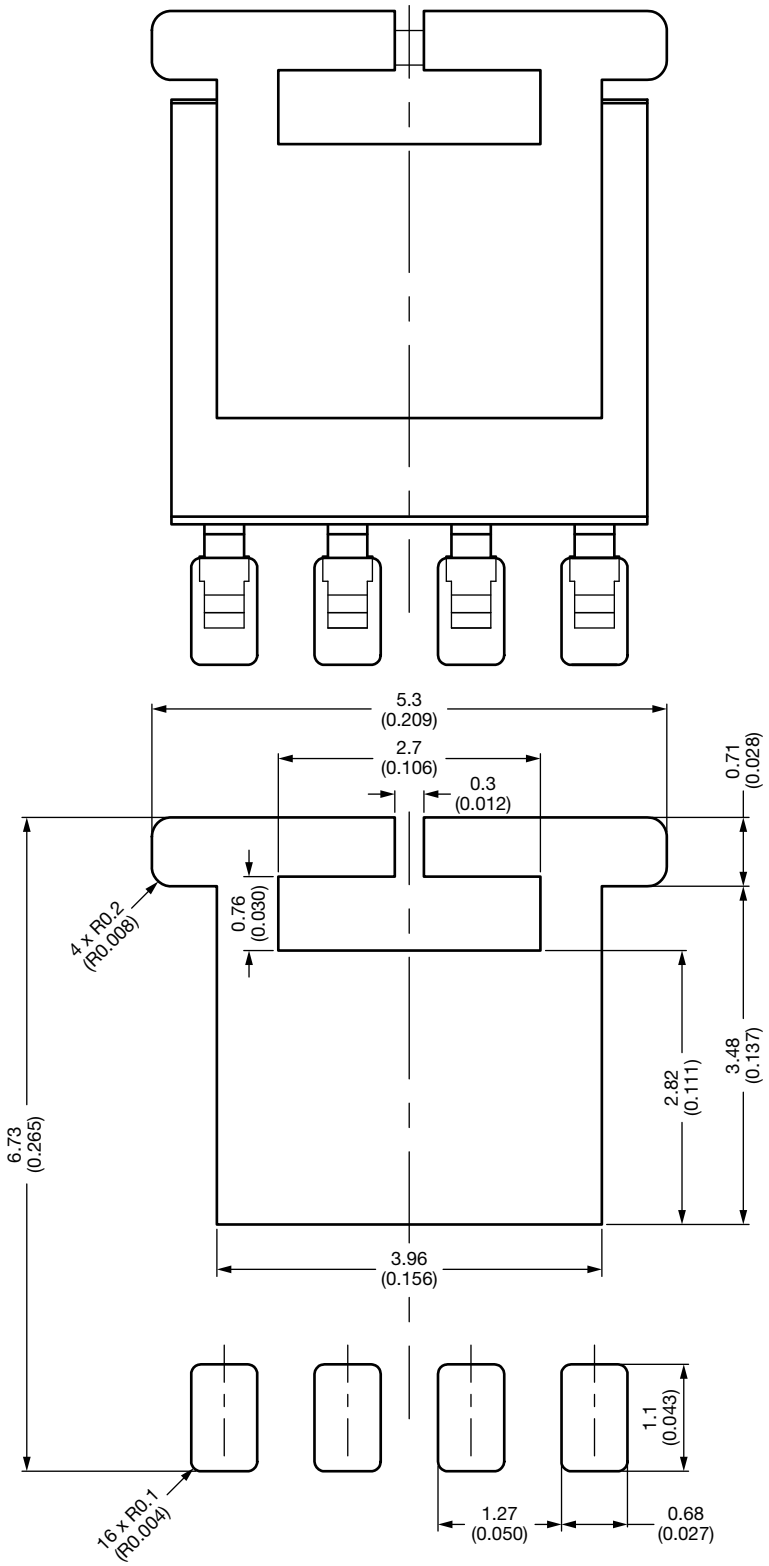
Backside view (single)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.05	1.10	0.039	0.041	0.043
A1	0.00	---	0.127	0.000	---	0.005
A2	0.40	0.45	0.50	0.016	0.018	0.020
b	0.33	0.41	0.49	0.013	0.016	0.019
b1	0.43	0.51	0.59	0.017	0.020	0.023
b2	4.00	4.10	4.20	0.157	0.161	0.165
c	0.15	0.20	0.25	0.006	0.008	0.010
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D5	0.51	0.61	0.71	0.020	0.024	0.028
D6	2.64	2.74	2.84	0.104	0.108	0.112
e		1.27 BSC			0.050 BSC	
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
E3	3.48	3.58	3.68	0.137	0.141	0.145
E4	2.72	2.82	2.92	0.107	0.111	0.115
E5	0.71	0.81	0.91	0.028	0.032	0.036
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
W1	0.31	0.41	0.51	0.012	0.016	0.020
W4	0.31	0.36	0.41	0.012	0.014	0.016
z1	0.37	0.47	0.57	0.015	0.019	0.022
z2	0.99	1.09	1.19	0.039	0.043	0.047
θ	0°	---	5°	0°	---	5°
ECN: S19-0643-Rev. B, 05-Aug-2019 DWG: 6067						

Note

- Millimeter will govern

Recommended Land Pattern PowerPAK® SO-8L Single Short Ear



Dimensions in Millimeters (Inches)

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