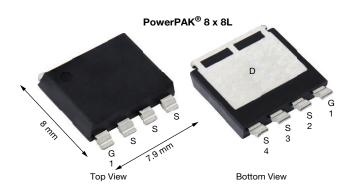
AUTOMOTIVE

Vishay Siliconix

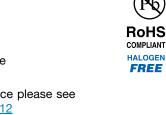
# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

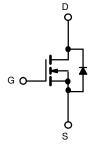


PRODUCT SUMMARY					
V <sub>DS</sub> (V)	40				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.00053				
I <sub>D</sub> (A)	701				
Configuration	Single				

#### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>q</sub> and UIS tested
- Thin 1.6 mm package
- · Very low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SQJQ140E (for detailed order number please see <a href="https://www.vishay.com/doc?79776">www.vishay.com/doc?79776</a> )

ABSOLUTE MAXIMUM RATING	(1) = 25 O, unless		1	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	40	V
Gate-source voltage		$V_{GS}$	V <sub>GS</sub> ± 20	
Continuous drain current	T <sub>C</sub> = 25 °C	1	701	A
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	405	
Continuous source current (diode conduction	on)	I <sub>S</sub>	545	
Pulsed drain current <sup>a</sup>		I <sub>DM</sub>	1820	
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	79	
Single pulse avalanche energy	L = 0.1 min	E <sub>AS</sub>	312	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C	D	600	W
	T <sub>C</sub> = 125 °C	$P_{D}$	200	VV
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperate		260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount b	$R_{thJA}$	44	°C/W
Junction-to-case (drain)		$R_{thJC}$	0.25	C/VV

#### **Notes**

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. When mounted on 1" square PCB (FR4 material)
- c. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	1			l	•			
Drain-source breakdown voltage	$V_{DS}$	V <sub>GS</sub>	= 0, I <sub>D</sub> = 250 μA	40	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.3	2.7	3.3	V	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V	-	-	1		
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	μΑ	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	150	1	
On-state drain current a	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	100	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.00044	0.00053		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.00092	Ω	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0013		
Forward transconductance b	9 <sub>fs</sub>	$V_{DS}$	= 15 V, I <sub>D</sub> = 80 A	-	160	-	S	
Dynamic <sup>b</sup>								
Input capacitance	C <sub>iss</sub>			-	12 140	17 000		
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	4740	6636	pF	
Reverse transfer capacitance	C <sub>rss</sub>			-	308	432		
Total gate charge <sup>c</sup>	$Q_g$			-	192	288		
Gate-source charge c	$Q_{gs}$	V <sub>GS</sub> = 10 V	$V_{DS} = 20 \text{ V}, I_{D} = 40 \text{ A}$	-	55	-	nC	
Gate-drain charge <sup>c</sup>	$Q_{gd}$			-	41	-		
Gate resistance	$R_g$		f = 1 MHz	0.8	1.6	2.4	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	26	39		
Rise time <sup>c</sup>	t <sub>r</sub>	V <sub>DD</sub> =	$= 20 \text{ V}, \text{ R}_{\text{L}} = 0.5 \Omega$	-	78	117		
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 40 A$ ,	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	62	93	ns	
Fall time <sup>c</sup>	t <sub>f</sub>	]		-	32	48		
Source-Drain Diode Ratings and Char	racteristics <sup>b</sup>							
Reverse recovery time	t <sub>rr</sub>	.,		-	94	188	ns	
Reverse recovery charge	Q <sub>rr</sub>	V <sub>DD</sub> = 32 V, I <sub>FM</sub> = 20 A, di/dt = 100 A/µs		-	177	354	nC	
Reverse recovery current	I <sub>RM</sub>	αιναι = 100 Ανμδ		-	-3.2	-	Α	
Pulsed current a	I <sub>SM</sub>			_	-	1600	Α	
. 4.004 04.1.01.1	Olvi							

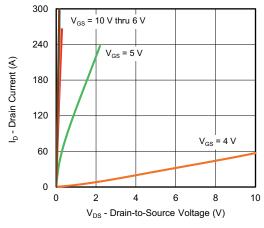
#### Notes

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

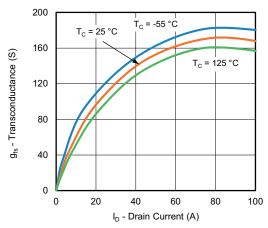
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



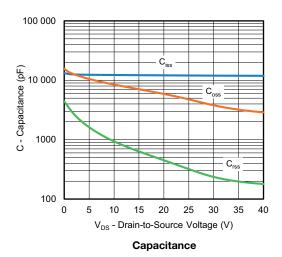
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

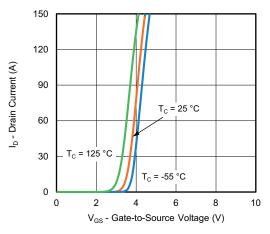


#### **Output Characteristics**

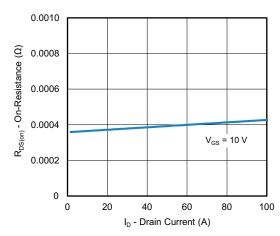


Transconductance

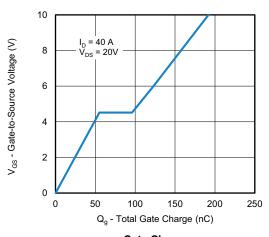




**Transfer Characteristics** 

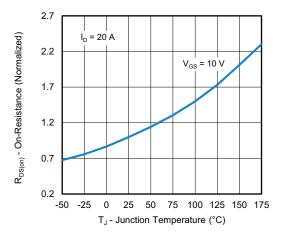


**On-Resistance vs. Drain Current** 

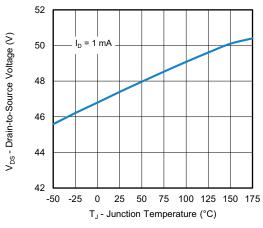




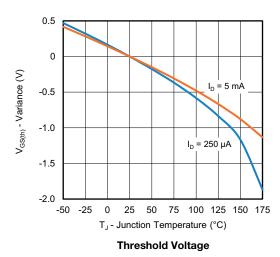
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



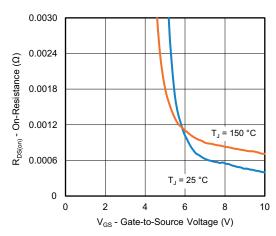
On-Resistance vs. Junction Temperature



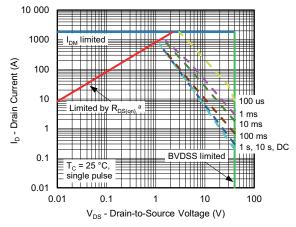
Drain Source Breakdown vs. Junction Temperature



**Source Drain Diode Forward Voltage** 



On-Resistance vs. Gate-to-Source Voltage



Safe Operating Area

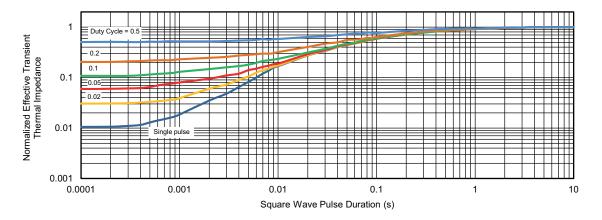
#### Note

a.  $V_{GS} > minimum V_{GS}$  at which  $R_{DS(on)}$  is specified

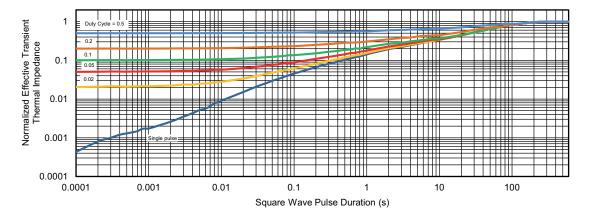
For technical questions, contact: automostech



### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Ambient



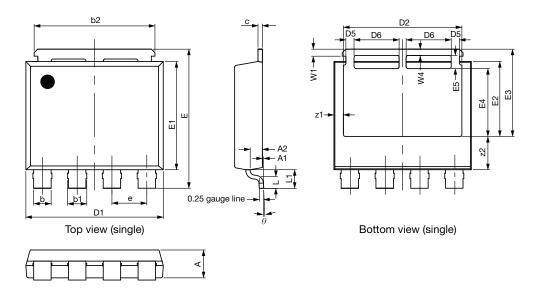
Normalized Thermal Transient Impedance, Junction-to-Case

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www.vishay.com

# PowerPAK® 8 x 8L BWL Case Outline 2



DIM	MILLIMETERS		INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α	1.50	1.60	1.70	0.059	0.063	0.067
A1	0.00	-	0.127	0.000	-	0.005
A2	0.655	0.705	0.755	0.026	0.028	0.030
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	6.84	6.94	7.04	0.269	0.273	0.277
С	0.20	0.25	0.30	0.008	0.010	0.012
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
е	1.97	2.00	2.03	0.078	0.079	0.080
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	4.21	4.31	4.41	0.166	0.170	0.174
E3	4.92	5.02	5.12	0.194	0.198	0.202
E4	3.80	3.90	4.00	0.150	0.154	0.157
E5	0.65	0.75	0.85	0.026	0.030	0.033
L	0.61	0.68	0.75	0.024	0.027	0.030
L1	1.00	1.07	1.15	0.039	0.042	0.045
W1	0.30	0.40	0.50	0.012	0.016	0.020
W4	0.32	0.37	0.42	0.013	0.015	0.017
z1	0.45	0.55	0.65	0.018	0.022	0.026
z2	1.81	1.91	2.01	0.071	0.075	0.079
θ	0°	-	5°	0°	-	5°

ECN: S19-0643-Rev. B, 05-Aug-2019

DWG: 6073

#### Note

Millimeter will govern

Revison: 05-Aug-2019 1 Document Number: 79736



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