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Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	40			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0027			
I _D (A)	100			
Configuration	Single			
Package	TO-263			



FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R_q and UIS tested
- AEC-Q101 qualified d
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



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	O S
N-Channel MOSFET	S

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	\/
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	T _C = 25 °C ^a	- I _D	100	A
Continuous Drain Current	T _C = 125 °C		98	
Continuous Source Current (Diode Condu	ction) a	I _S	100	
Pulsed Drain Current ^b		I _{DM}	400	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	70	
Single Pulse Avalanche Energy	L = U. I IIII	E _{AS}	245	mJ
Maximum Power Dissipation b	T _C = 25 °C	5 °C	157	W
iviaximum Fower Dissipation 5	T _C = 125 °C	P_{D}	52	VV
Operating Junction and Storage Temperation	T _J , T _{stg}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount c	R_{thJA}	40	°C/W		
Junction-to-Case (Drain)	Case (Drain)		0.95	C/VV		

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.



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SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V _{GS}	$V_{GS} = 0$, $I_D = 250 \mu A$		-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.5	3.0	3.5	V
Gate-Source Leakage	I_{GSS}	V _{DS} =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 40 V	-	-	1	
Zero Gate Voltage Drain Current	I_{DSS}	V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	120	-	-	Α
		V _{GS} = 10 V	I _D = 30 A	-	0.00225	0.00270	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A, T _J = 125 °C	-	-	0.00440	Ω
		V _{GS} = 10 V	I _D = 30 A, T _J = 175 °C	-	-	0.00540	
Forward Transconductance b	9 _{fs}	V_{DS}	V _{DS} = 15 V, I _D = 30 A		201	-	S
Dynamic ^b							
Input Capacitance	C _{iss}			-	6325	7910	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	744	930	pF
Reverse Transfer Capacitance	C _{rss}			-	314	395	
Total Gate Charge ^c	Qg			-	95.5	145	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_{D} = 100 \text{ A}$	-	25.5	-	nC
Gate-Drain Charge ^c	Q_{gd}			-	14.7	-	
Gate Resistance	R_g		f = 1 MHz	0.7	1.48	3.8	Ω
Turn-On Delay Time ^c	t _{d(on)}				14	21	
Rise Time ^c	t _r	V_{DD} = 20 V, R_L = 0.2 Ω $I_D \cong 100$ A, V_{GEN} = 10 V, R_g = 1 Ω		-	11	17	ns
Turn-Off Delay Time ^c	t _{d(off)}			-	48	72	
Fall Time ^c	t _f			-	9	14	
Source-Drain Diode Ratings and Characteristics b							
Pulsed Current ^a	I _{SM}			-	-	400	Α
Forward Voltage	V _{SD}	I _F = 30 A, V _{GS} = 0		-	0.8	1.5	V

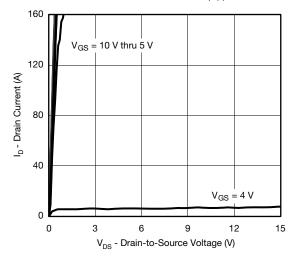
Notes

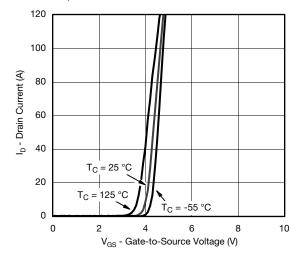
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



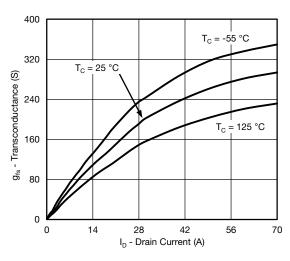
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

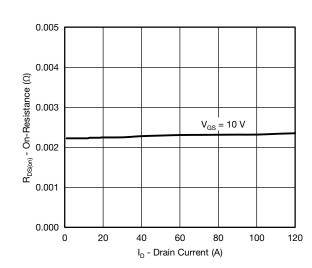




Output Characteristics

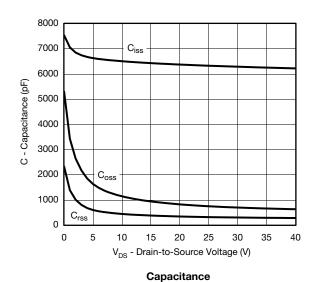


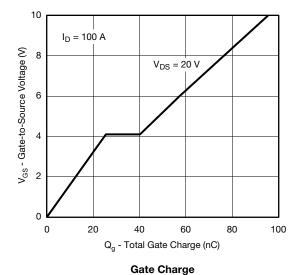




Transconductance

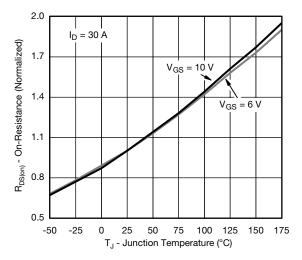
On-Resistance vs. Drain Current



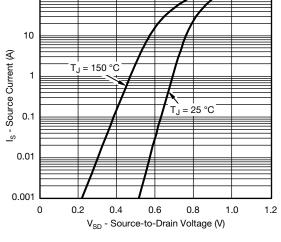




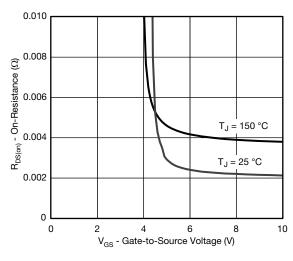
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



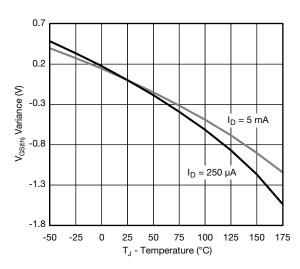
On-Resistance vs. Junction Temperature



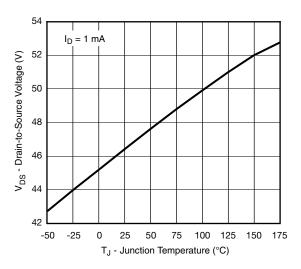
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

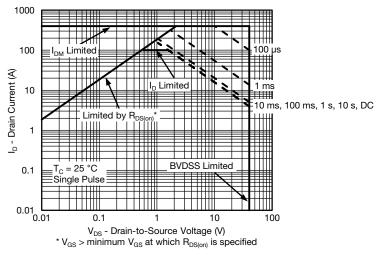


Drain Source Breakdown vs. Junction Temperature

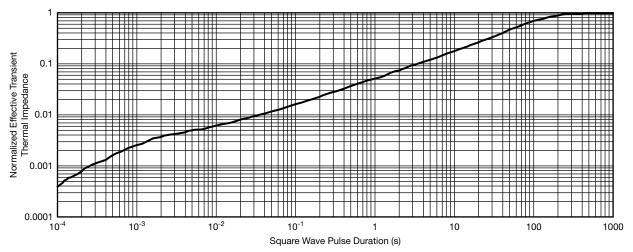
For technical questions, contact: automostech



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



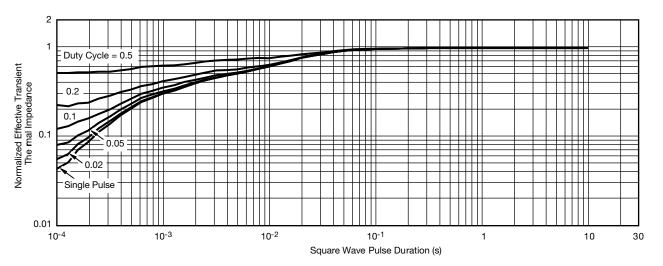
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg262769.



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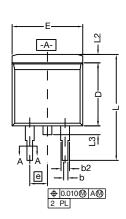
REVISION HISTORY ^a				
REVISION	DATE	DESCRIPTION OF CHANGE		
В	04-Aug-15	Revised R _g minimum limit		

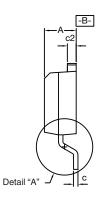
Note

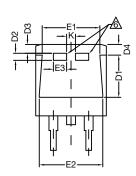
a. As of April 2014



TO-263 (D²PAK): 3-LEAD

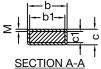








DETAIL A (ROTATED 90°)



_ 1	b	
27	ਹ <i>ੀ </i>	
c	SECTION A-4	1

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6 This feature is for thick lead.

		INCHES		MILLIMETERS		
	DIM.	MIN.	MAX.	MIN.	MAX.	
	Α	0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	Е	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	=	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100) BSC	2.54 BSC		
K		0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
	L2 0.040		0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13						

DWG: 5843





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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