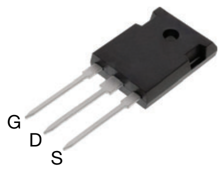
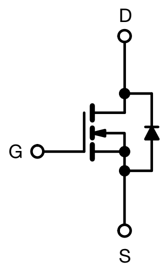
E Series Power MOSFET With Fast Body Diode

TO-247AD





N-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ typ. (Ω) at 25 °C	V_{GS} = 10 V	0.063
Q_g typ. (nC)	177	
Q_{gs} (nC)	46	
Q_{gd} (nC)	68	
Configuration	Single	

FEATURES

- Fast body diode MOSFET using E series technology
- Reduced t_{rr}, Q_{rr}, and I_{RRM}
- Low figure-of-merit (FOM): R_{on} x Q_g
- Low input capacitance (C_{iss})
- Low switching losses due to reduced Q_{rr}
- 175 °C operating temperature
- AEC-Q101 qualified
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE Available

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Automotive onboard charger
- Automotive DC/DC converter

ORDERING INFORMATION	
Package	TO-247AD
Lead (Pb)-free and halogen-free	SQW44N65EF-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	650	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	47	A
		T_C = 100 °C		34	
Pulsed drain current [a]			I_{DM}	146	
Linear derating factor				3.3	W/°C
Single pulse avalanche energy [b]			E_{AS}	596	mJ
Maximum power dissipation			P_D	500	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +175	°C
Drain-source voltage slope	T_J = 125 °C		dv/dt	100	V/ns
Reverse diode dv/dt [d]				50	
Soldering recommendations (peak temperature) [c]	for 10 s			260	°C

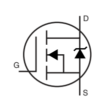
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 6.5 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, di/dt = 145 A/μs, starting T_J = 25 °C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.3	

For technical questions, contact: hvm@vishay.com

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	650	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 10 mA	-	0.7	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	μA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 520 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_J = 125 °C	-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 22 A	-	0.063	0.073	Ω
Forward transconductance [a]	g_{fs}	V_{DS} = 30 V, I_D = 22 A	-	18	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	5858	-	pF
Output capacitance	C_{oss}		-	227	-	
Reverse transfer capacitance	C_{rss}		-	6	-	
Effective output capacitance, energy related [a]	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0 V to 520 V	-	173	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$		-	710	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 22 A, V_{DS} = 520 V	-	177	266	nC
Gate-source charge	Q_{gs}		-	46	-	
Gate-drain charge	Q_{gd}		-	68	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 520 V, I_D = 22 A, R_g = 9.1 Ω, V_{GS} = 10 V	-	47	94	ns
Rise time	t_r		-	71	142	
Turn-off delay time	$t_{d(off)}$		-	206	412	
Fall time	t_f		-	66	132	
Gate input resistance	R_g	f = 1 MHz, open drain	0.5	1.0	2.0	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	47	A
Pulsed diode forward current	I_{SM}		-	-	146	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 22 A, V_{GS} = 0 V	-	0.9	1.2	V
Reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S = 22 A, di/dt = 100 A/μs, V_R = 400 V	-	190	380	ns
Reverse recovery charge	Q_{rr}		-	1.7	3.4	μC
Reverse recovery current	I_{RRM}		-	17	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

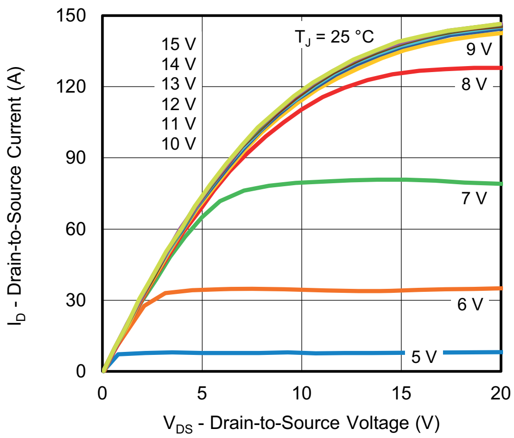


Fig. 1 - Typical Output Characteristics

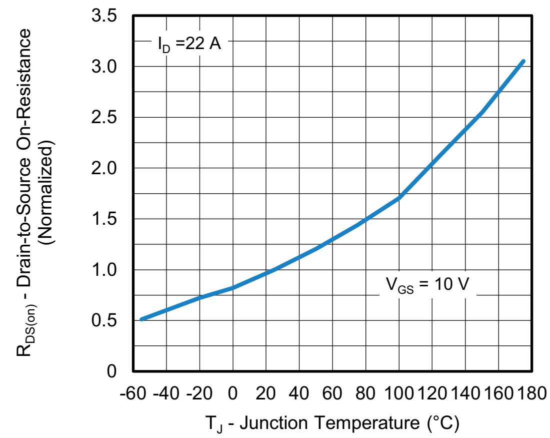


Fig. 4 - Normalized On-Resistance vs. Temperature

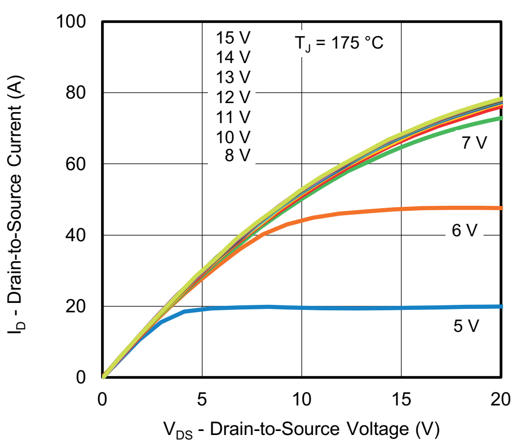


Fig. 2 - Typical Output Characteristics

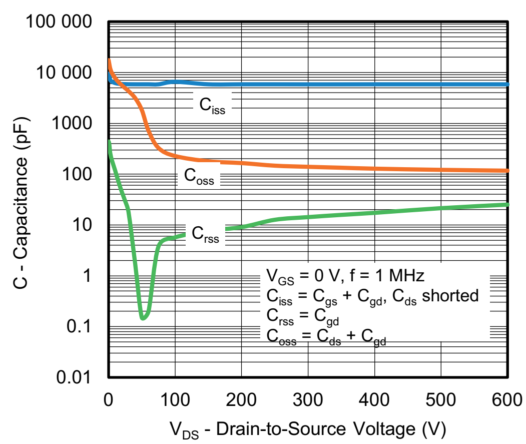


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

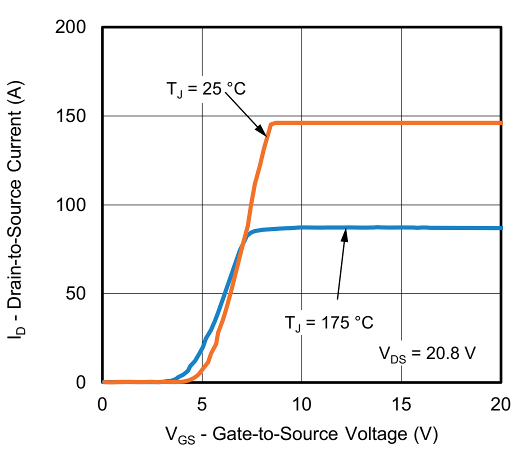


Fig. 3 - Typical Transfer Characteristics

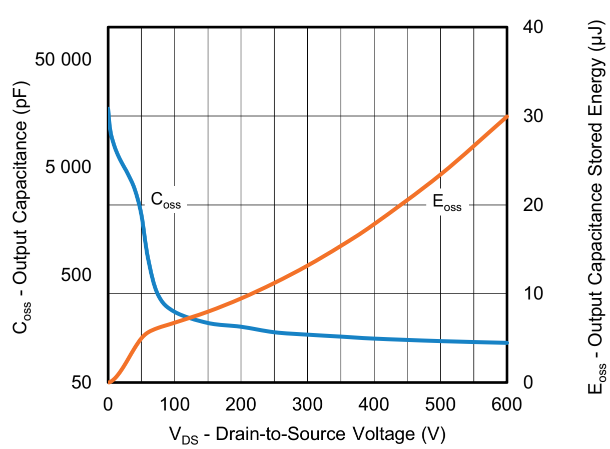


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

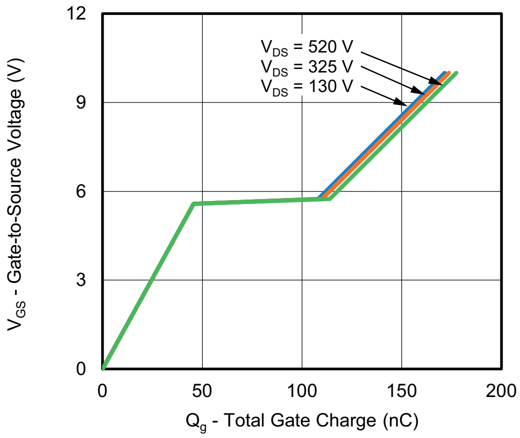


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

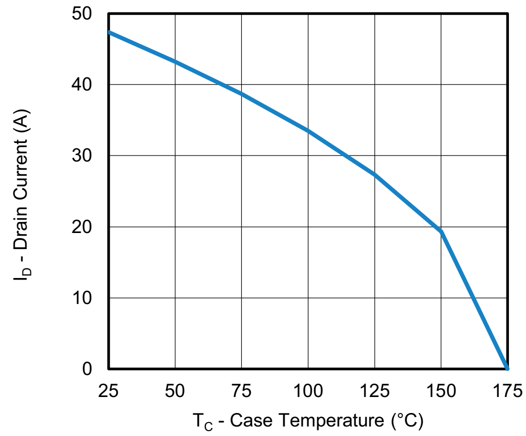


Fig. 10 - Maximum Drain Current vs. Case Temperature

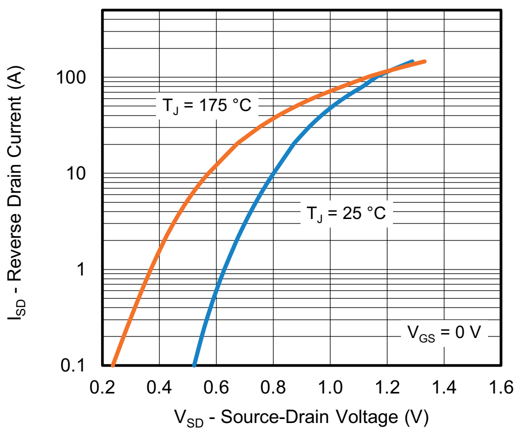


Fig. 8 - Typical Source-Drain Diode Forward Voltage

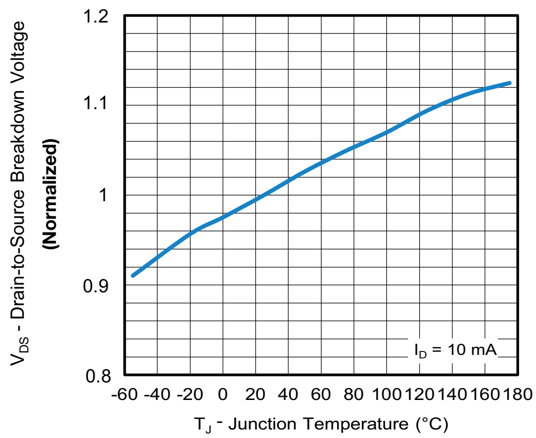


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

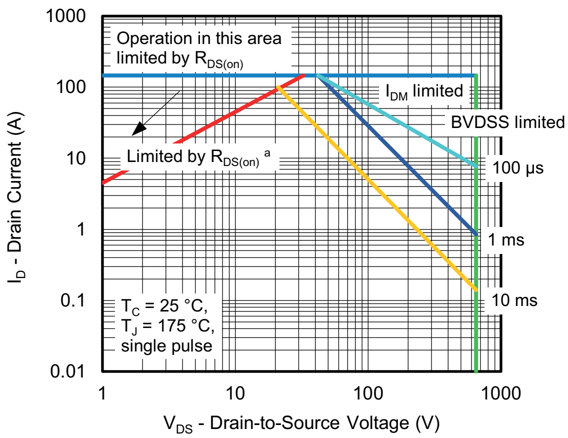


Fig. 9 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

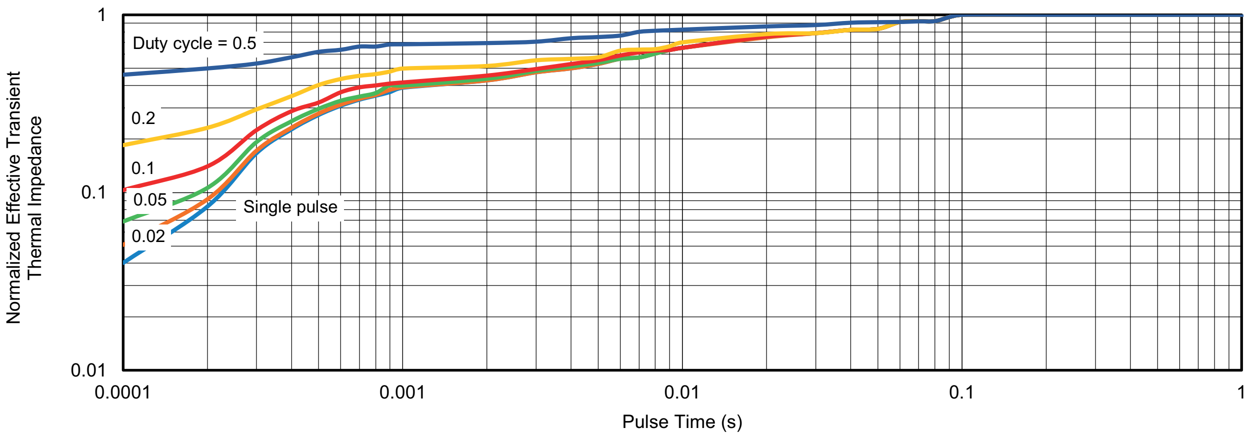


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

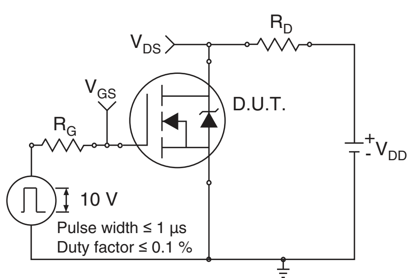


Fig. 13 - Switching Time Test Circuit

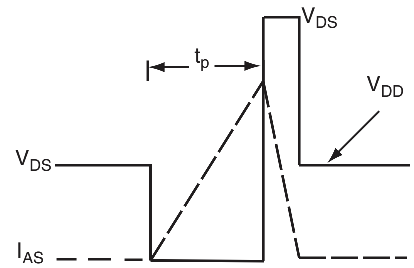


Fig. 16 - Unclamped Inductive Waveforms

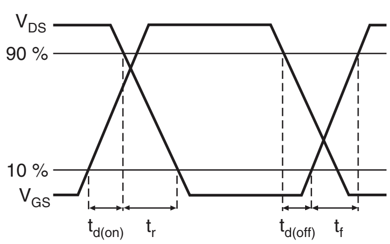


Fig. 14 - Switching Time Waveforms

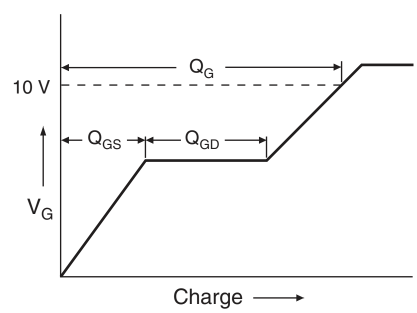


Fig. 17 - Basic Gate Charge Waveform

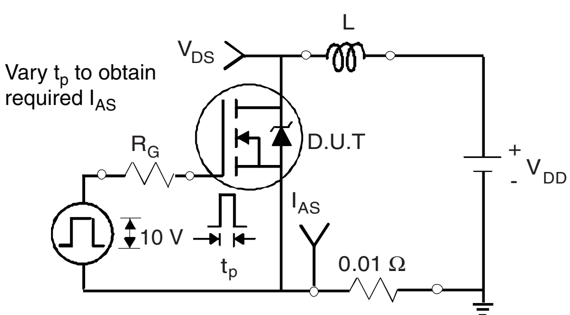


Fig. 15 - Unclamped Inductive Test Circuit

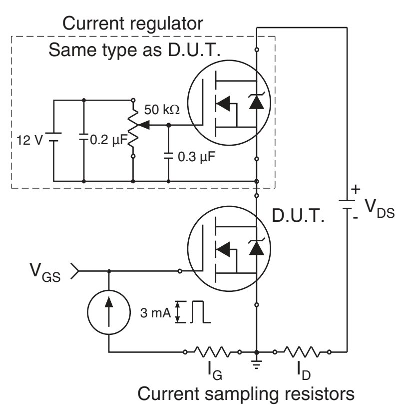
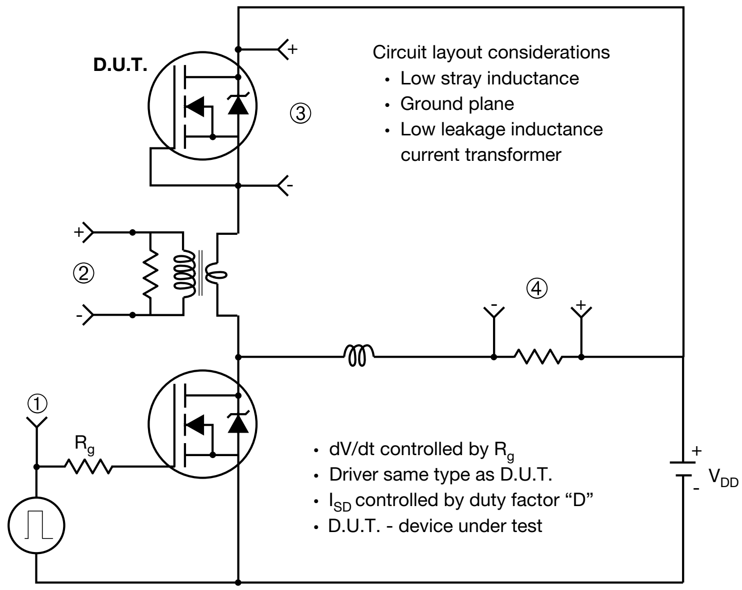
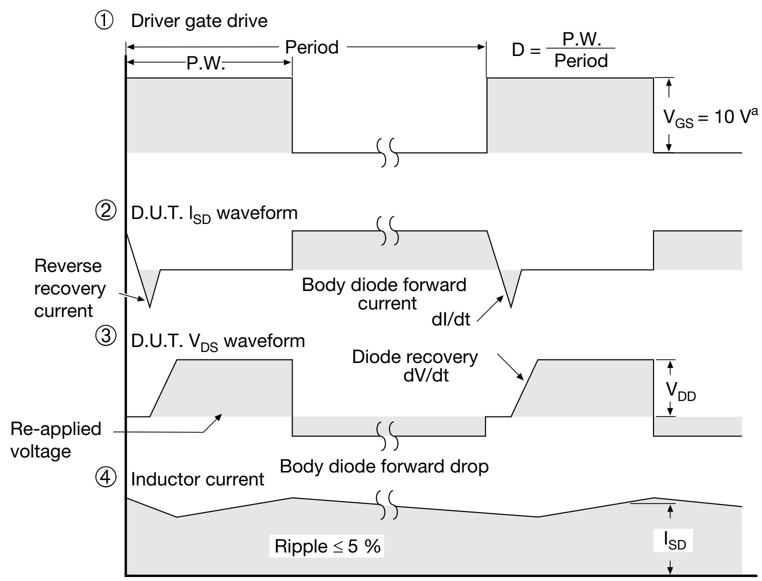


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

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