SUM50020EL

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Vishay Siliconix

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^d	Q _g (TYP.)			
60	0.0021 at V _{GS} = 10 V	120	126			
	0.0026 at V_{GS} = 4.5 V	120	120			



Ordering Information:

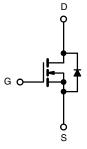
SUM50020EL-GE3 (lead (Pb)-free and halogen-free)

FEATURES

- TrenchFET[®] power MOSFET
- Maximum 175 °C junction temperature
- Q_{gd}/Q_{gs} ratio < 0.25
- Operable with logic-level gate drive
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Power supply
 Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25 \degree C$, unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-Source Voltage	V _{DS}	60	V			
Gate-Source Voltage	V _{GS}	± 20	v			
Continuous Drain Current ($T_{,1} = 150 \ ^{\circ}C$)	T _C = 25 °C	1_	120 ^d	A		
Continuous Drain Current $(1) = 130^{\circ}$ C)	T _C = 70 °C	– I _D	120 ^d			
Pulsed Drain Current (t = 100 µs)	I _{DM}	300	A			
Avalanche Current	L = 0.1 mH	I _{AS}	75			
Single Avalanche Energy ^a	L = 0.1 mm	E _{AS}	281	mJ		
Maximum Power Dissipation ^a	T _C = 25 °C	- P _D	375 ^b	W		
Maximum Power Dissipation -	T _C = 125 °C	FD	125 ^b			
Operating Junction and Storage Temperature Ra	ange	T _J , T _{stg}	-55 to +175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W		
Junction-to-Case (Drain)	R _{thJC}	0.4	C/W		

Notes

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR4 material).
- d. Package limited.

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					1 1		
Drain-Source Breakdown Voltage	V _{DS}	V_{GS} = 0 V, I_D = 250 μ A	60	-	-		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.2	-	2.5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 250	nA	
		$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	^	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125 ^{\circ}\text{C}$	-	-	150	μA	
		$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	5	mA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	120	-	-	А	
Ducia Course On Otata Decistance 3	D	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 30 \text{ A}$	-	0.0017	0.0021	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	-	0.0021	0.0026	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 30 \text{ A}$	-	145	-	S	
Dynamic ^b							
Input Capacitance	C _{iss}		-	11 113	-	pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$, $V_{DS} = 30 V$, f = 1 MHz	-	4625	-		
Reverse Transfer Capacitance	C _{rss}		-	475	-		
Total Gate Charge ^c	Qg		-	126	-	nC	
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	-	31.2	-		
Gate-Drain Charge ^c	Q _{gd}		-	7.1	-		
Gate Resistance	Rg	f = 1 MHz	0.32	1.6	3.2	Ω	
Turn-On Delay Time ^c	t _{d(on)}		-	15	30		
Rise Time ^c	tr	V_{DD} = 30 V, R_L = 5 Ω	-	20	40	ns	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 10$ Å, $V_{GEN} = 10$ V, $R_g = 1$ Ω	-	55	100		
Fall Time ^c	t _f		-	11	20		
Drain-Source Body Diode Ratings and	nd Characteria	stics ^b (T_C = 25 °C)					
Pulsed Current (t = 100 µs)	I _{SM}		-	-	300	А	
Forward Voltage ^a	V _{SD}	$I_F = 10 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.8	1.5	V	
Reverse Recovery Time	t _{rr}		-	120	180	ns	
Peak Reverse Recovery Charge	I _{RM(REC)}	I _F = 39 A, di/dt = 100 A/μs	-	5	10	А	
Reverse Recovery Charge	Q _{rr}		-	0.287	0.430	μC	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

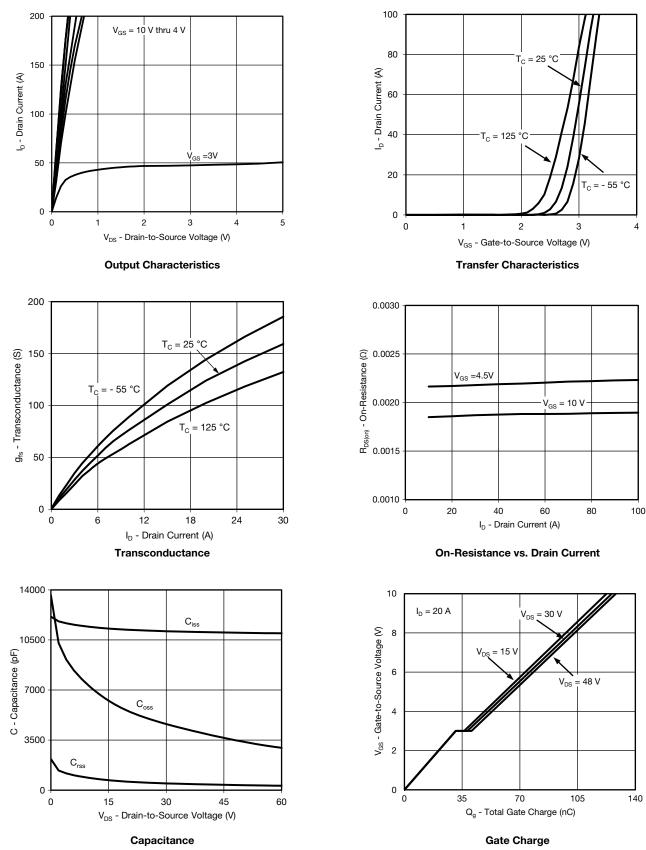
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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



S15-1868-Rev. A, 10-Aug-15

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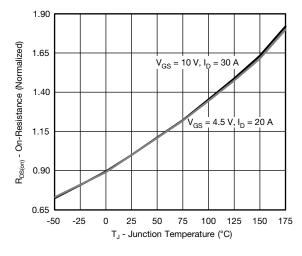
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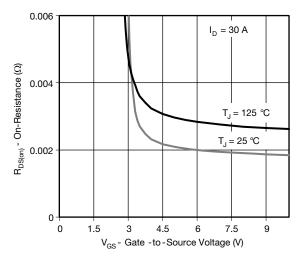


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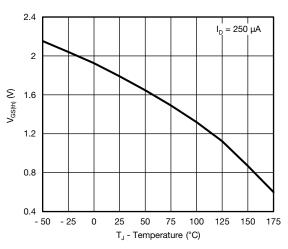
TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



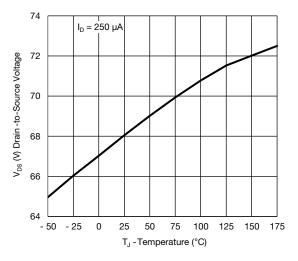
On-Resistance vs. Junction Temperature



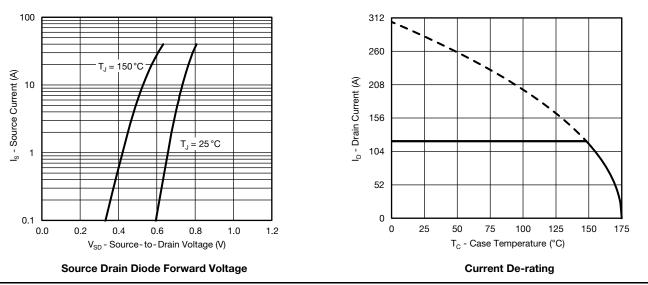
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



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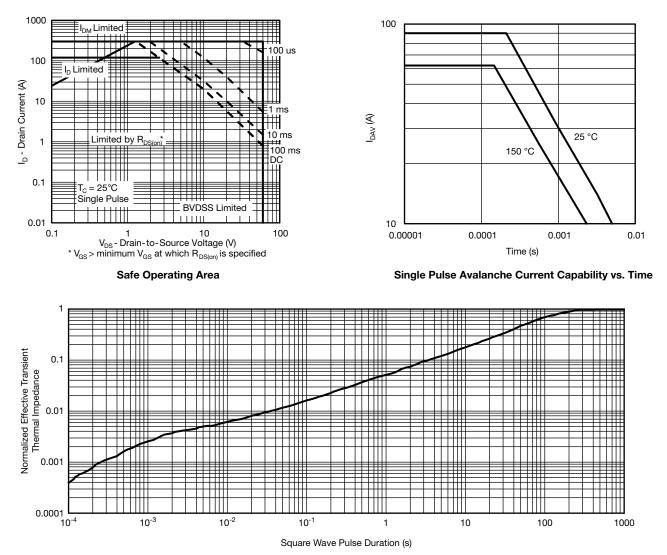
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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)

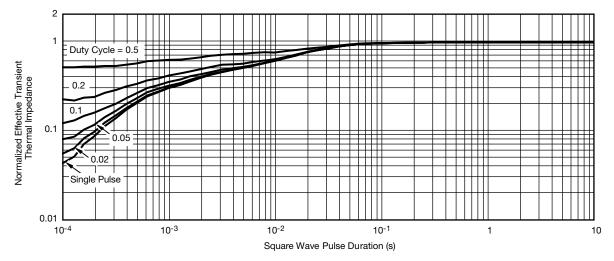


Normalized Thermal Transient Impedance, Junction-to-Ambient



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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction to Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction to Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

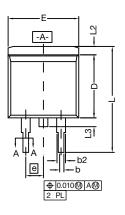
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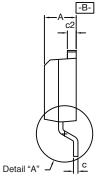
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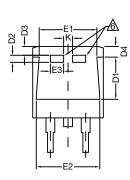


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TO-263 (D²PAK): 3-LEAD

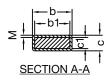








DETAIL A (ROTATED 90°)



		INCHES		MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
А		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
с*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100	0.100 BSC		BSC	
	К	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
	L1	0.090	0.110	2.286	2.794	
	L2	0.040	0.055	1.016	1.397	
	L3	0.050	0.070	1.270	1.778	
	L4	0.010 BSC 0.254 I		BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843						

Notes

- 1. Plane B includes maximum features of heat sink tab and plastic. 2. No more than 25 % of L1 can fall above seating plane by
- max. 8 mils.3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB.
 - Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

This feature is for thick lead.

Revison: 30-Sep-13



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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