Vishay Siliconix

HALOGEN

FREE

P-Channel 80 V (D-S) MOSFET



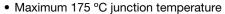
PRODUCT SUMMARY					
V _{DS} (V)	-80				
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0058				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	0.0081				
Q _g typ. (nC)	145				
I _D (A)	-150				
Configuration	Single				

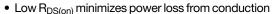
ORDERING INFORMATION

Package

FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance





- · Compatible with logic-level gate driving
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

281 375

125

-55 to +175

W

°C

APPLICATIONS

- Battery protection
- Motor drive control

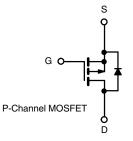
 E_{AS}

 P_D

 T_J, T_{stq}

· Load switch

TO-220AB



Lead (Pb)-free and halogen-free	SUP600	61EL-GE3			
ABSOLUTE MAXIMUM RATINGS	$(T_C = 25 ^{\circ}C, \text{ unless otherw})$	vise noted)			
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	-80	V	
Gate-source voltage		V _{GS}	± 20	V	
Continuous drain current ^d (T _J = 175 °C)	T _C = 25 °C		-150 ^d		
	T _C = 70 °C	I _D	-150 ^d		
Pulsed drain current (100 μs)		I _{DM}	-250	A	
Avalanche current		I _{AS}	-75		
C:	L = 0.1 mH		001	1	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^b	R _{thJA}	40	°C/W
Junction-to-case		R _{th} IC	0.4]

 $T_C = 25 \, ^{\circ}C \, ^{c}$

 $T_C = 125 \, ^{\circ}C^{\ b}$

Notes

a. Duty cycle ≤ 1 %

Power dissipation

b. When mounted on 1" square PCB (FR4 material)

Operating junction and storage temperature range

c. See SOA curve for voltage derating

Single pulse avalanche energy a

d. Limited by package



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -10 \text{ mA}$	-80	-	-		
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1.5	-	-2.5	V	
Gate-body leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
		V _{DS} = -80 V, V _{GS} = 0 V	-	-	-1		
Zero gate voltage drain current	I _{DSS}	V _{DS} = -80 V, V _{GS} = 0 V, T _J = 125 °C	-	-	-50	μА	
		V _{DS} = -80 V, V _{GS} = 0 V, T _J = 175 °C	ı	-	-250		
On-state drain current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	-30	-	-	Α	
Duain accuracy on atota vaciations 2	Б	V _{GS} = -10 V, I _D = -20 A	-	0.0048	0.0058		
Drain-source on-state resistance a	R _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -15 \text{ A}$	-	0.0065	0.0081	Ω	
Forward transconductance ^a	9fs	V _{DS} = -15 V, I _D = -15 A	-	80	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	9600	-	pF	
Output capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = -40 \text{ V}, f = 1 \text{ MHz}$	-	3300	-		
Reverse transfer capacitance	C _{rss}		-	110	-		
Total gate charge ^c	Qg		-	145	218		
Gate-source charge ^c	Q _{gs}	$V_{DS} = -40 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -110 \text{ A}$	-	34	-	nC	
Gate-drain charge ^c	Q_{gd}		-	16	-		
Gate resistance	Rg	f = 1 MHz	0.46	2.3	4.6	Ω	
Turn-on delay time ^c	t _{d(on)}		-	25	35		
Rise time ^c	t _r	$V_{DD} = -40 \text{ V}, R_L = 0.71 \Omega$	-	20	30		
Turn-off delay time ^c	t _{d(off)}	$I_D \cong -20 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$	-	90	140	ns	
Fall time ^c	t _f		-	20	30		
Drain-Source Body Diode Characte	ristics (T _C = 25	5 °C b)					
Continuous current	Is		ı	-	-150	. ^	
Pulsed current	I _{SM}		-	-	-250	Α	
Forward voltage ^a	V _{SD}	I _F = -10 A, V _{GS} = 0 V	i	-0.8	-1.5	V	
Reverse recovery time	t _{rr}		ı	90	135	ns	
Peak reverse recovery charge	I _{RM(REC)}	I _F = -20 A, dl/dt = 100 A/μs	-	-2.8	-4.2	Α	
Reverse recovery charge	Q _{rr}		-	145	218	nC	

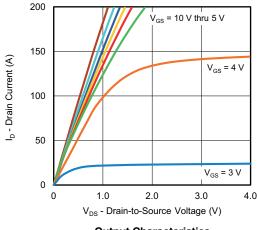
Notes

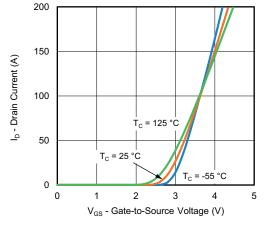
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



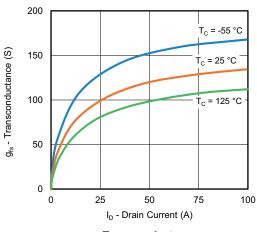
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

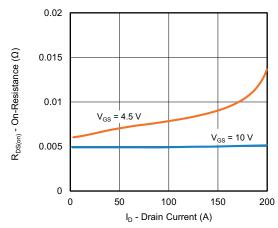




Output Characteristics

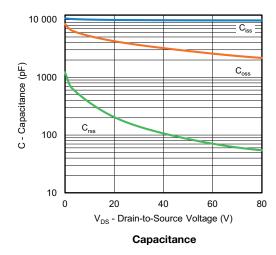


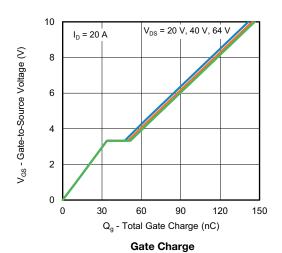




Transconductance

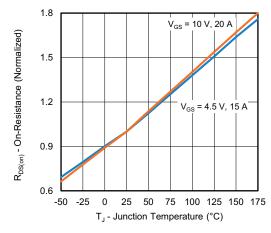
On-Resistance vs. Drain Current



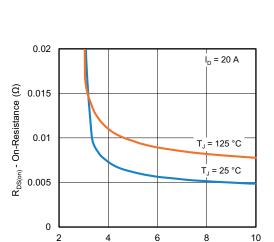




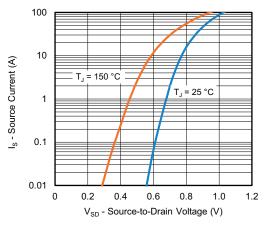
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



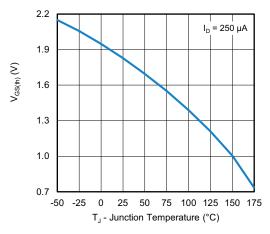
On-Resistance vs. Junction Temperature



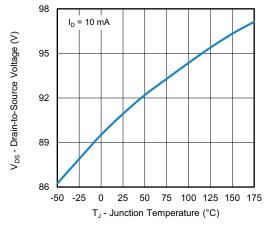
 $\label{eq:VGS} V_{GS} \text{ - Gate-to-Source Voltage (V)}$ On-Resistance vs. Gate-to-Source Voltage



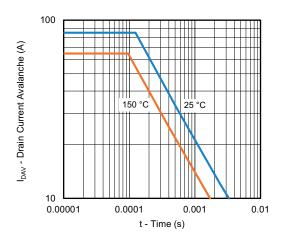
Source Drain Diode Forward Voltage



Threshold Voltage



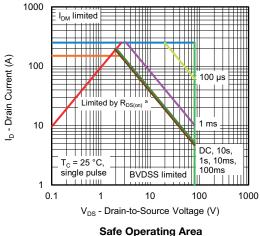
Drain Source Breakdown vs. Junction Temperature



Avalanche Current vs. Time



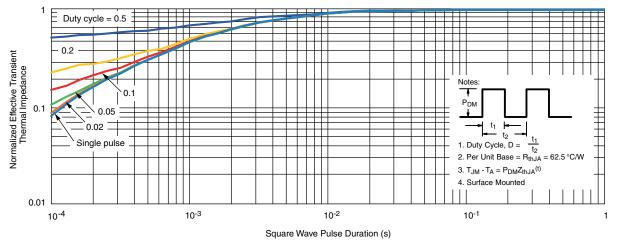
THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Sare Operat

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63020.



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TO-220AB



	D2

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
С	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
Е	10.04	10.51	0.395	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
ØΡ	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: T14-0413-Rev. P, 16-Jun-14 DWG: 5471				

Note

 $^{^{\}star}$ M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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