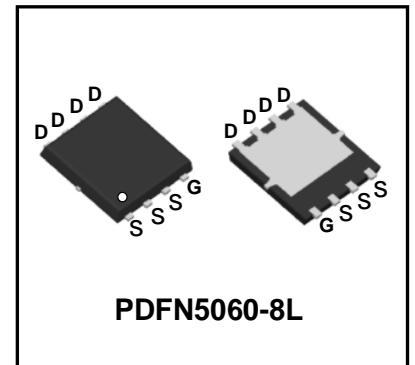


120V N-Channel Enhancement Mode Power MOSFET

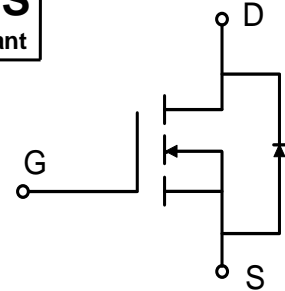
Description

WMB072N12LG2 uses Wayon's 2nd generation power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.



Features

- $V_{DS} = 120V$, $I_D = 90A$ (Silicon Limited)
 $R_{DS(on)} < 7.2m\Omega @ V_{GS} = 10V$
- Green Device Available
- 100% EAS Guaranteed
- Optimized for High Speed Smooth Switching



Applications

- Hard Switching and High Speed Circuit
- DC/DC Conversion
- Synchronous Rectification in SMPS

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹ (Silicon Limited)	I_D	$T_C=25^\circ C$	90
		$T_C=100^\circ C$	60
Continuous Drain Current ¹ (Package Limited)		$T_C=25^\circ C$	60
Pulsed Drain Current ²	I_{DM}	310	A
Single Pulse Avalanche Energy ³	EAS	460	mJ
Total Power Dissipation ⁴	P_D	110	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ¹	$R_{\theta JA}$	56	$^\circ C/W$
Thermal Resistance from Junction-to-Case ¹	$R_{\theta JC}$	1.2	$^\circ C/W$

Electrical Characteristics $T_c = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static Characteristics							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	120	-	-	V	
Gate-body Leakage Current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	$T_J=25^\circ\text{C}$	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$	-	-	1	μA
	$T_J=100^\circ\text{C}$			-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.4	2	2.5	V	
Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	5.7	7.2	m Ω	
		$V_{GS} = 4.5V, I_D = 20A$	-	7.0	10		
Forward Transconductance	g_{fs}	$V_{DS} = 5V, I_D = 20A$	-	76	-	S	
Dynamic Characteristics							
Input Capacitance	C_{iss}	$V_{DS} = 50V, V_{GS} = 0V, f = 1\text{MHz}$	-	3725	-	μF	
Output Capacitance	C_{oss}		-	985	-		
Reverse Transfer Capacitance	C_{rss}		-	20	-		
Switching Characteristics							
Gate Resistance	R_g	$V_{DS} = 0V, V_{GS} = 0V, f = 1\text{MHz}$	-	2.5	-	Ω	
Total Gate Charge	Q_g	$V_{GS} = 4.5V, V_{DD} = 60V, I_D = 20A$	-	19.2	-	nC	
Total Gate Charge	Q_g	$V_{GS} = 10V, V_{DD} = 60V, I_D = 20A$	-	43	-		
Gate-Source Charge	Q_{gs}		-	7.7	-		
Gate-Drain Charge	Q_{gd}		-	6.7	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 60V, R_G = 10\Omega, I_D = 20A$	-	14.4	-	nS	
Rise Time	t_r		-	7.7	-		
Turn-Off Delay Time	$t_{d(off)}$		-	29	-		
Fall Time	t_f		-	8.6	-		
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ²	V_{SD}	$I_S = 20A, V_{GS} = 0V$	-	-	1.2	V	
Reverse Recovery Time	t_{rr}	$V_R = 60V, I_F = 20A, dI_F/dt = 500A/\mu s$	-	46	-	ns	
Reverse Recovery Charge	Q_{rr}		-	278	-	nC	

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.4mH, I_{AS}=48A$
- The power dissipation is limited by 150°C junction temperature

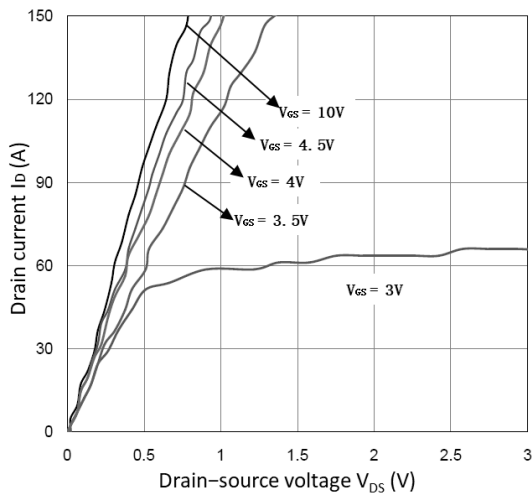


Figure 1. Output Characteristics

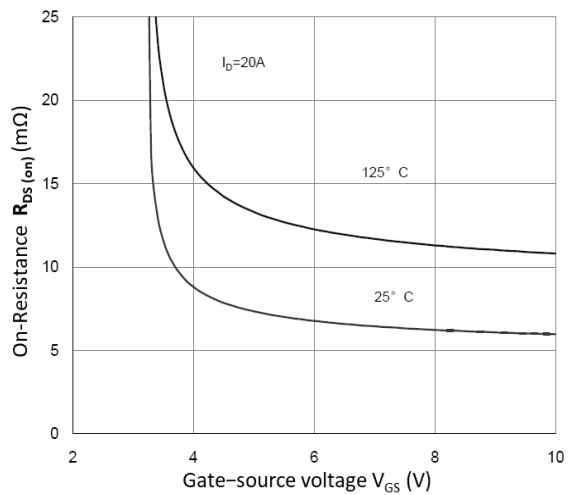


Figure 2. $R_{DS(on)}$ vs. V_{GS}

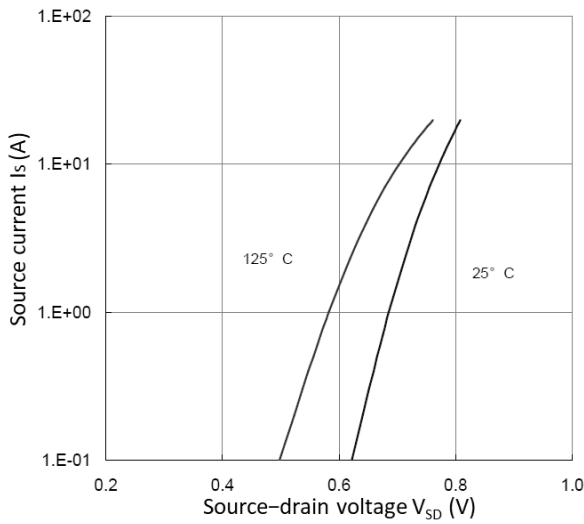


Figure 3. Forward Characteristics of Reverse

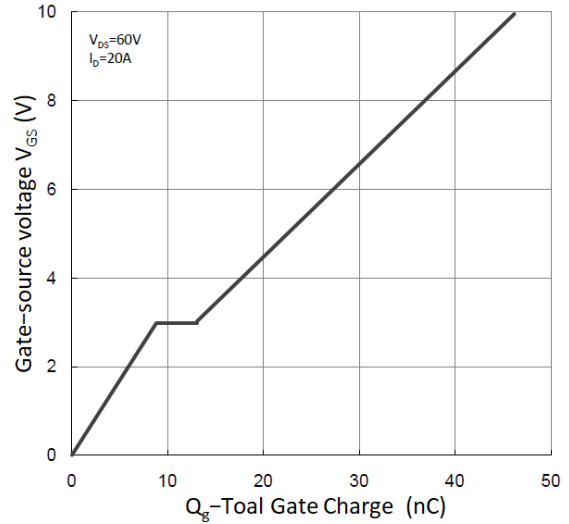


Figure 4. Gate Charge Characteristics

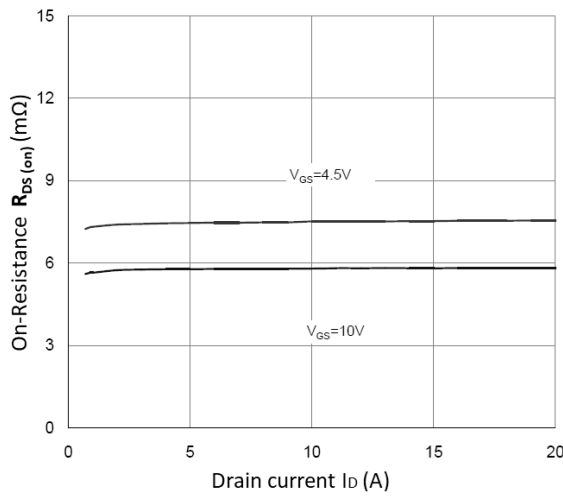


Figure 5. $R_{DS(on)}$ Vs I_D

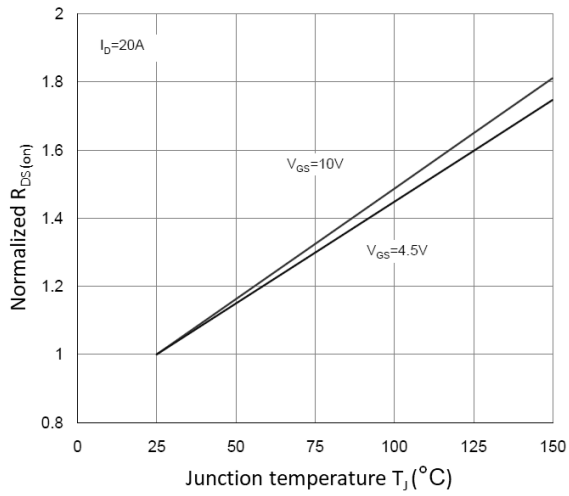


Figure 6. Normalized $R_{DS(on)}$ vs. T_J

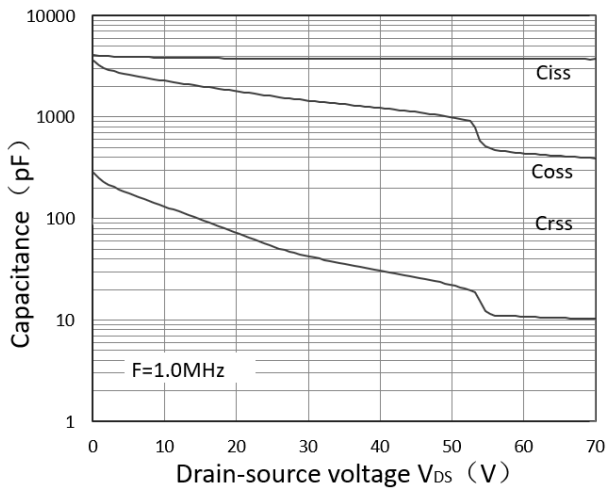


Figure 7. Capacitance Characteristics

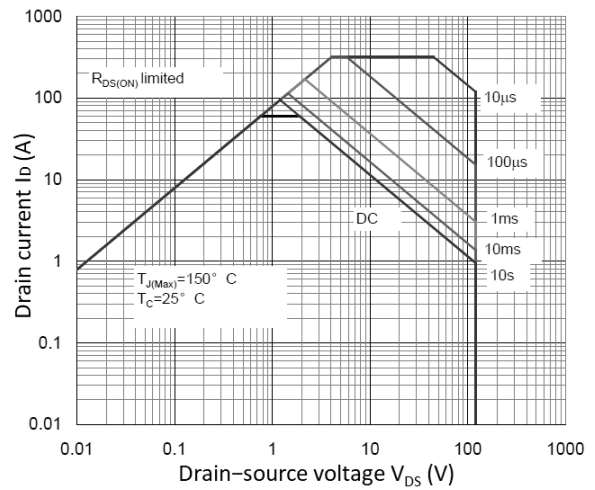


Figure 8. Safe Operating Area

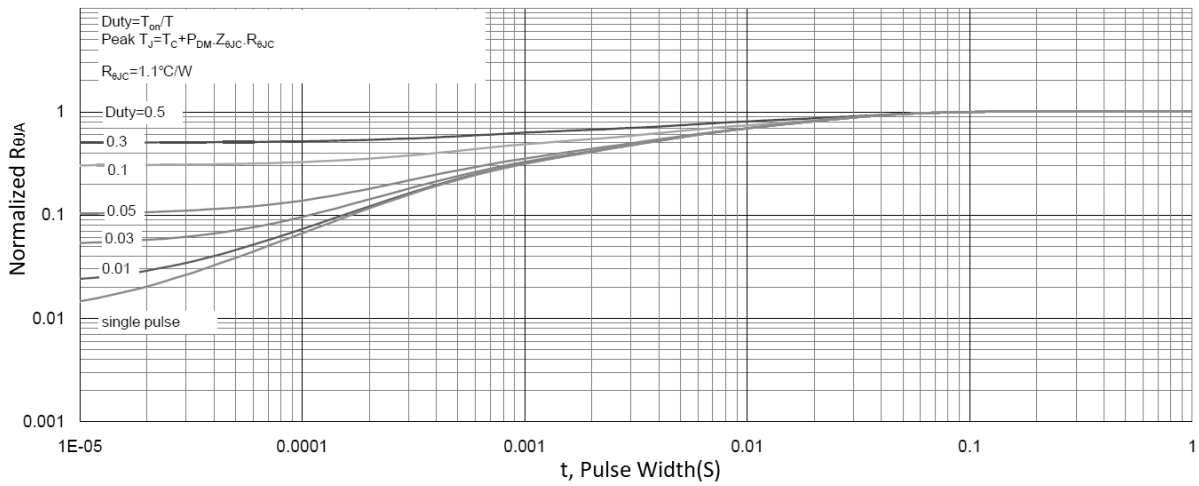


Figure 9. Normalized Maximum Transient Thermal Impedance

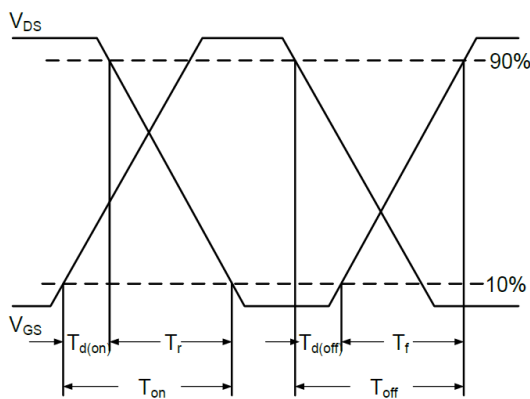


Figure 10. Switching Time Waveform

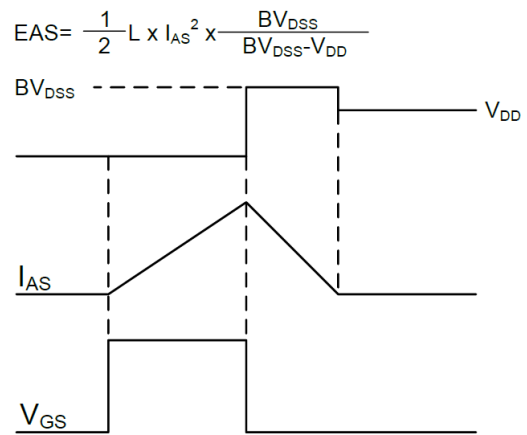
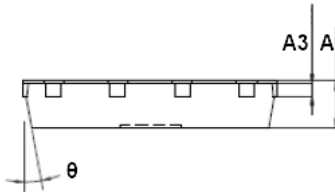
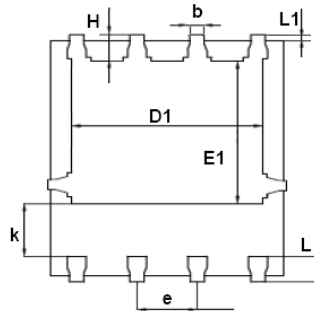
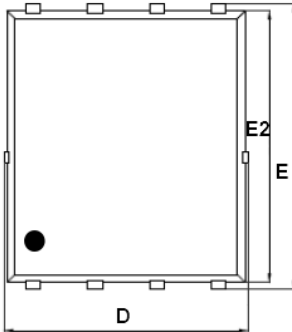


Figure 11. Unclamped Inductive Switching Waveform

Mechanical Dimensions for PDFN5060-8L

COMMON DIMENSIONS

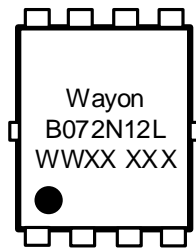


SYMBOL	MM	
	MIN	MAX
A	0.90	1.20
A3	0.15	0.35
D	4.80	5.40
E	5.90	6.35
D1	3.61	4.31
E1	3.30	3.92
E2	5.65	6.06
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.61
θ	0°	12°

Ordering Information

Part	Package	Marking	Packing method
WMB072N12LG2	PDFN5060-8L	B072N12L	Tape and Reel

Marking Information



B072N12L = Device code

WWXX XXX= Date code

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