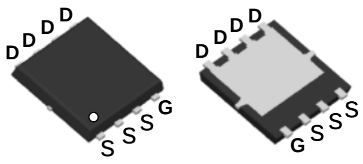
WAYON

WMB085N10LG2

100V N-Channel Enhancement Mode Power MOSFET



PDFN5060-8L

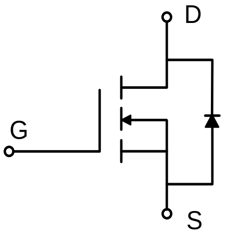
Description

WMB085N10LG2 uses Wayon's 2nd generation POWERTRENCH MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications

Features

- V_{DS}= 100 V, I_D = 62A(Silicon Limited)
  $R_{DS(on)}$ < 8.5mΩ @ V_{GS} = 10 V
  $R_{DS(on)}$ < 10.5mΩ @ V_{GS} = 4.5V
- Green Device Available
- Low Gate Charge
- 100% EAS Guaranteed
- Low $R_{DS(ON)}$

RoHS compliant



Applications

- Power Management Switches
- Synchronous Rectification for AC/DC Quick Charger

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current@10V[1]	T_C=25℃	I_D	62	A
	T_C=70℃		48	
Pulsed Drain Current[2]		I_{DM}	290	A
Single Pulse Avalanche Energy[3]		EAS	80	mJ
Avalanche Current		I_{AS}	40	A
Total Power Dissipation[4]	T_C=25℃	P_D	81	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[1]	$R_{θJA}$	55	°C/W
Thermal Resistance from Junction-to-Case[1]	$R_{θJC}$	1.2	°C/W

Electrical Characteristics T_c = 25°C, unless otherwise noted

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	-	-	V
Gate-body Leakage Current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25℃	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
	T_J=55℃			-	-	5	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	-	2.3	V
Drain-Source On-Resistance[2]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 13.5A	-	6.5	8.5	mΩ
			V_{GS} = 4.5V, I_D = 11.5A	-	7.8	10.5	
Forward Transconductance		g_{fs}	V_{DS} = 5V, I_D = 20A	-	85	-	S
Dynamic Characteristics							
Input Capacitance		C_{iss}	V_{DS} = 50V, V_{GS} =0V, f =1MHz	-	2858	-	pF
Output Capacitance		C_{oss}		-	450	-	
Reverse Transfer Capacitance		C_{rss}		-	13.5	-	
Switching Characteristics							
Gate Resistance		R_g	V_{DS}=0V , V_{GS}=0V , f=1MHz	-	3.0	-	Ω
Total Gate Charge		Q_g	V_{GS} = 4.5V,V_{DS} = 50V, I_D=13.5A	-	21.2	-	nC
Total Gate Charge		Q_g	V_{GS} = 10V,V_{DS} = 50V, I_D=13.5A	-	47	-	
Gate-Source Charge		Q_{gs}		-	9.5	-	
Gate-Drain Charge		Q_{gd}		-	6.8	-	
Turn-On Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DD} =50V, R_G = 3Ω, I_D= 13.5A	-	19	-	nS
Rise Time		t_r		-	47	-	
Turn-Off Delay Time		$t_{d(off)}$		-	121	-	
Fall Time		t_f		-	76	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[2]		V_{SD}	I_S = 1A, V_{GS} = 0V	-	-	1.1	V
Continuous Source Current[1,5]		I_S	V_G=V_D=0V,Force Current	-	-	62	A
Body Diode Reverse Recovery Time		t_{rr}	I_F = 13.5A,dI/dt =500A/μs	-	51	-	nS
Body Diode Reverse Recovery Charge		Q_{rr}		-	120	-	nC

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=40A

4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

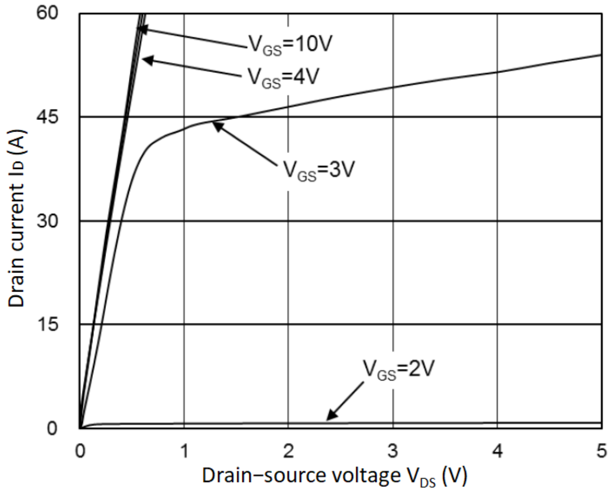


Figure 1. Output Characteristics

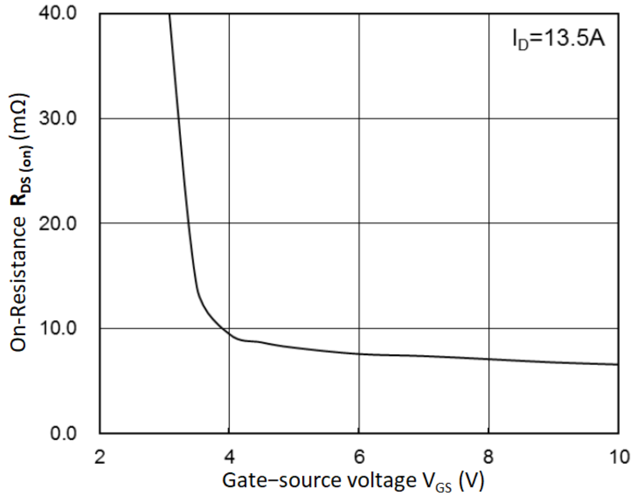


Figure 2. R_{DS}(on) vs. V_{GS}

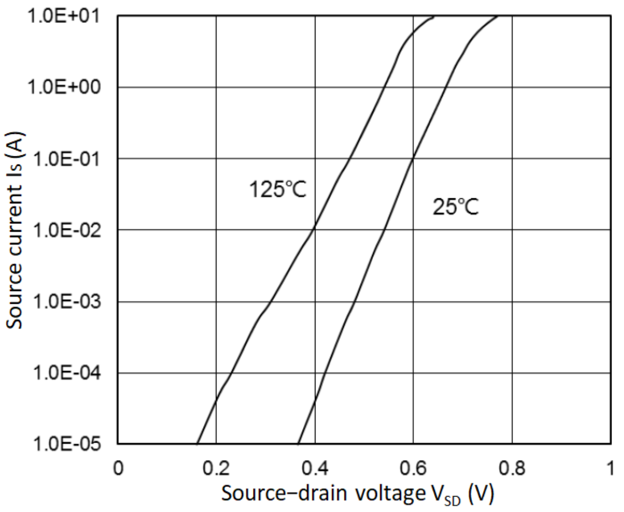


Figure 3. Forward Characteristics of Reverse

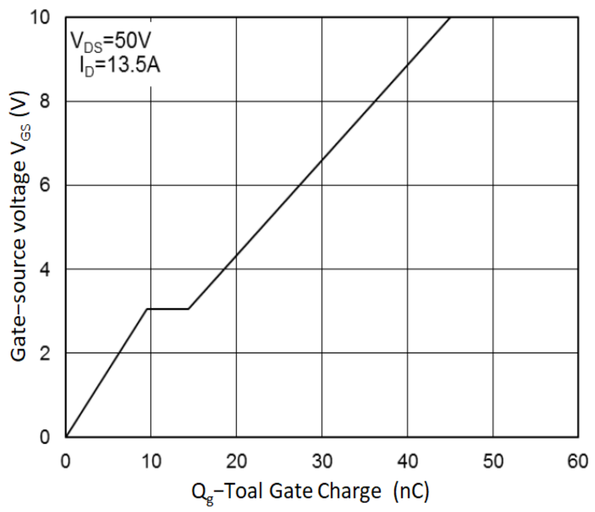


Figure 4. Gate Charge Characteristics

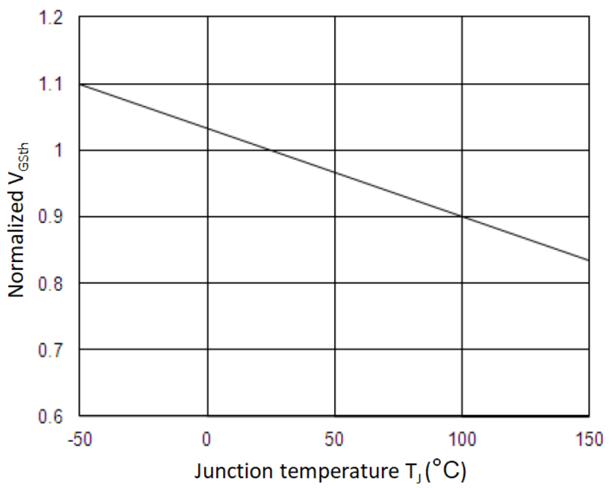


Figure 5. Normalized V_{GSth} vs. T_J

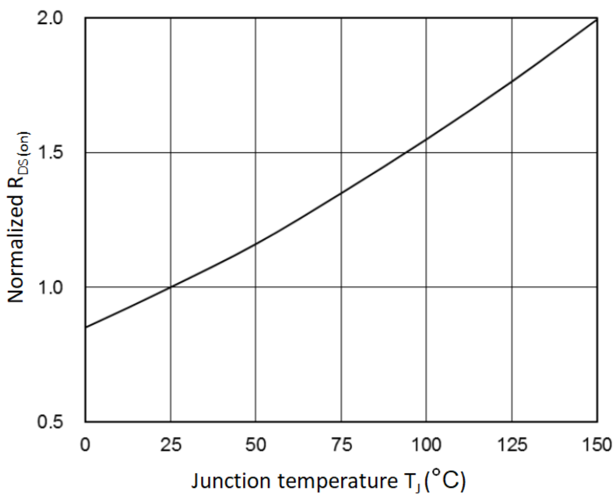
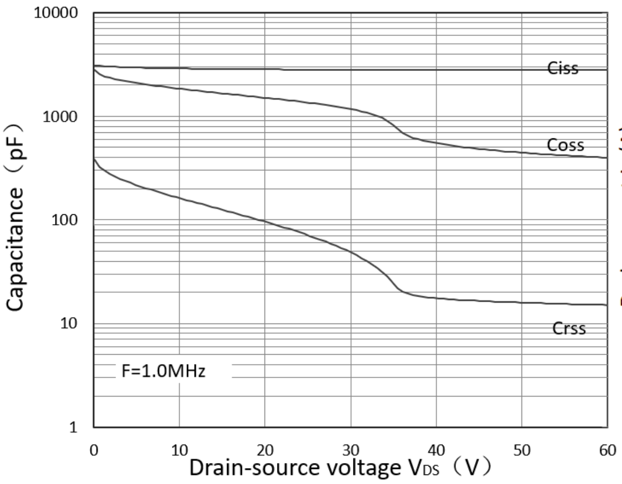


Figure 6. Normalized $R_{DS(on)}$ vs. T_J



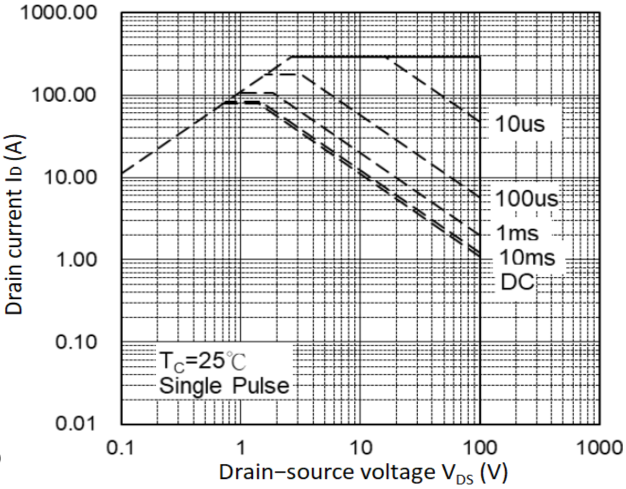


Figure 7. Capacitance Characteristics

Figure 8. Safe Operating Area

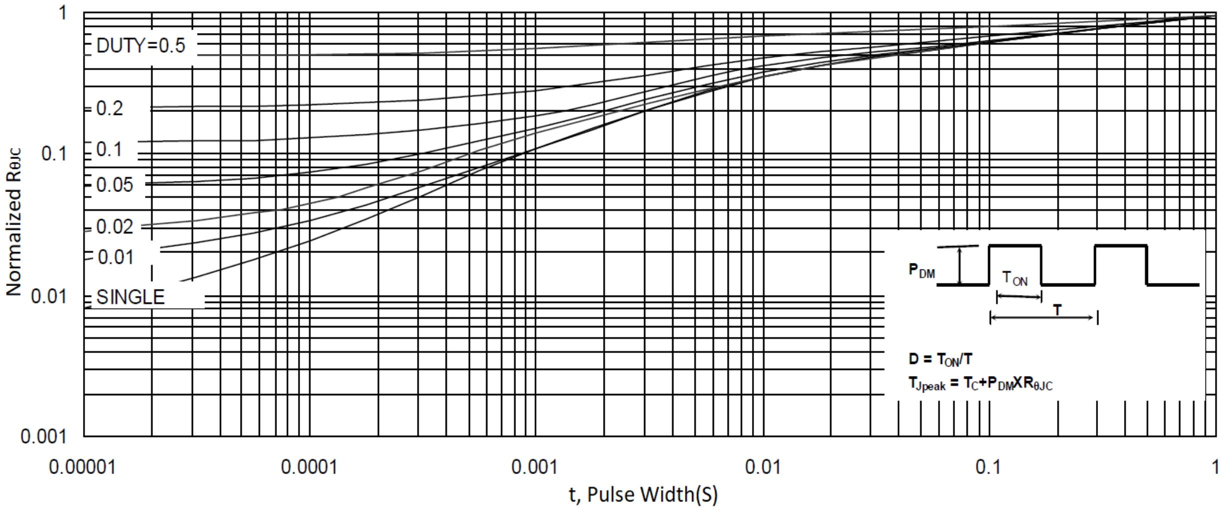
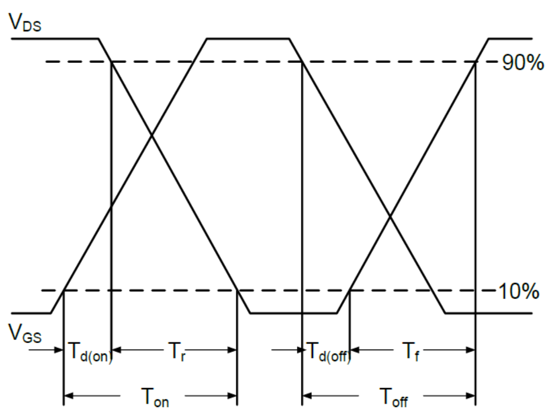


Figure 9. Normalized Maximum Transient Thermal Impedance



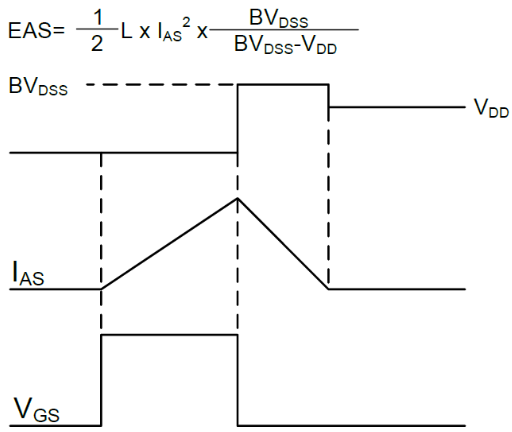
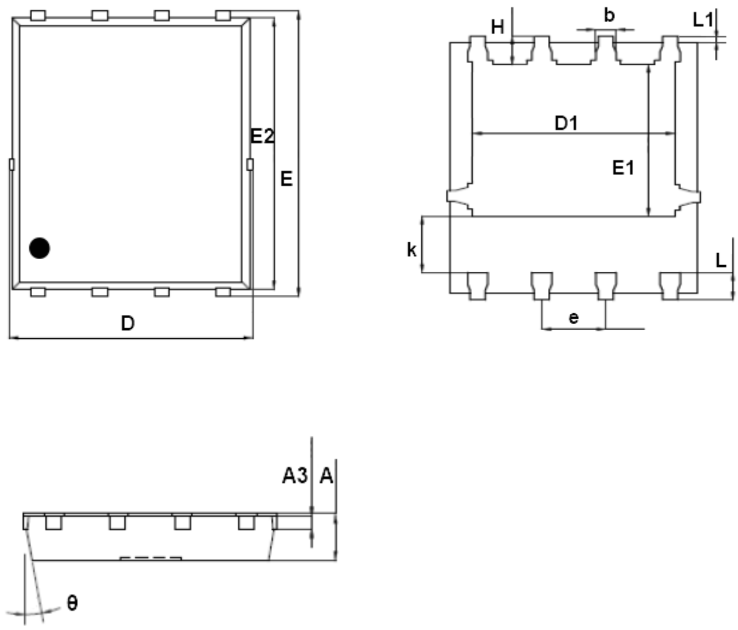


Figure 10. Switching Time Waveform

Figure 11. Unclamped Inductive Switching Waveform

Mechanical Dimensions for PDFN5060-8L



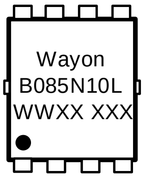
COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	0.90	1.17
A3	0.20	0.35
D	4.80	5.40
E	5.90	6.15
D1	3.61	4.31
E1	3.3	3.78
E2	5.65	5.85
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.61
θ	0°	12°

Ordering Information

Part	Package	Marking	Packing method
WMB085N10LG2	PDFN5060-8L	B085N10L	Tape and Reel

Marking Information



B085N10L = Device code

WWXX XXX= Date code

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