

## 30V N-Channel Enhancement Mode Power MOSFET

### Description

WMB58N03T1 uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Features

- $V_{DS} = 30\text{ V}$ ,  $I_D = 58\text{ A}$   
 $R_{DS(on)} < 8.5\text{ m}\Omega @ V_{GS} = 10\text{ V}$   
 $R_{DS(on)} < 14\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Low  $R_{DS(on)}$
- Low Gate Charge
- 100% EAS Guaranteed

### Applications

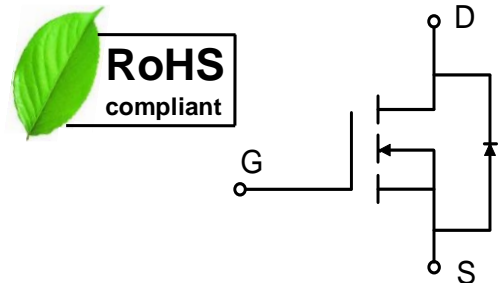
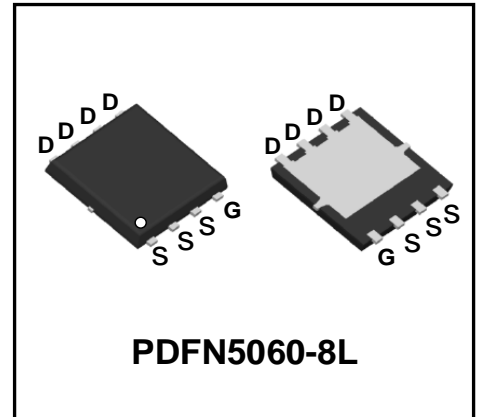
- Power Management Switches
- DC/DC Converter

### Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current@10V <sup>1</sup>	$T_C = 25^\circ\text{C}$	$I_D$	58	A
	$T_C = 100^\circ\text{C}$		38	
	$T_A = 25^\circ\text{C}$		12	
	$T_A = 70^\circ\text{C}$		9.6	
Pulsed Drain Current <sup>2</sup>		$I_{DM}$	115	A
Single Pulse Avalanche Energy <sup>3</sup>		<b>EAS</b>	57.8	mJ
Avalanche Current		$I_{AS}$	34	A
Total Power Dissipation <sup>4</sup>	$T_C = 25^\circ\text{C}$	$P_D$	46	W
	$T_A = 25^\circ\text{C}$		2	
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>1</sup>	$R_{\theta JA}$	62	$^\circ\text{C/W}$
Thermal Resistance from Junction-to-Case <sup>1</sup>	$R_{\theta JC}$	2.7	$^\circ\text{C/W}$



**Electrical Characteristics**  $T_c = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30	-	-	V
Gate-body Leakage current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$T_J=25^\circ\text{C}$	$V_{DS} = 24V, V_{GS} = 0V$	-	-	1	$\mu A$
	$T_J=55^\circ\text{C}$		-	-	5	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.7	2.5	V
Drain-Source On-Resistance <sup>2</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 30A$	-	6.7	8.5	m $\Omega$
		$V_{GS} = 4.5V, I_D = 15A$	-	9	14	
Forward Transconductance	$g_{fs}$	$V_{DS} = 5V, I_D = 30A$	-	38	-	S
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{MHz}$	-	1100	-	pF
Output Capacitance	$C_{oss}$		-	163	-	
Reverse Transfer Capacitance	$C_{rss}$		-	131	-	
<b>Switching Characteristics</b>						
Gate Resistance	$R_g$	$V_{DS} = 0V, V_{GS} = 0V, f = 1\text{MHz}$	-	2.5	-	$\Omega$
Total Gate Charge	$Q_g$	$V_{GS} = 4.5V, V_{DS} = 15V, I_D = 15A$	-	12.6	-	nC
Gate-Source Charge	$Q_{gs}$		-	4.2	-	
Gate-Drain Charge	$Q_{gd}$		-	5.1	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 15V, R_G = 3.3\Omega, I_D = 15A$	-	4.6	-	nS
Rise Time	$t_r$		-	12.2	-	
Turn-Off Delay Time	$t_{d(off)}$		-	26.6	-	
Fall Time	$t_f$		-	8	-	
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	$I_S = 1A, V_{GS} = 0V$	-	-	1	V
Continuous Source Current <sup>1,5</sup>	$I_S$	$V_G = V_D = 0V$ , Force Current	-	-	58	A
Reverse Recovery Time	$t_{rr}$	$I_F = 30A, dI/dt = 100A/\mu s$	-	9.2	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	2	-	nC

Note :

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=34A$
- The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

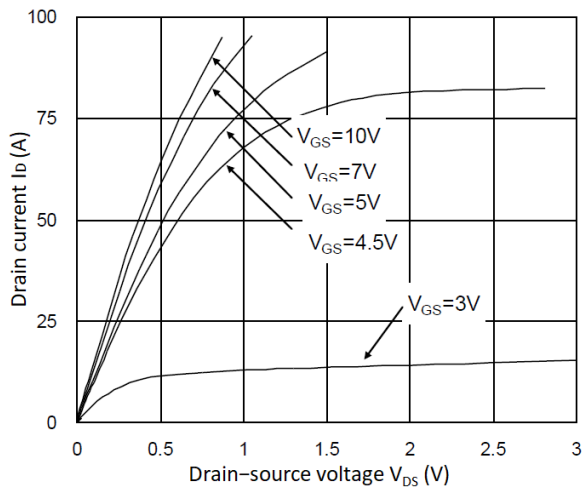


Figure 1. Typical Output Characteristics

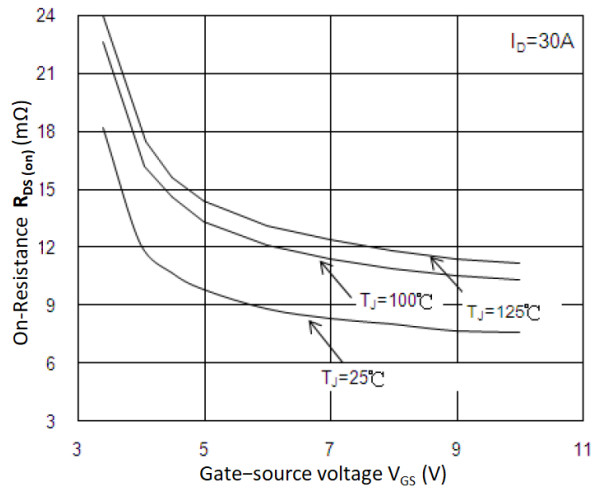


Figure 2.  $R_{DS(on)}$  vs.  $V_{GS}$

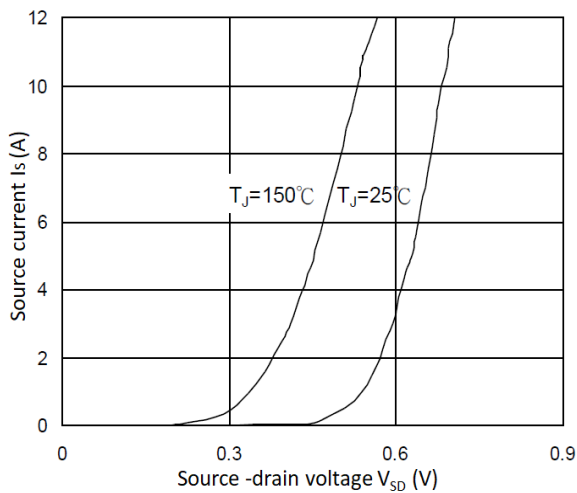


Figure 3. Forward Characteristics Of Reverse

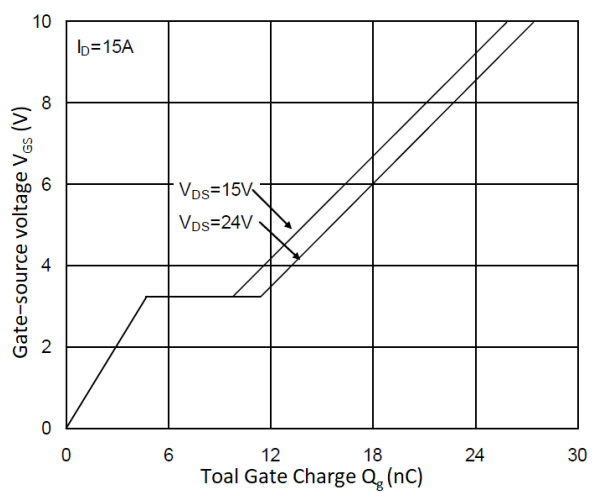


Figure 4. Gate Charge Characteristics

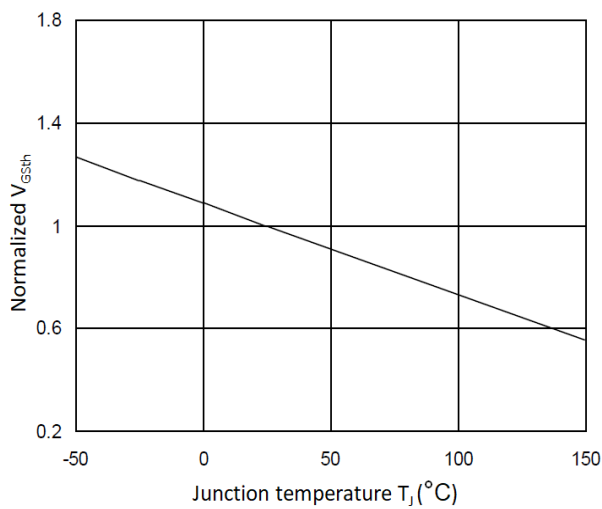


Figure 5. Normalized  $V_{GS(th)}$  vs.  $T_J$

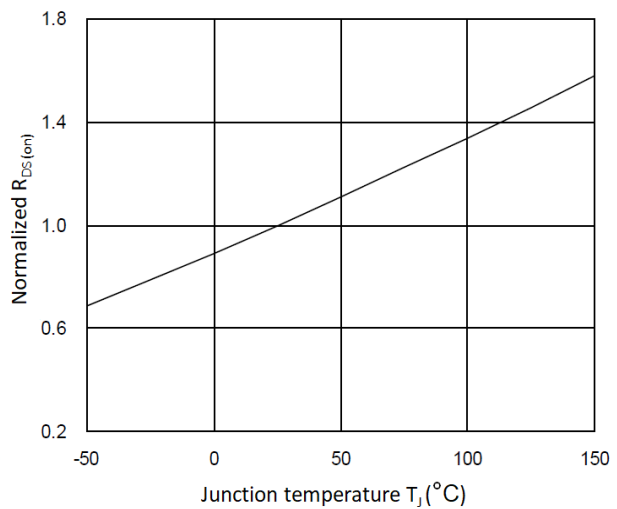


Figure 6. Normalized  $R_{DS(on)}$  vs.  $T_J$

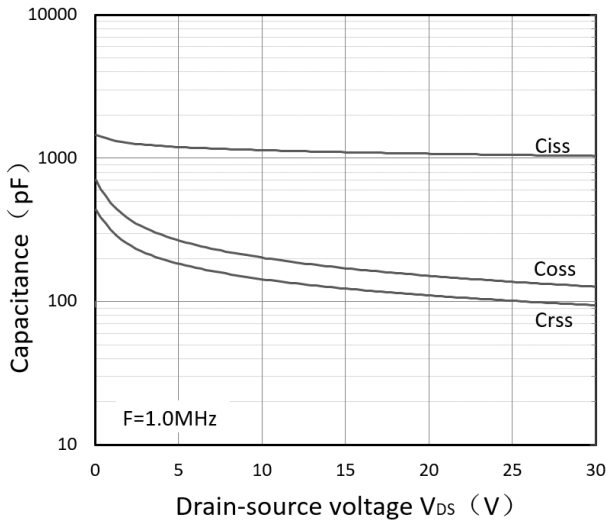


Figure 7. Capacitance Characteristics

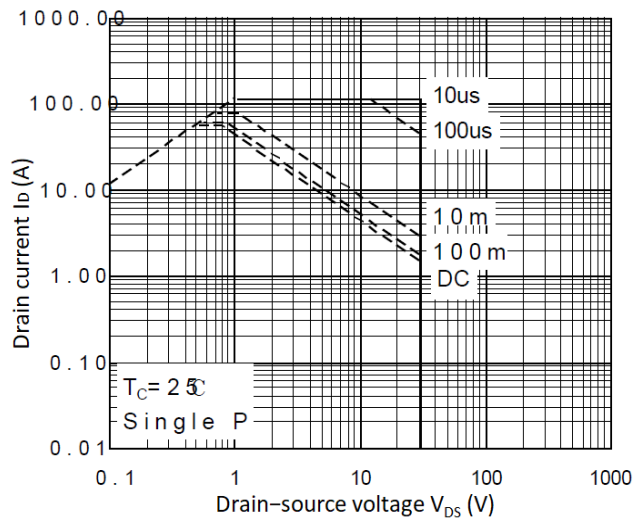


Figure 8. Safe Operating Area

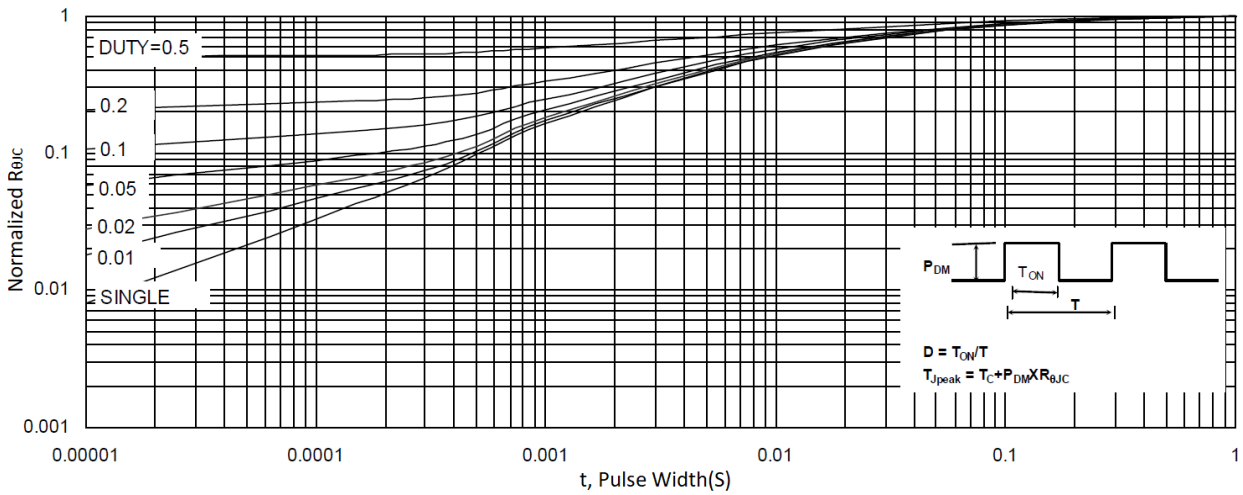


Figure 9. Normalized Maximum Transient Thermal Impedance

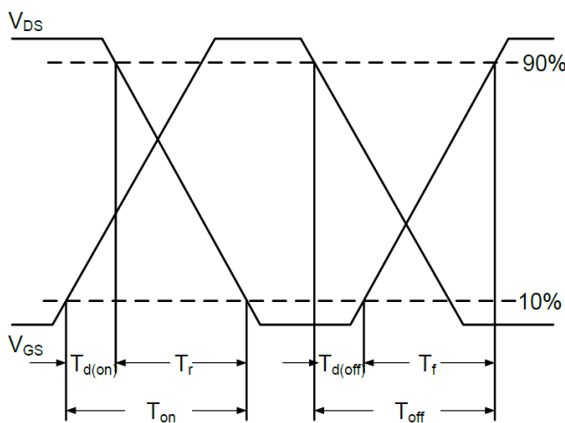


Figure 10. Switching Time Waveform

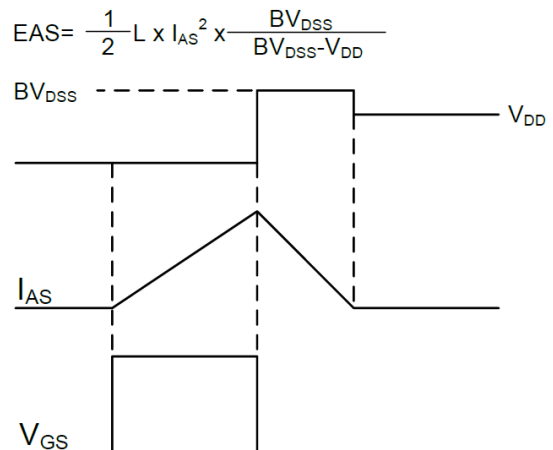
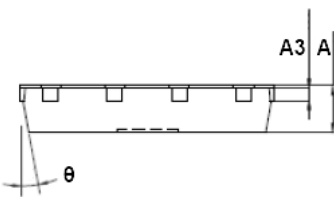
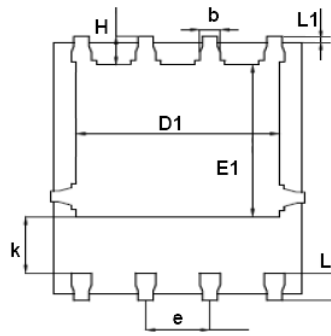
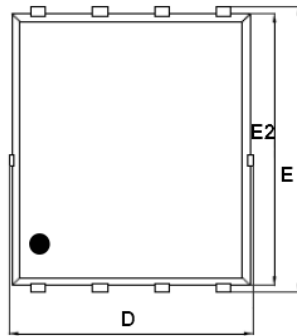


Figure 11. Unclamped Inductive Switching Waveform

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

## Mechanical Dimensions for PDFN5060-8L

## COMMON DIMENSIONS

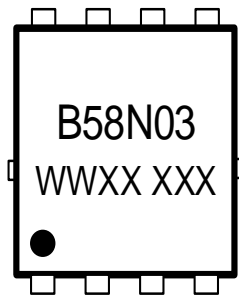


SYMBOL	MM	
	MIN	MAX
A	0.90	1.17
A3	0.20	0.35
D	4.80	5.40
E	5.90	6.15
D1	3.61	4.31
E1	3.3	3.78
E2	5.65	5.85
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.61
$\theta$	0°	12°

## Ordering Information

Part	Package	Marking	Packing method
WMB58N03T1	PDFN5060-8L	B58N03	Tape and Reel

## Marking Information



B58N03 = Device code

WWXX XXX= Date code

## Contact Information

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